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Technology Development & Design for 22 nm InGaAs/InP-channel MOSFETs

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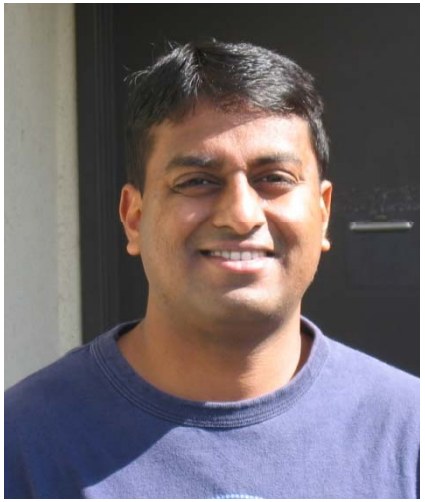

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Why III-V CMOS ?

Why Develop III-V MOSFETs ?

Silicon MOSFETs continue to scale...

...22 nm is feasible in production (or so the Silicon industry tells us...)

...16 nm ? -- it is not yet clear

If we can't make MOSFETs yet smaller,

instead move the electrons faster:

$$I_d / W_g = q n_s v \qquad I_d / Q_{transit} = v / L_g$$

III-V materials → lower m* → higher velocities

Serious challenges:

High-K dielectrics on InGaAs channels,

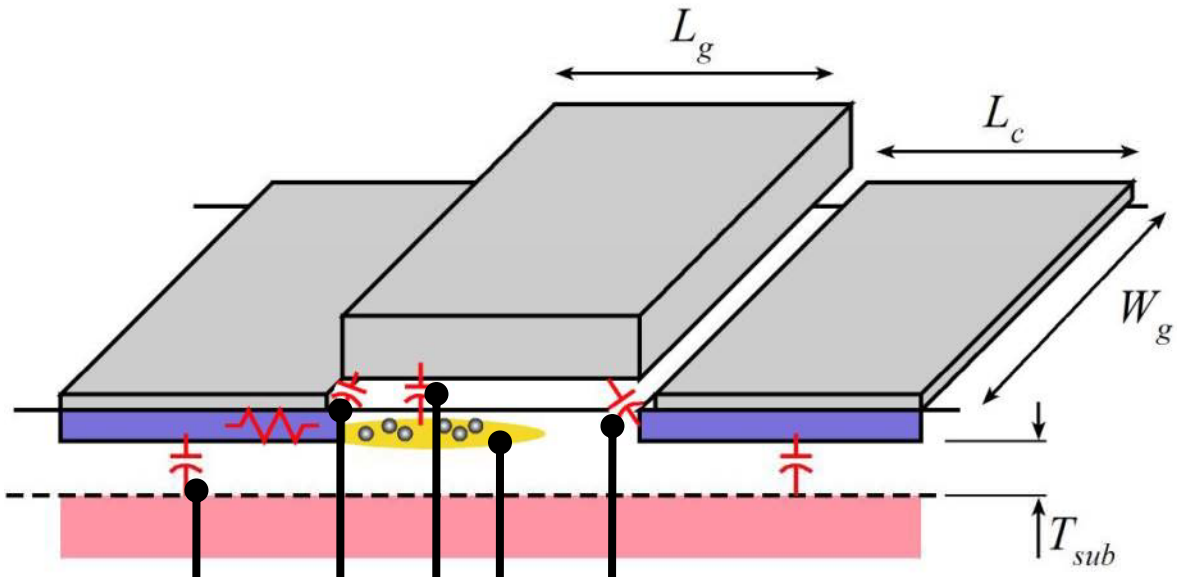
InGaAs growth on Si

True MOSFET fabrication processes

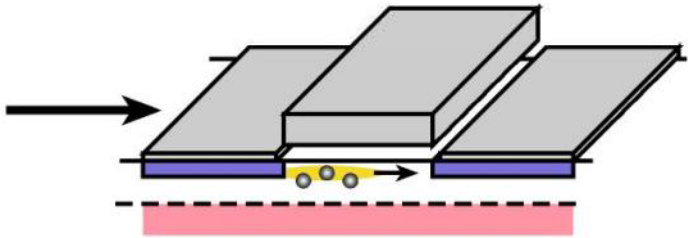
Designing small FETs which use big (low m*) electrons

Simple FET Scaling

Goal: *double transistor bandwidth when used in any circuit*
→ reduce 2:1 all capacitances and all transport delays
→ keep constant all resistances, voltages, currents



All lengths, widths, thicknesses reduced 2:1



S/D contact resistivity reduced 4:1

$C_{gd} / W_g \sim \varepsilon$

$g_m / W_g \sim v\varepsilon / T_{ox}$

$C_{gs} / W_g \sim \varepsilon \cdot L_g / T_{ox}$

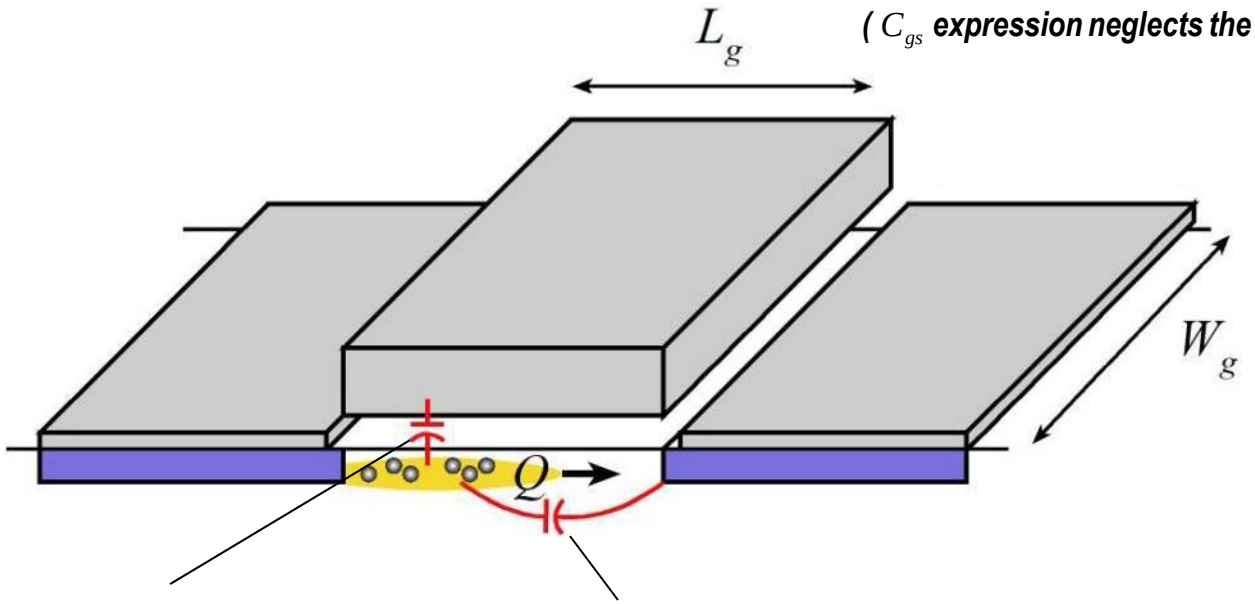
$C_{gs,f} / W_g \sim \varepsilon$

$C_{sb} / W_g \sim \varepsilon \cdot L_c / T_{sub}$

If T_{ox} cannot scale with gate length,
$C_{parasitic} / C_{gs}$ increases, ✗
g_m / W_g does not increase
hence $C_{parasitic} / g_m$ does not scale ✗

FET scaling: Output Conductance & DIBL

(C_{gs} *expression neglects the effect of a finite density of states*)



$$C_{gs} \sim \varepsilon W_g L_g / T_{ox} \qquad C_{d-ch} \sim \varepsilon W_g$$

$$I_d = Q/\tau \quad \text{where} \quad \delta Q = C_{gs}\delta V_{gs} + C_{d-ch}\delta V_{ds}$$

transconductance *output conductance*

→ **Keep L_g / T_{ox} constant as we scale L_g**

Well-Known: Si FETs No Longer Scale Perfectly

Effective oxide thickness is no longer scaling in proportion to L_g

T_{ox} (nm) [2]	2.2	2.1	2.0	1.9	1.6	1.5	1.4	1.4	1.3
Gate Length (nm) [2]	75	65	53	45	37	32	28	25	22
g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$ [3]	47	40	32	30	30	30	30	30	30
1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$) [4]	190	180	160	140	100	90	80	80	70
σ V_{th} matching ($mV \cdot \mu m$) [5]	6	6	6	6	5	5	5	5	5
I_{ds} ($\mu A/\mu m$) [6]	19	15	13	11	9	8	7	6	6
Peak F_t (GHz) [7]	120	140	170	200	240	280	320	360	400
Peak F_{max} (GHz) [8]	200	220	270	310	370	420	480	530	590

(ITRS roadmap copied from Larry Larson's files)

High - K gate dielectrics : SiO_2 interlayer limits acheivable (capacitance / area)

Gate capacitance density is not increasing rapidly

Output conductance is degrading

$\left(C_{\text{parasitic}}/I_d\right)$ is improving only slowly ...soon will dominate gate delay

Highly Scaled MOSFETs: What Are Our Goals ?

Low off-state current (10 nA/μm) for *low static dissipation*

→ minimum subthreshold slope → minimum L_g / T_{ox}

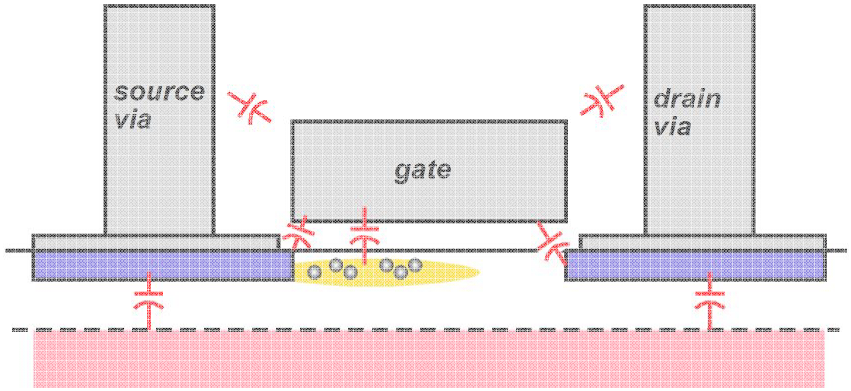
low gate tunneling, low band-band tunneling

Low delay $C_{FET}\ \Delta V/I_d$ *in gates where transistor capacitances dominate.*

Parasitic capacitances are 0.5-1.0 fF/μm

→ while low C_{gs} is good,

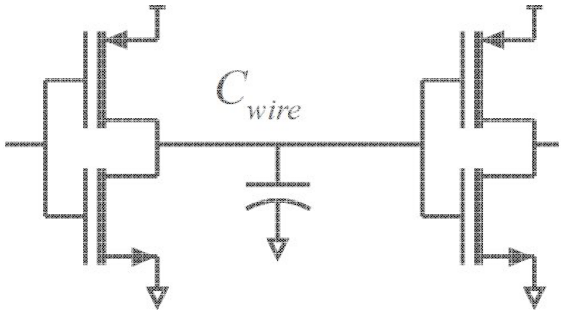
high I_d is much better



Low delay $C_{wire}\ \Delta V/I_d$ *in gates where wiring capacitances dominate.*

large FET footprint → long wires between gates

→ need high I_d / W_g ; target ~6 mA/μm



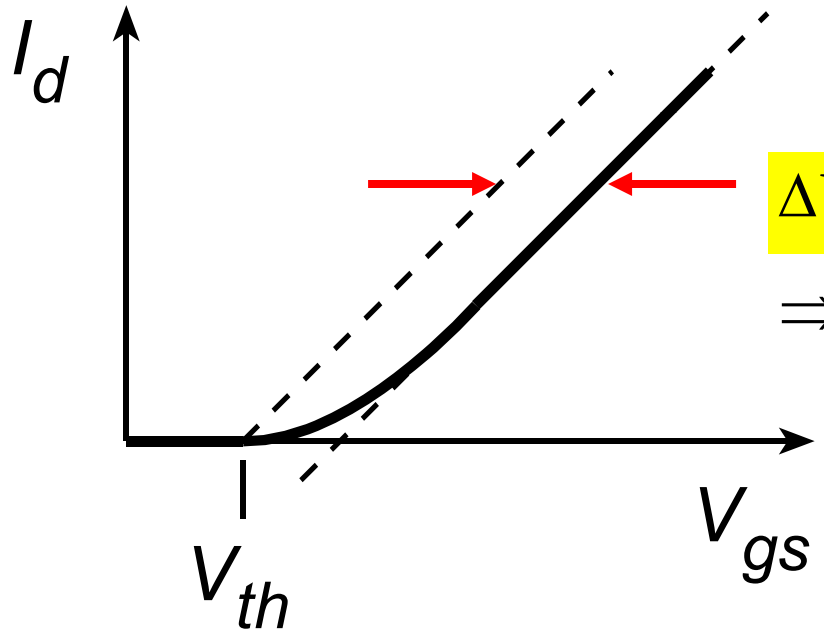
short transit time alone (low $C_{gs,\ int}\ \Delta V_{gs}/\Delta I_d$) is not sufficient

III-V MOSFETs: Drive Current and CV/I delay

III-V CMOS: The Benefit Is Low Mass, Not High Mobility

Simple drift - diffusion theory, nondegenerate, far above threshold :

$$I_D \approx c_{ox} W_g v_{injection} (V_{gs} - V_{th} - \Delta V) \qquad \text{where } v_{injection} \sim v_{thermal} = (kT / m^*)^{1/2}$$



$$\Delta V = v_{injection} L_g / \mu$$

$\Rightarrow$ Ensure that $\Delta V << (V_{gs} - V_{th})$

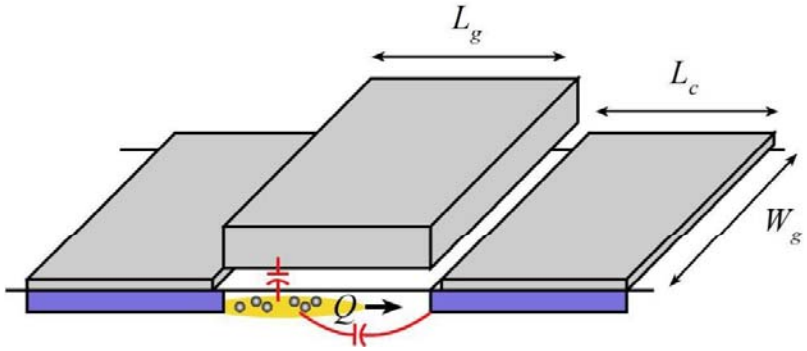
~ 700 mV

low effective mass → high currents

mobilities above ~ 1000 cm²/V-s of little benefit at 22 nm Lg

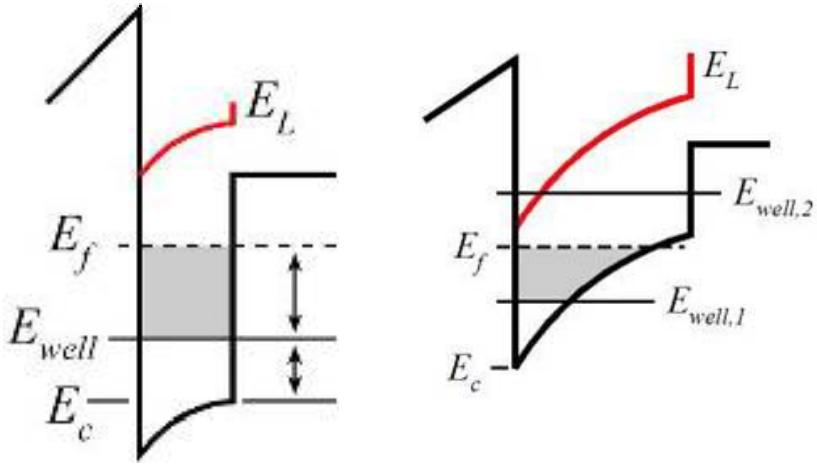
Low Effective Mass Impairs Vertical Scaling

Shallow electron distribution needed for high g_m / G_{ds} ratio, low drain-induced barrier lowering.



Energy of L^{th} well state $\sim L^2 / m^* T_{well}^2$.

For thin wells,
only 1st state can be populated.
For very thin wells,
1st state approaches L-valley.



Only one vertical state in well.
Mimimum ~ 5 nm well thickness.
→ Hard to scale below 22 nm L_g.

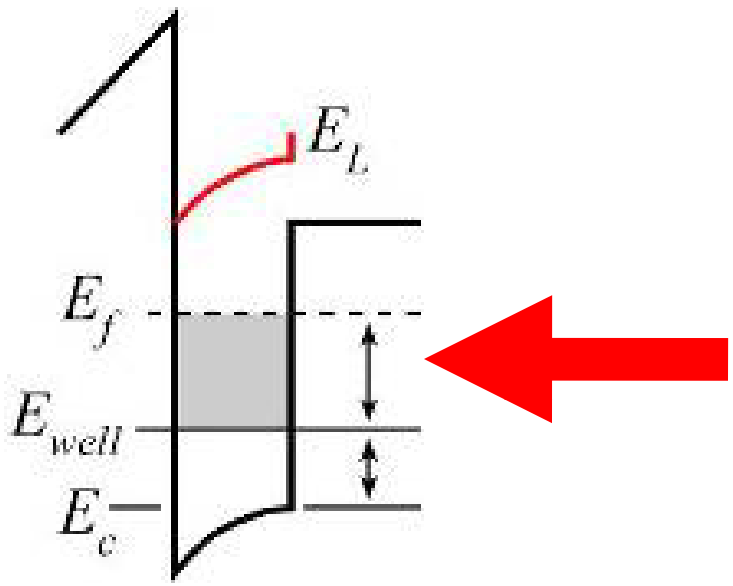
Density-Of-States Capacitance

$$E_f - E_{well} = n_s / (nm^* / 2\pi\hbar^2)$$

$$V_f - V_{well} = \rho_s / c_{dos}$$

where $c_{dos} = q^2 nm^* / 2\pi\hbar^2$

and n is the # of band minima



Two implications:

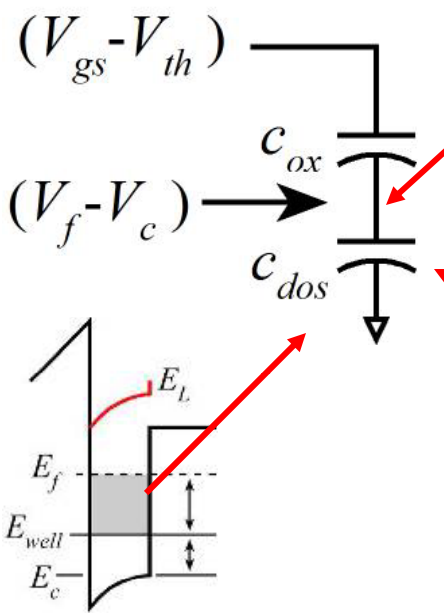
- With N_s >10^{13}/cm^2, electrons populate satellite valleys

Fischetti et al, IEDM2007

- Transconductance dominated by finite state density

Solomon & Laux , IEDM2001

Drive Current in the Ballistic & Degenerate Limits



Channel Fermi voltage = voltage applied to c_{dos}

determines Fermi velocity v_f through $E_f = qV_f = m^* v_f^2 / 2$

Channel charge : $\rho_s = c_{dos}(V_f - V_c) = \dfrac{c_{dos} c_{ox}}{c_{ox} + c_{dos}}(V_{gs} - V_{th})$

$c_{dos} = q^2 n m^* / 2\pi\hbar^2 = c_{dos,o} \cdot n \cdot (m^* / m_o)$, where n is the # of band minima

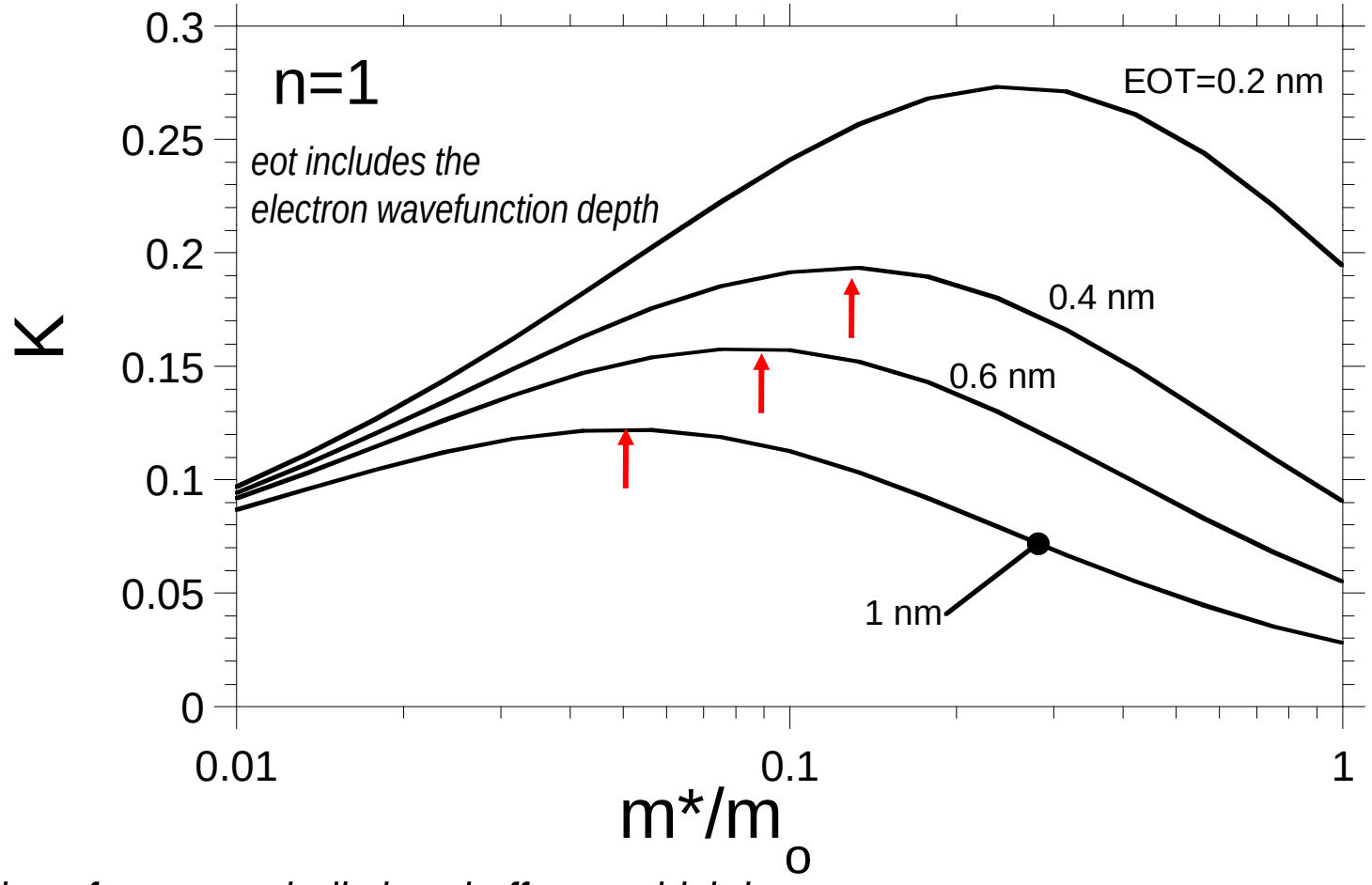
$$\Rightarrow \quad J = \left(84 \frac{\text{mA}}{\mu\text{m}}\right) \cdot \left(\frac{V_{gs} - V_{th}}{1\text{V}}\right)^{3/2} \cdot \frac{n \cdot (m^*/m_o)^{1/2}}{\left(1 + (c_{dos,o}/c_{ox}) \cdot n \cdot (m^*/m_o)\right)^{3/2}}$$

Ballistic but nondegenerate case : $J \approx (kT/m^*)^{1/2} c_{ox}(V_{gs} - V_{th})$

More careful analyses by Taur & Asbeck Groups, UCSD; Fischetti Group: U-Mass: IEDM2007

Drive Current in the Ballistic & Degenerate Limits

$$J = \underline{K} \cdot \left(84\frac{\text{mA}}{\mu\text{m}}\right) \cdot \left(\frac{V_{gs} - V_{th}}{1\,\text{V}}\right)^{3/2}, \quad \text{where } \underline{K} = \frac{n \cdot \left(m^*/m_o\right)^{1/2}}{\left(1 + (c_{dos,o}/c_{ox}) \cdot n \cdot (m^*/m_o)\right)^{3/2}}$$



Inclusive of non-parabolic band effects, which increase c_{dos} ,
InGaAs & InP have near-optimum mass for 0.4-1.0 nm EOT gate dielectrics

Rough Projections From Simple Ballistic Theory

22 nm gate length

0.5-1.0 fF/μm parasitic capacitances

Channel	*EOT*	*drive current* *(700 mV overdrive)*	*intrinsic gate capacitance*
InGaAs	*1 nm*	*6 mA/μm*	*0.2 fF/μm*
InGaAs	*1/2 nm*	*8.5 mA/μm*	*0.25 fF/μm*
Si	*1 nm*	*2.5-3.5 mA/μm*	*0.7 fF/μm*
Si	*1/2 nm*	*5-7 mA/μm*	*1.4 fF/μm*

InGaAs has much less gate capacitance

1 nm EOT → InGaAs gives much more drive current

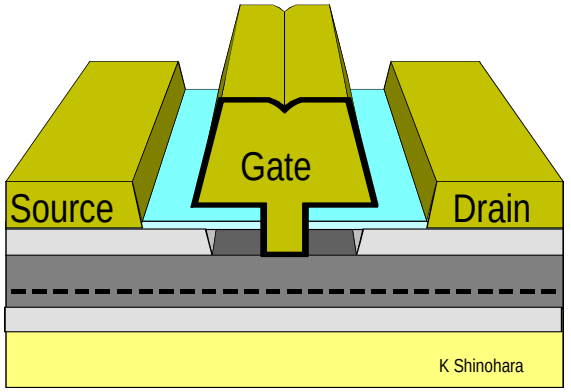
1/2 nm EOT → InGaAs & Si have similar drive current

InGaAs channel→ no benefit for sub-22-nm gate lengths

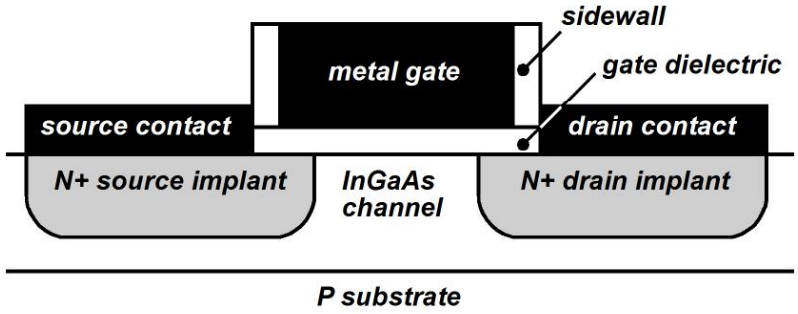
Device Structure
&
Process Flow

Device Fabrication: Goals & Challenges

III-V HEMTs are built like this→

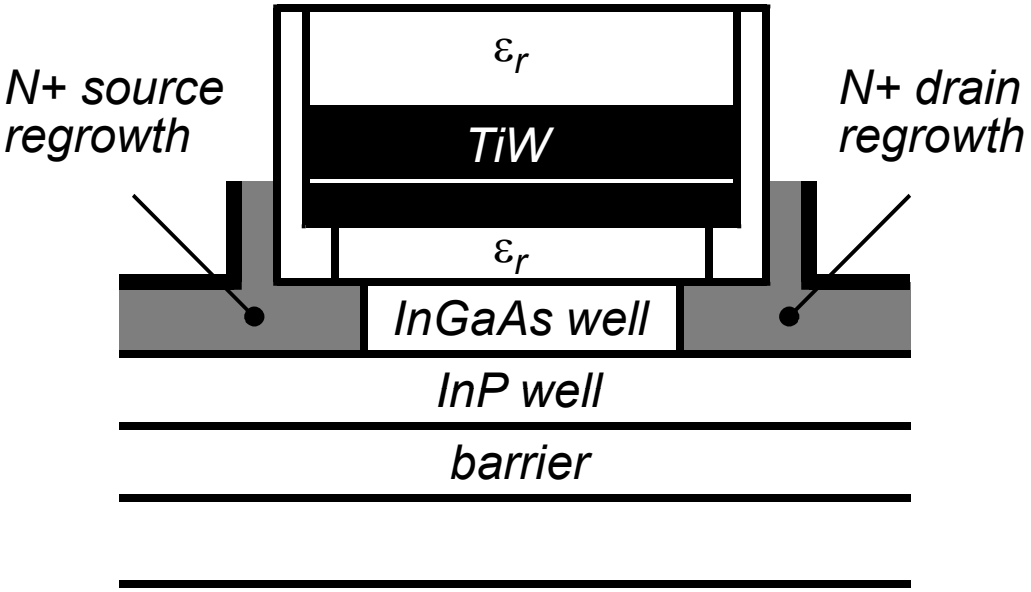


....and most
III-V MOSFETs are built like this→

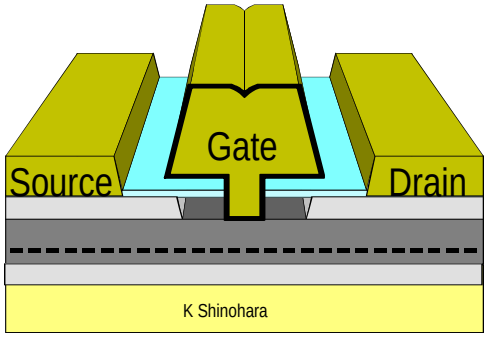


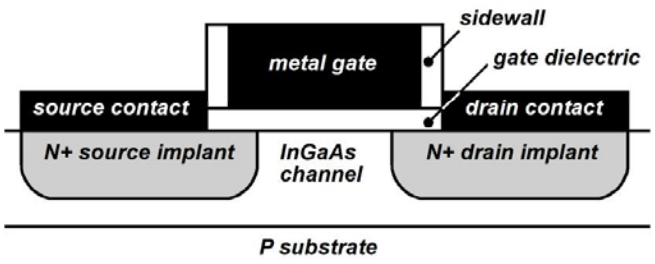
Device Fabrication: Goals & Challenges

Yet, we are developing,
at great effort,
a structure like this →



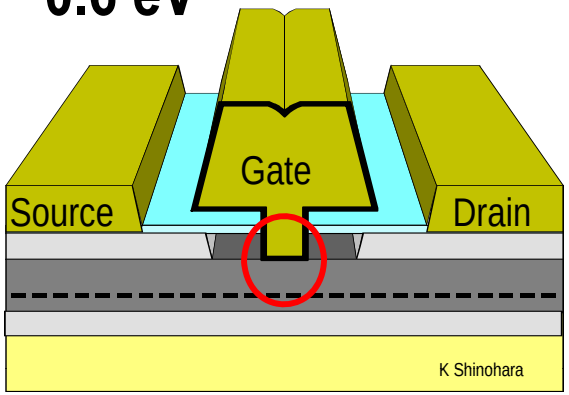
Why ?

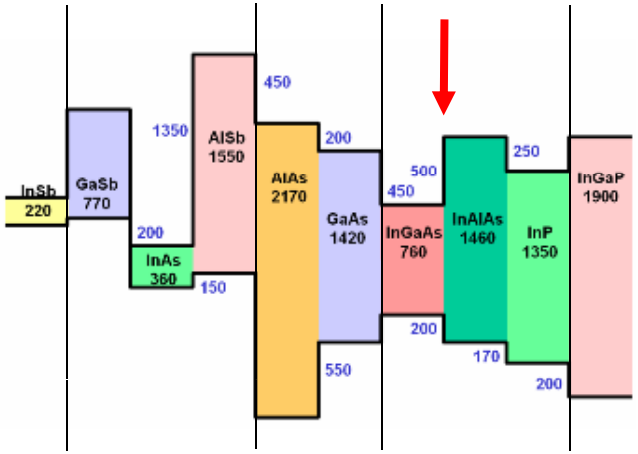




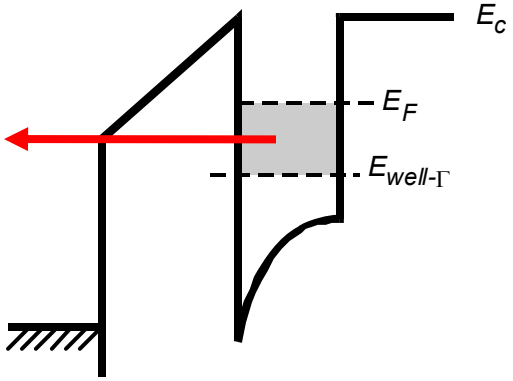
Why not just build HEMTs ? Gate Barrier is Low !

Gate barrier is low: ~0.6 eV

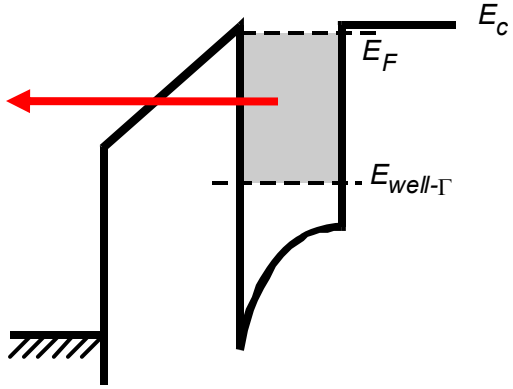




Tunneling through barrier
→ sets minimum thickness



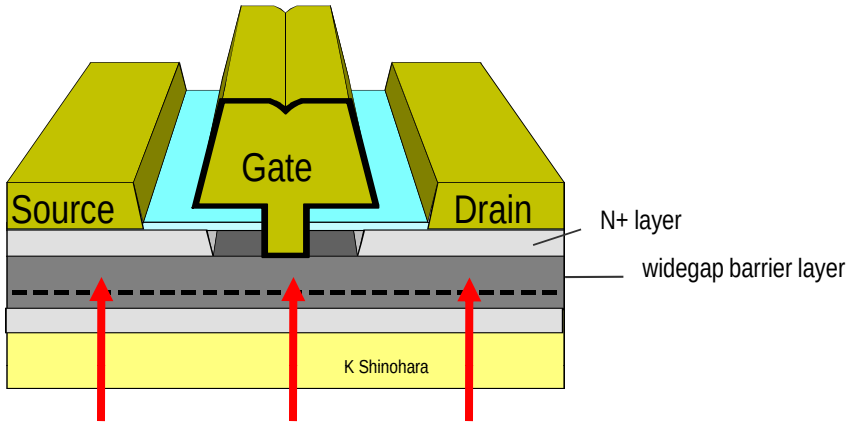
Emission over barrier
→ limits 2D carrier density



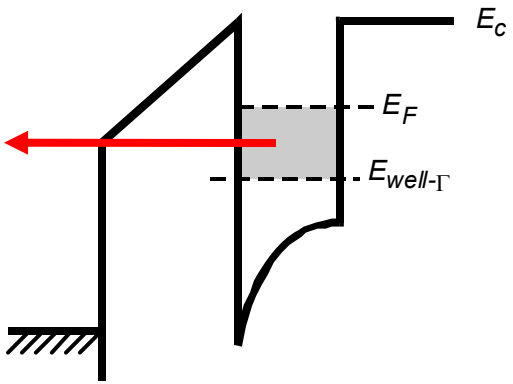
At $N_s = 10^{13}/\mathrm{cm}^2, (E_f - E_c) \sim 0.6\,\mathrm{eV}$

Why not just build HEMTs ?

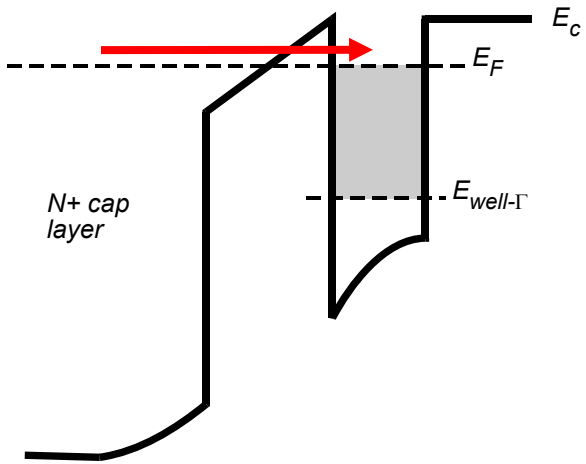
Gate barrier also lies under source / drain contacts



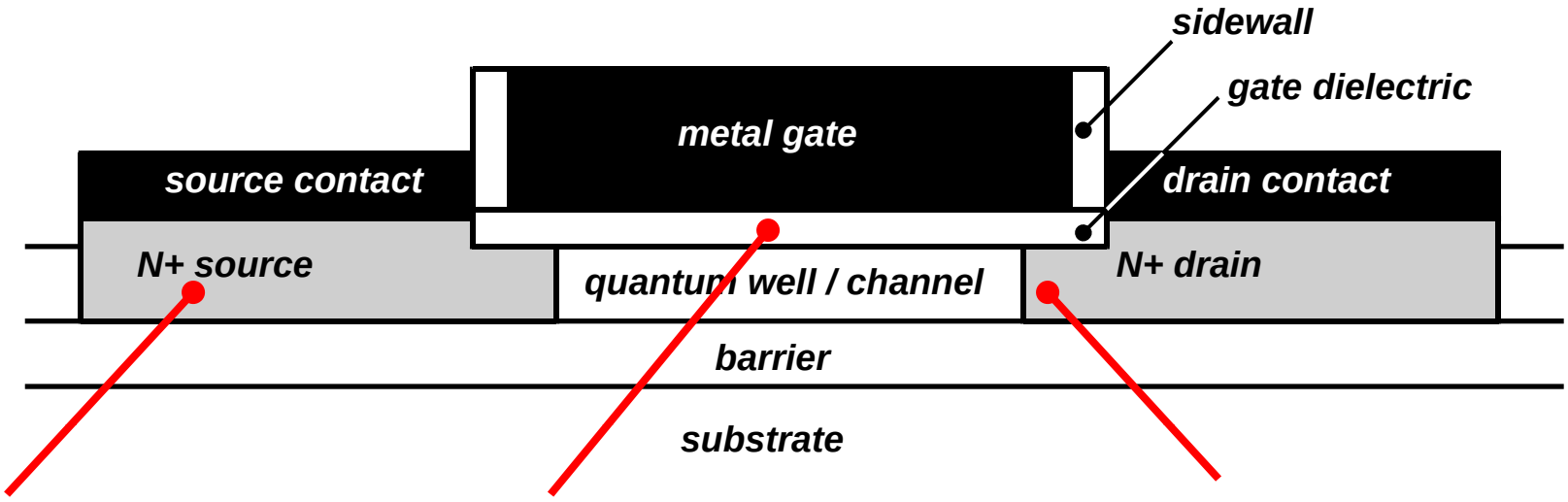
low leakage:
need high barrier under gate



low resistance:
need low barrier under contacts



The Structure We Need -- is Much Like a Si MOSFET



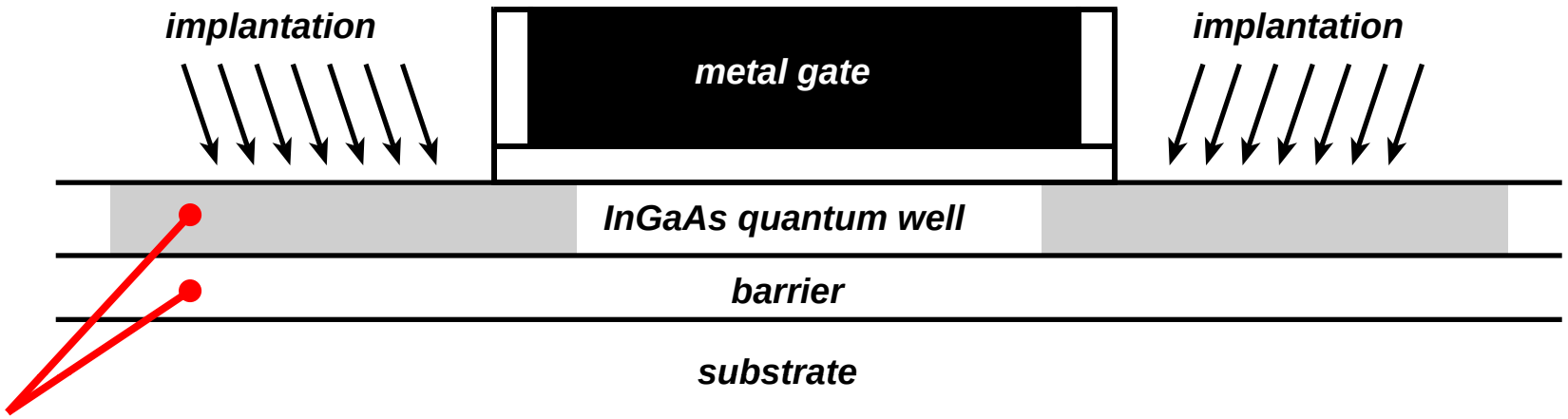
no gate barrier under S/D contacts

high-K gate barrier

Overlap between gate and N+ source/drain

How do we make this device ?

Source/Drain Implantation Does Not Look Easy



Implantation will intermix InGaAs well & InAlAs barrier

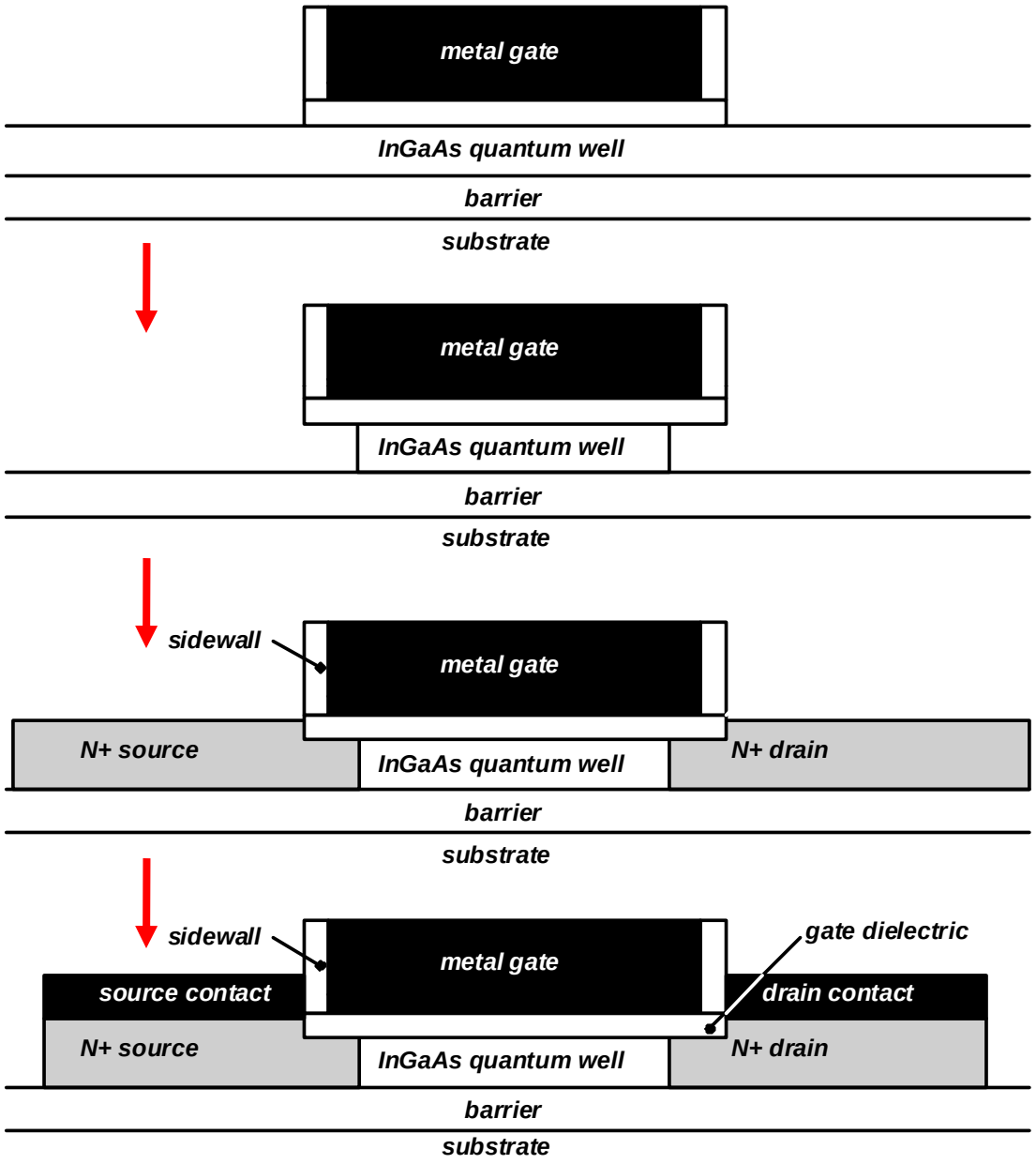
Annealing can't fix this.

Incommensurate sublimation of III vs. V elements during anneal

Need ~ 5 nm implant depth & ~ $6*10^{19}$ /cm^3 doping

Implanted structures have not shown the necessary low contact resistivity.

So, We Are Forming the Source/Drain By Regrowth



Process selected to meet 22 nm ITRS targets

But...

unlike HEMT process flows, fully established in 1980's...

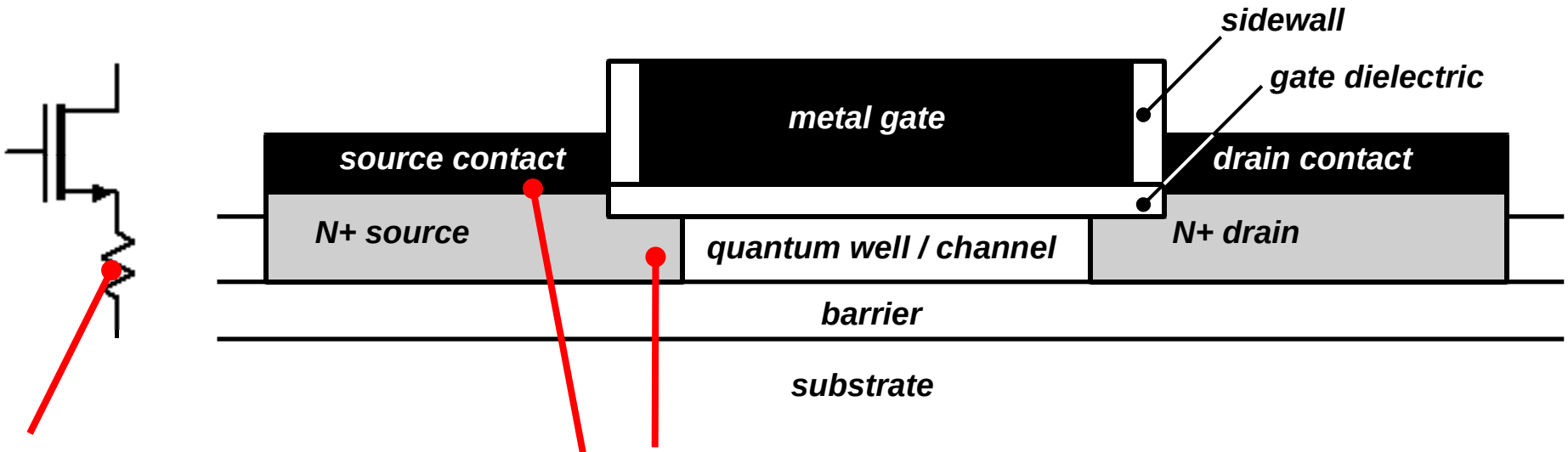
*...most process steps **here** are **completely new***

The technology is aggressive and challenging

The Required Performance is Formidable

~5 nm thick well **1 nm Insulator EOT**

Target ~7 mA/μm @ 700 mV gate overdrive



For $<10\%$ impact on drive current,

$I_D R_S < 70\ \text{mV}.$

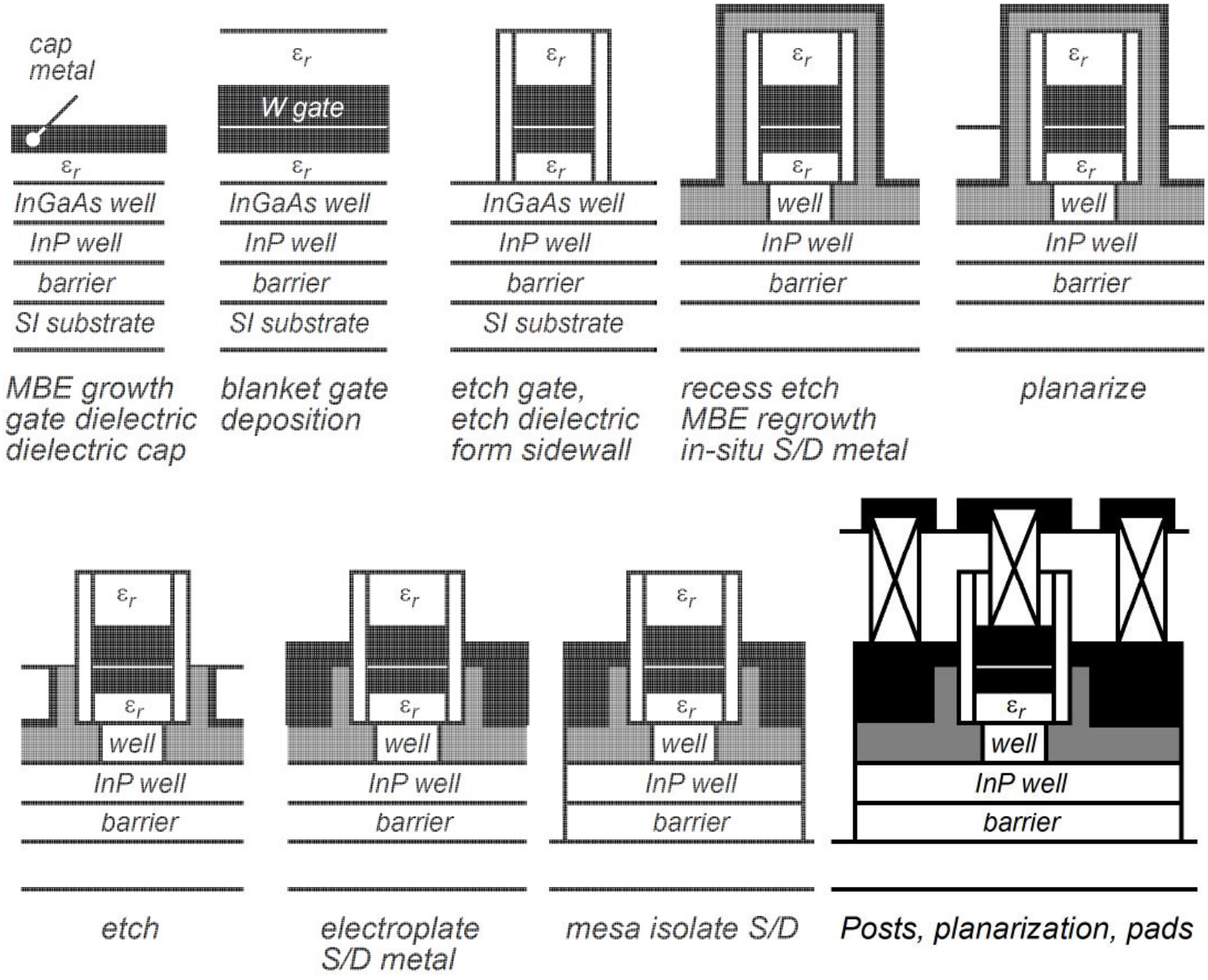
$\rightarrow R_s < 10\,\Omega - \mu\text{m}$

$(20\ \text{nm N} + \text{extension}) \times (100\,\Omega/\text{square}) = 2\,\Omega - \mu\text{m}$

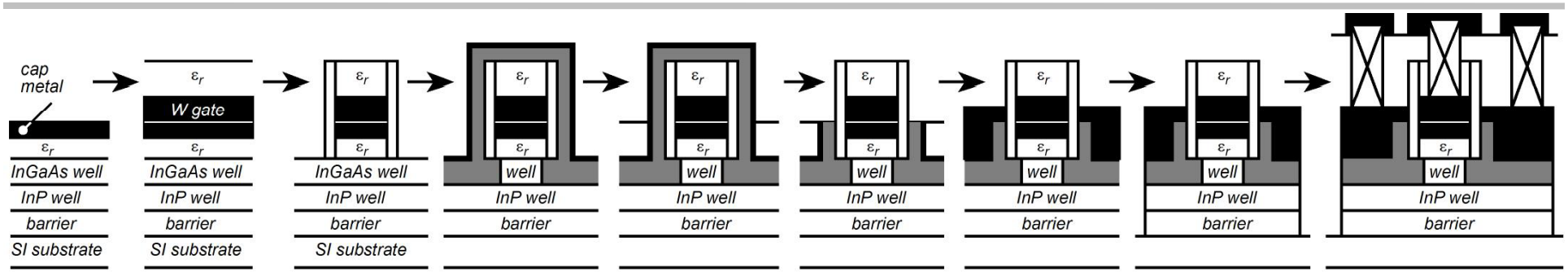
$(0.25\,\Omega - \mu\text{m}^2)\,/(25\ \text{nm wide contact}) = 10\,\Omega - \mu\text{m}$

Process Development

Process Flow with MBE Source/Drain Regrowth



Process Flow with MBE Source/Drain Regrowth



Gate Dielectrics

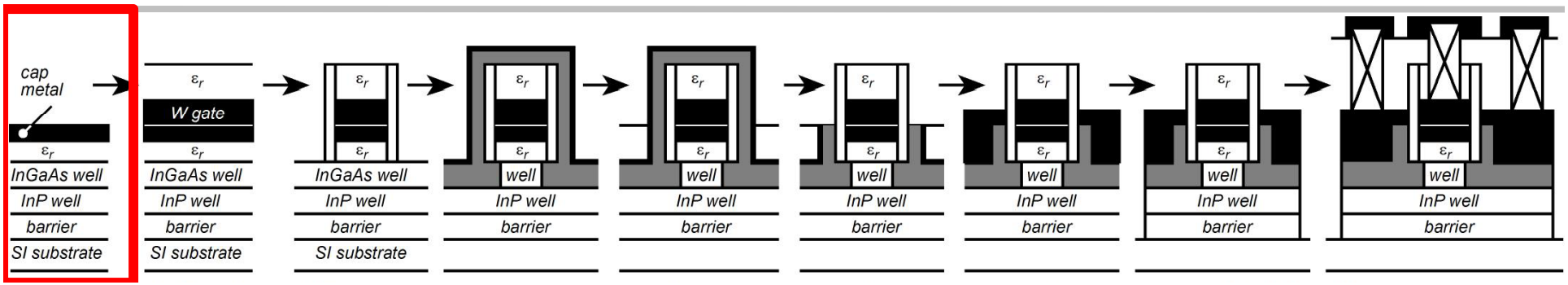
ALD Al_2O_3 from IBM (D. Sedana) & Stanford (P. McIntyre)

ALD ZrO_2 from Intel (S. Koveshnikov *et al*, DRC 2008)

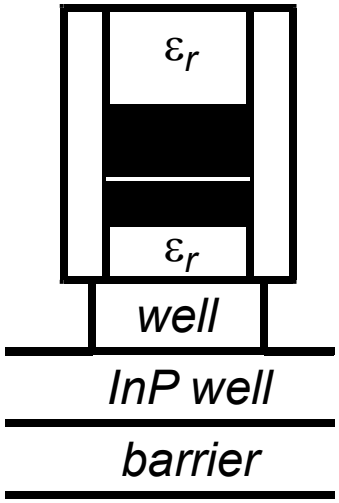
Al_2O_3 is more robust in processing.

→ initial process development

Process modules being developed for ZrO_2 .



Gate Definition: Challenges



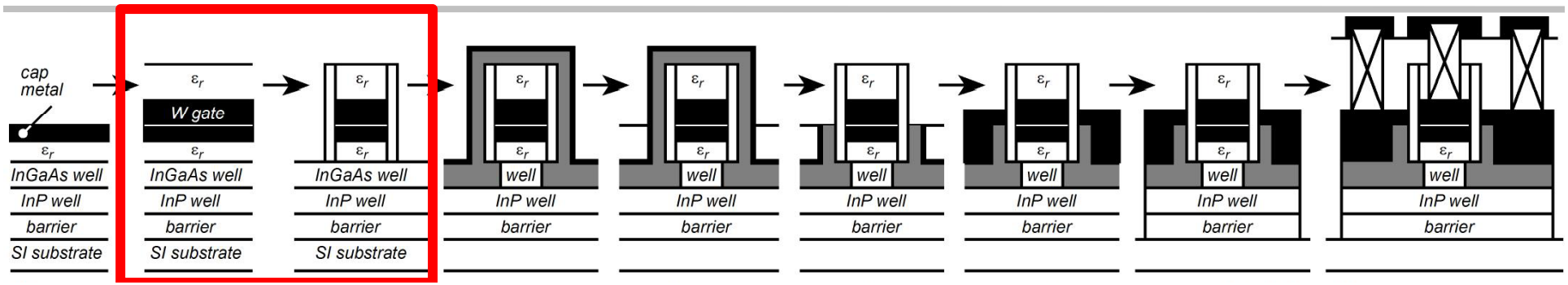
Must scale to 22 nm

Dielectric cap on gate for source/drain regrowth

Metal & Dielectric etch must stop in 5 nm channel

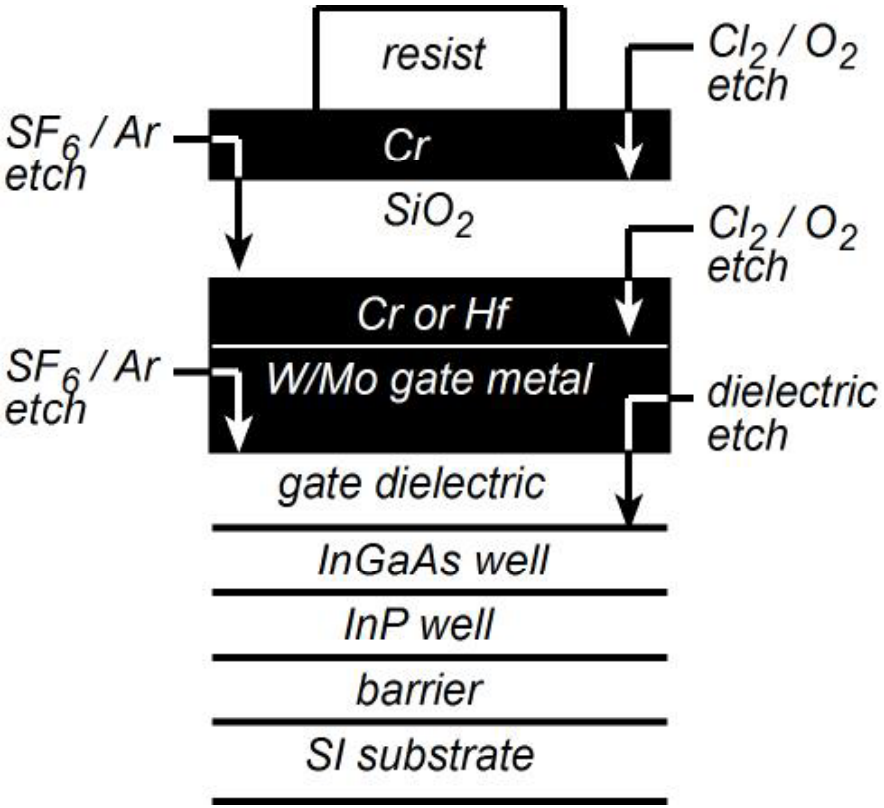
Semiconductor etch must not etch through 5 nm InP subchannel

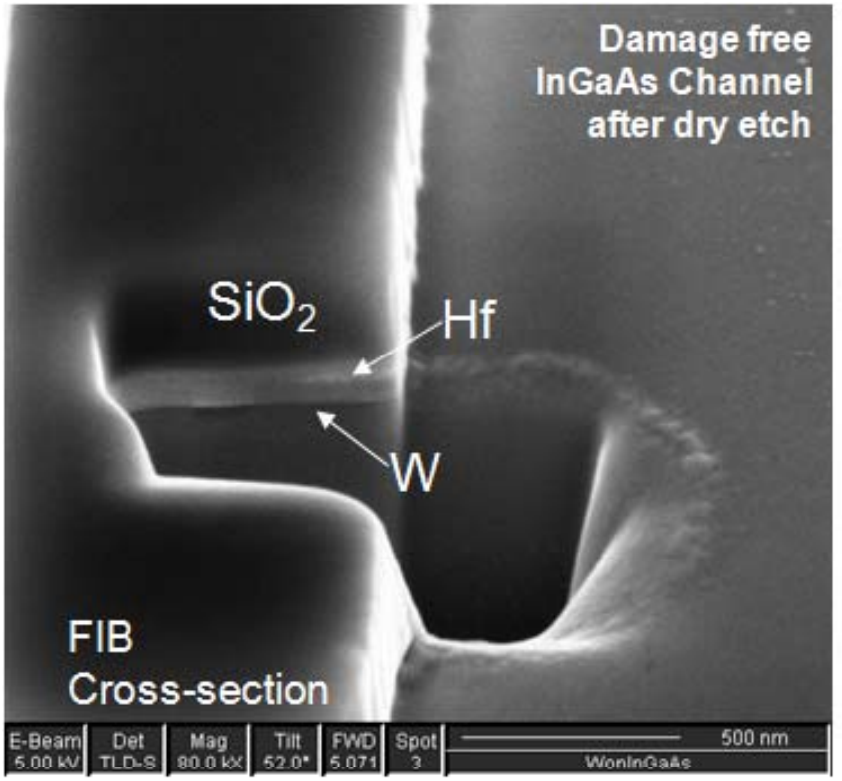
Process must leave surfaces ready for S/D regrowth

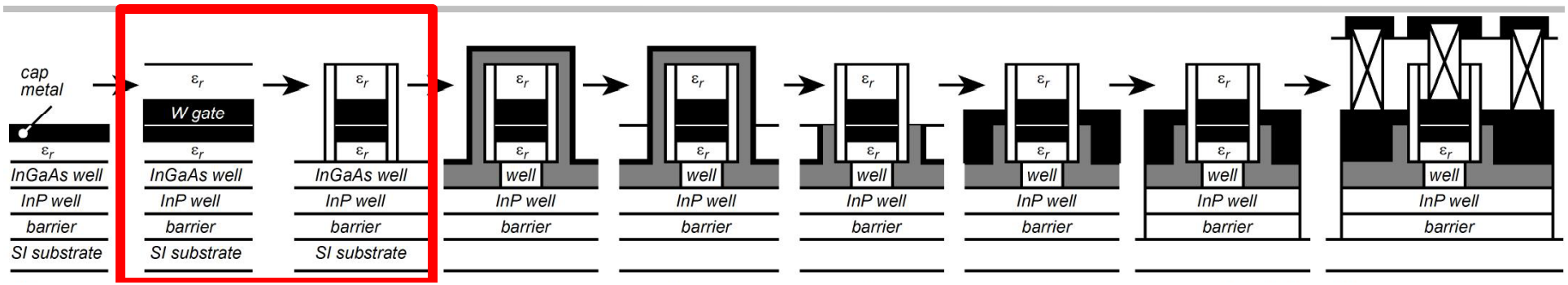


Gate Stack: Multiple Layers & Selective Etches

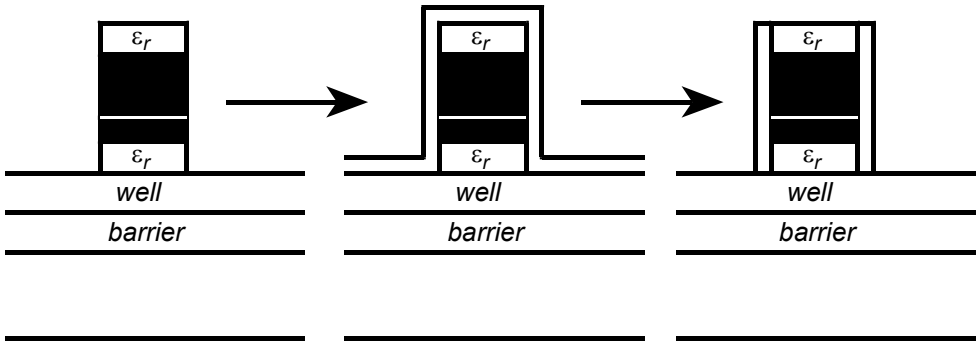
Key: stop etch before reaching dielectric, then gentle low-power etch to stop on dielectric

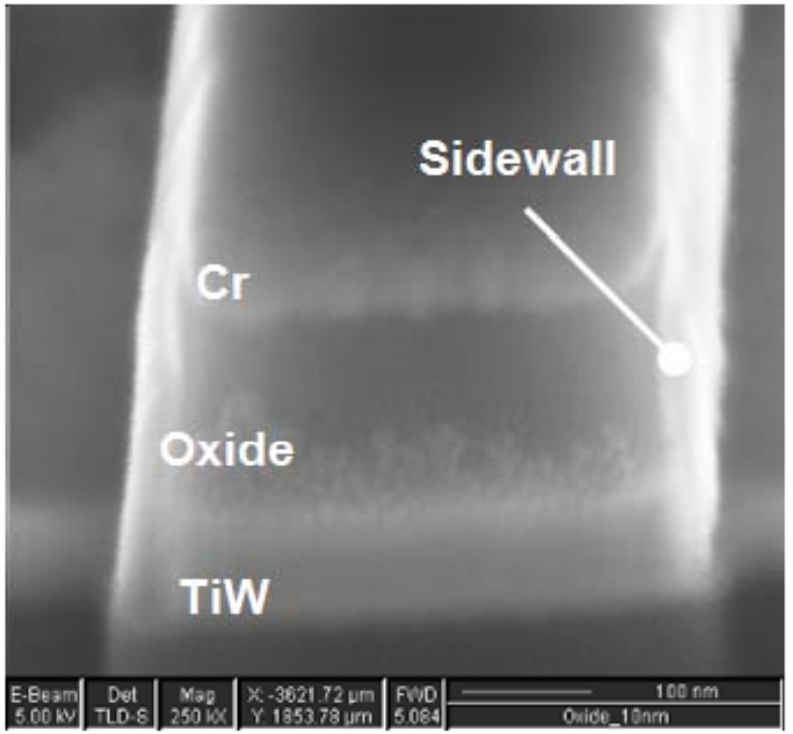






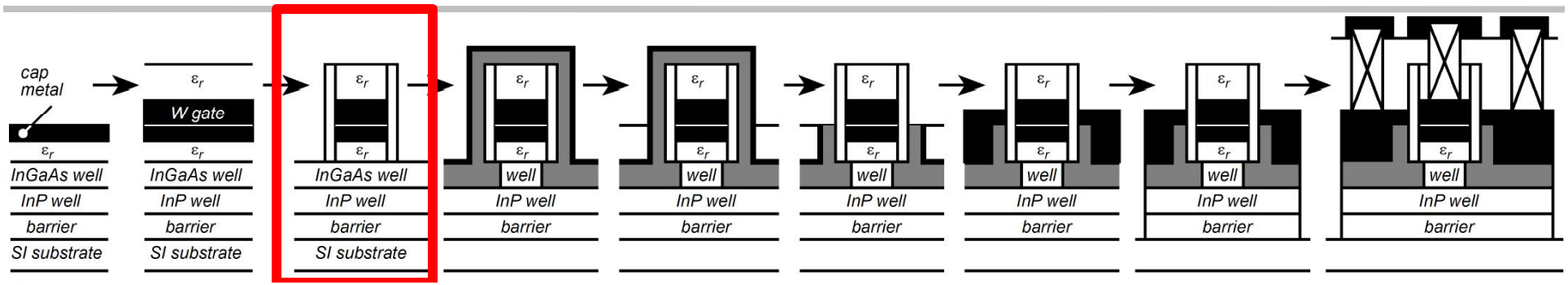
Sidewall Formation





PECVD SiN sidewall deposition, low power anisotropic RIE etch

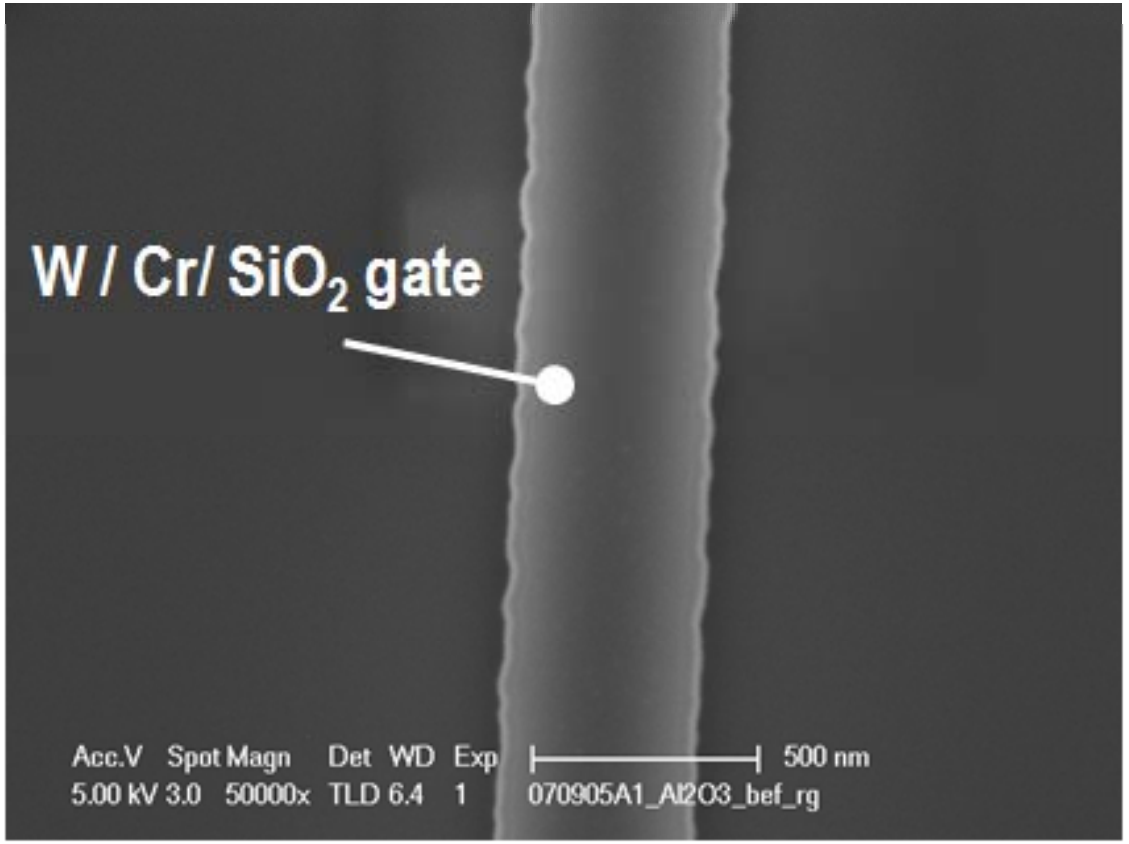
...sidewall etch must not damage the channel

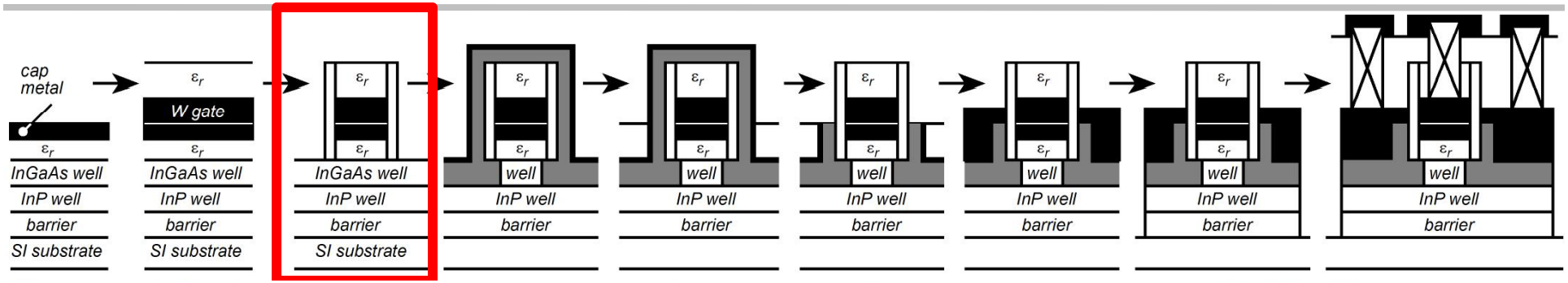


Clean, Undamaged Surface Before Regrowth

undamaged
InP subchannel

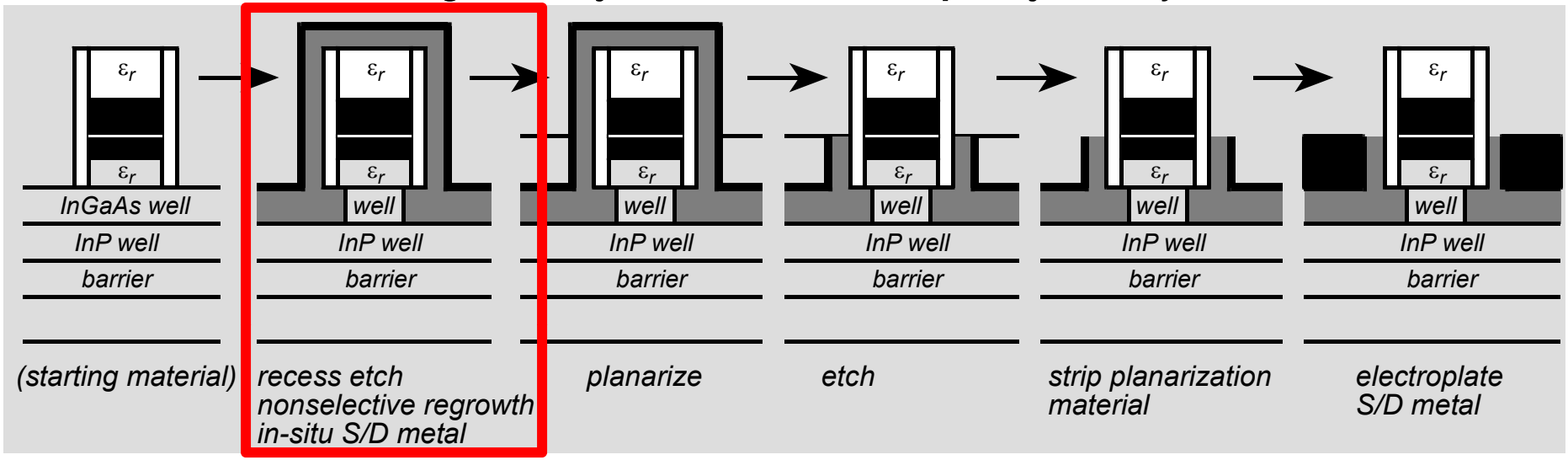
(after Al_2O_3 dielectric etch
& InGaAs recess etch)



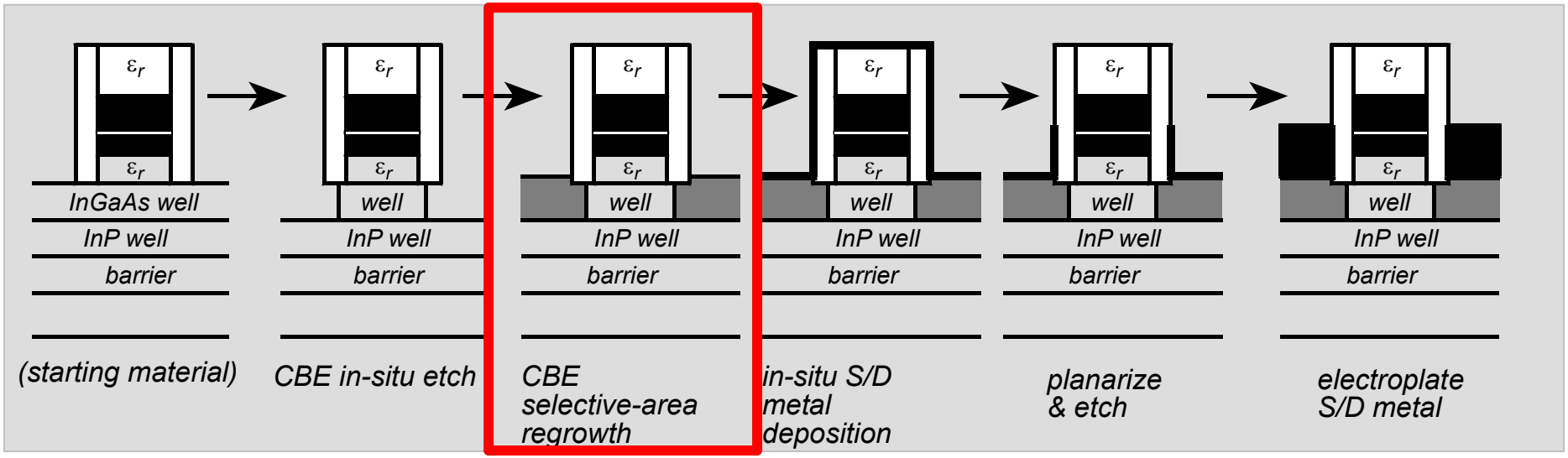


Two Source/Drain Regrowth Processes

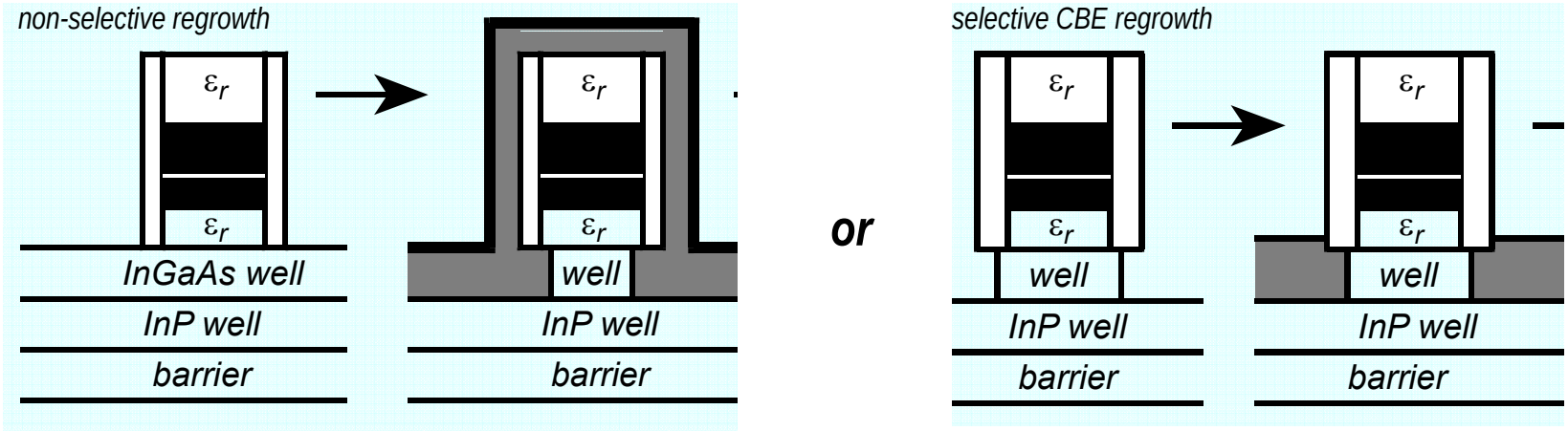
non-selective area S/D regrowth by Molecular Beam Epitaxy: *Wistey*



selective area S/D regrowth by Chemical Beam Epitaxy: *Palmstrøm / Arkun*



Recess Etch & Regrowth: Inter-Relationships

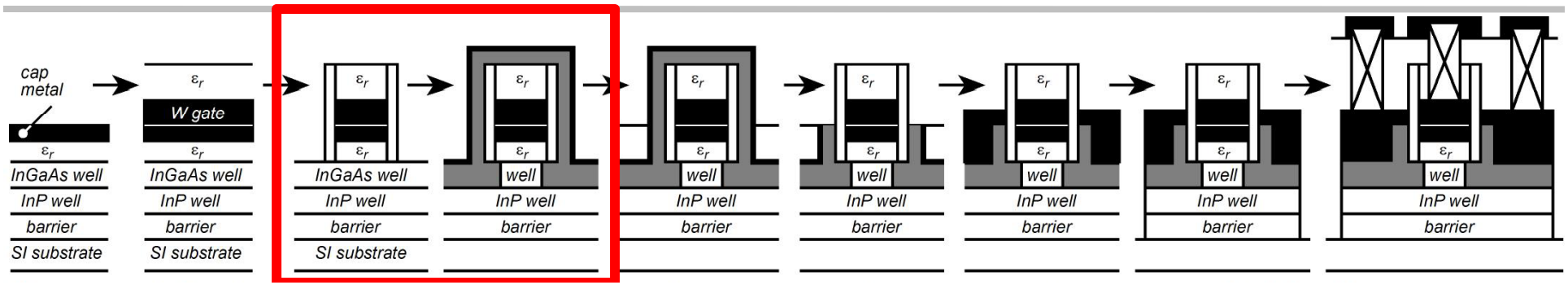


InGaAs/InP composite channel

permits selective InGaAs wet-etch, stopping on InP

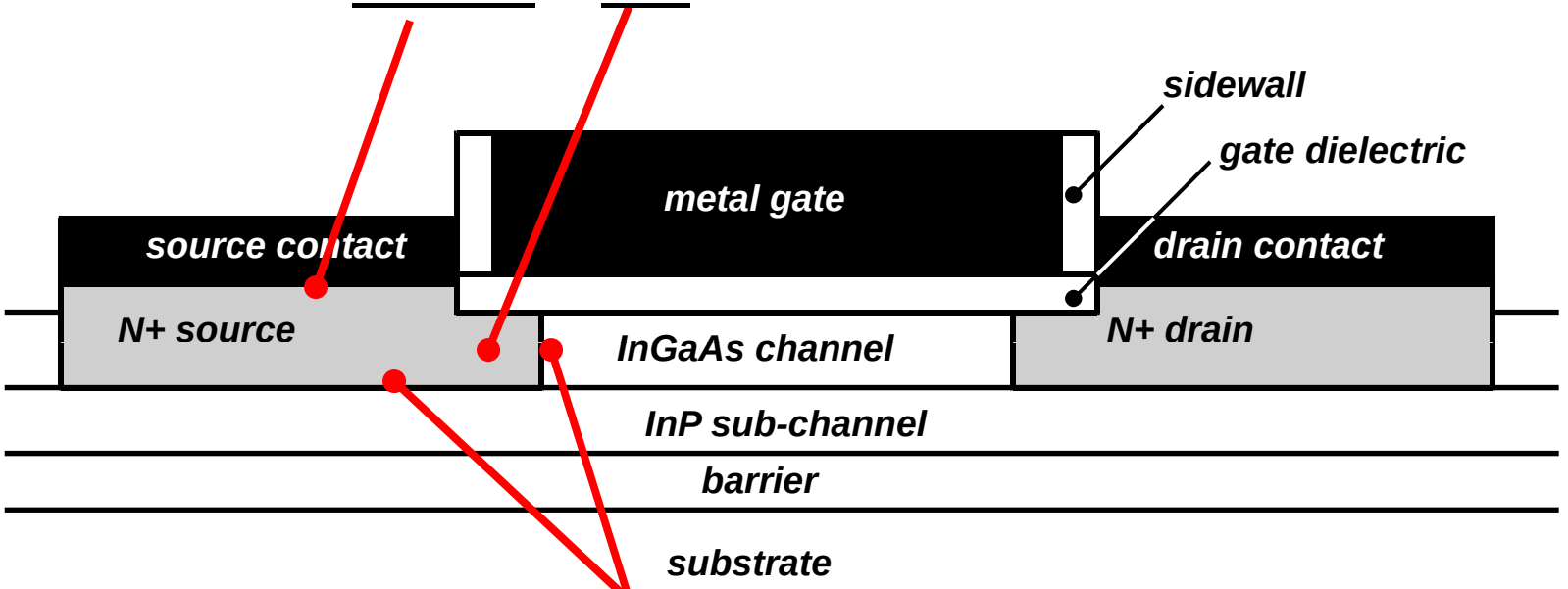
regrowth initiated on InP (desirable ?)

If regrowth can extend laterally under sidewall, sidewall can be thicker

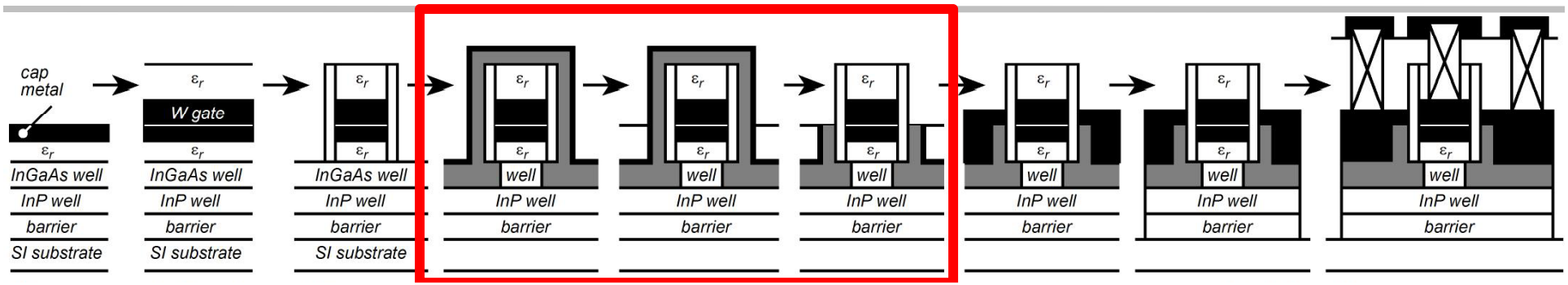


Regrowth interface resistance

In addition to the contact & link resistances



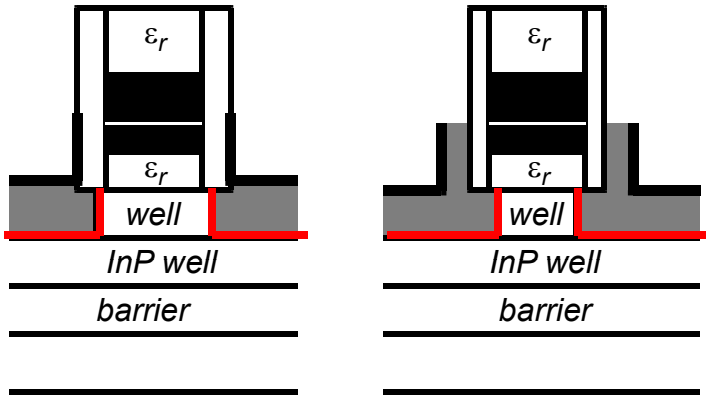
resistance at the regrowth interfaces is also of concern...

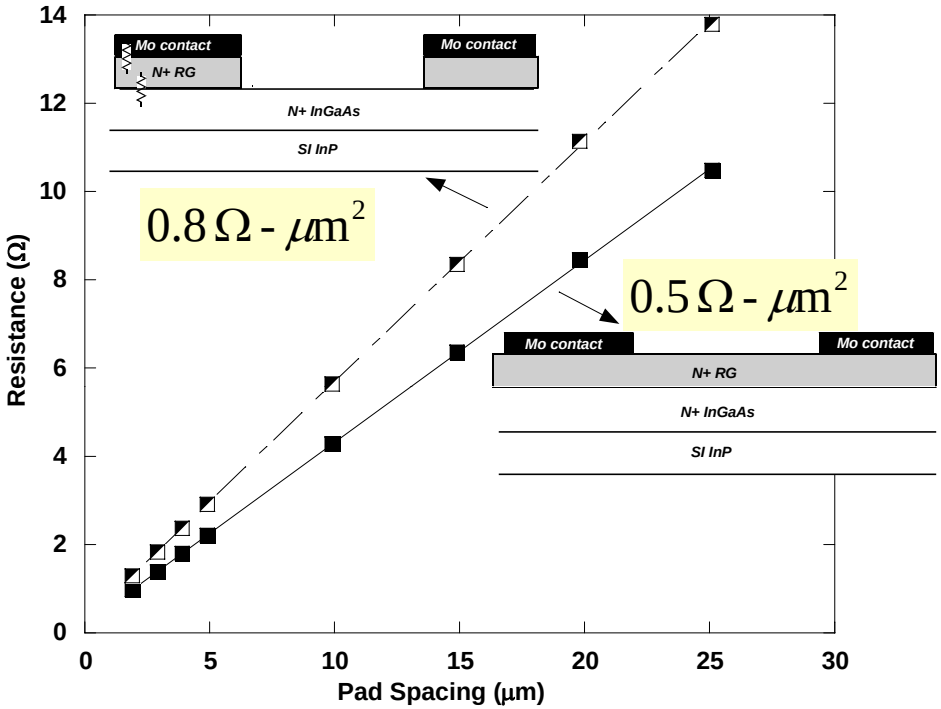


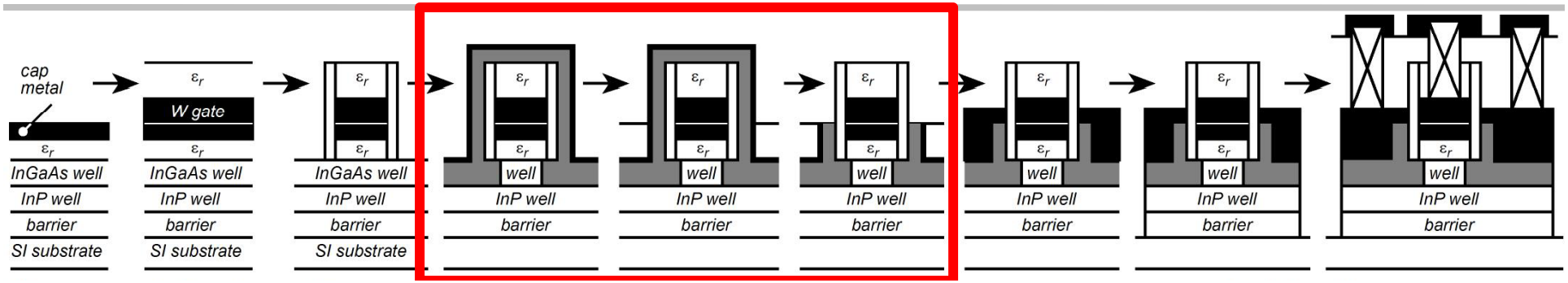
Contact & Regrowth Interface Resistance

Selective
-Arkun

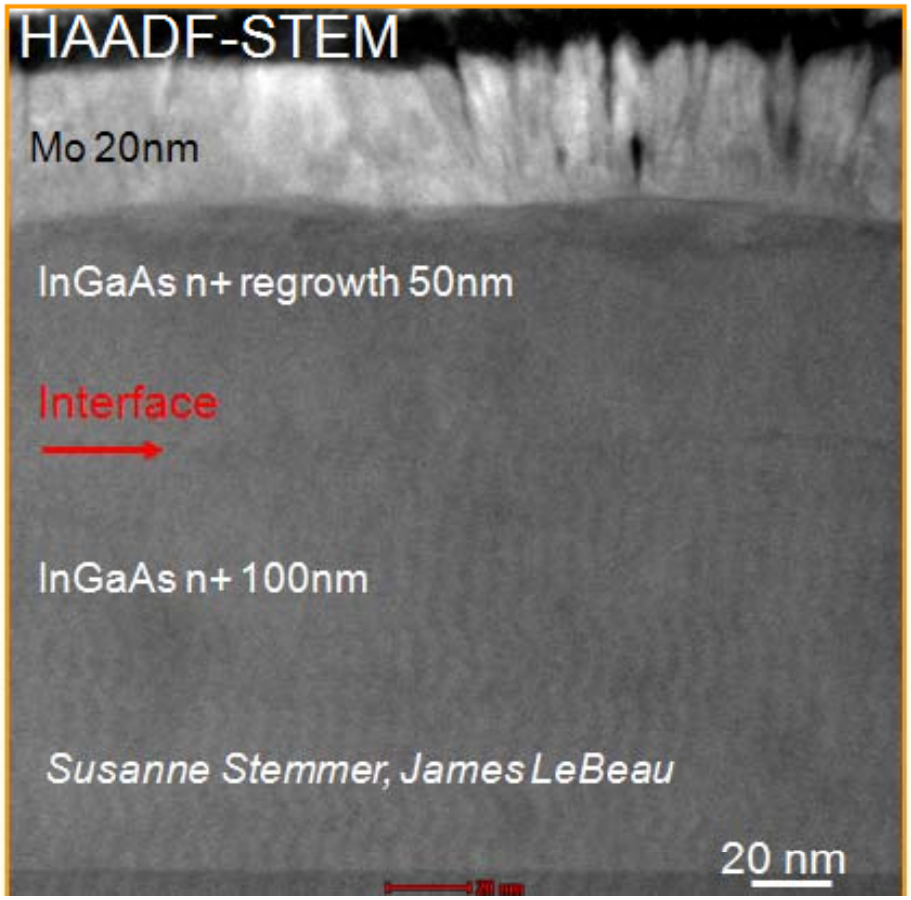
Nonselective
-Wistey

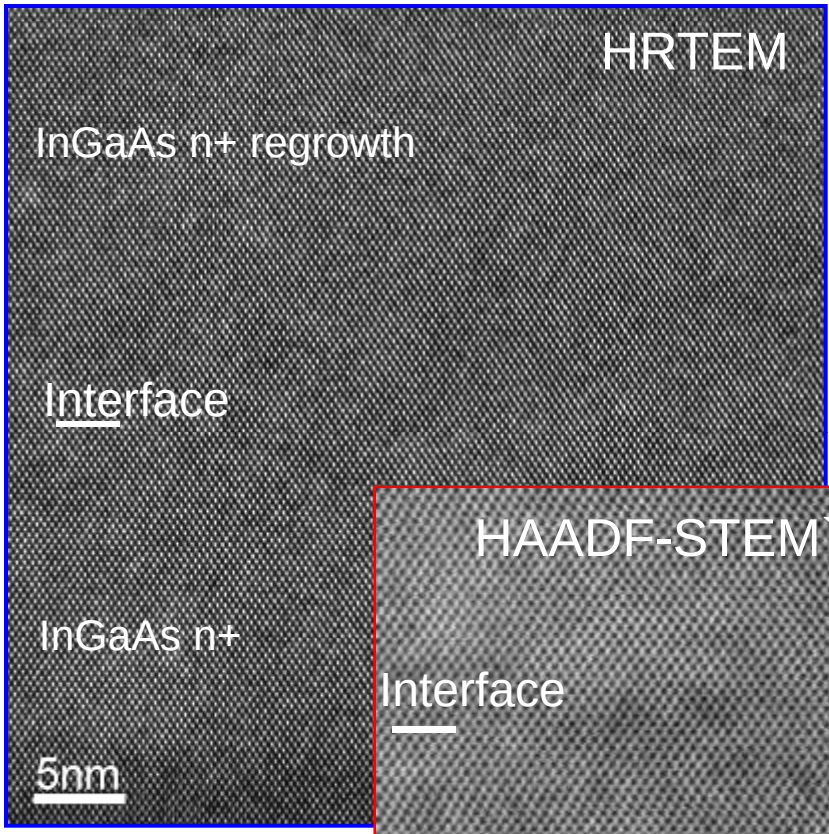


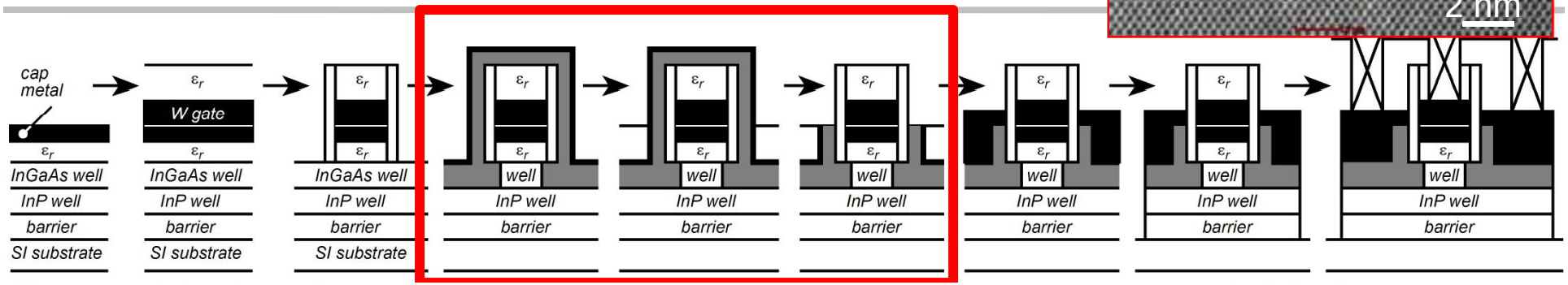




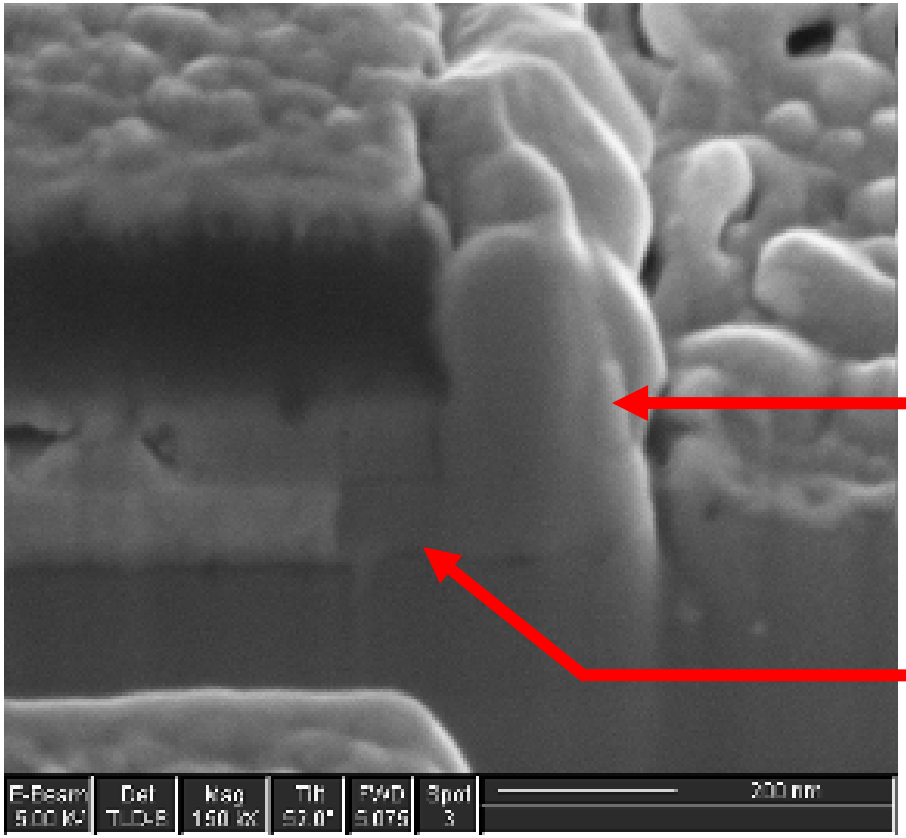
TEM of Regrowth: InGaAs on InGaAs (Mark Wistey)







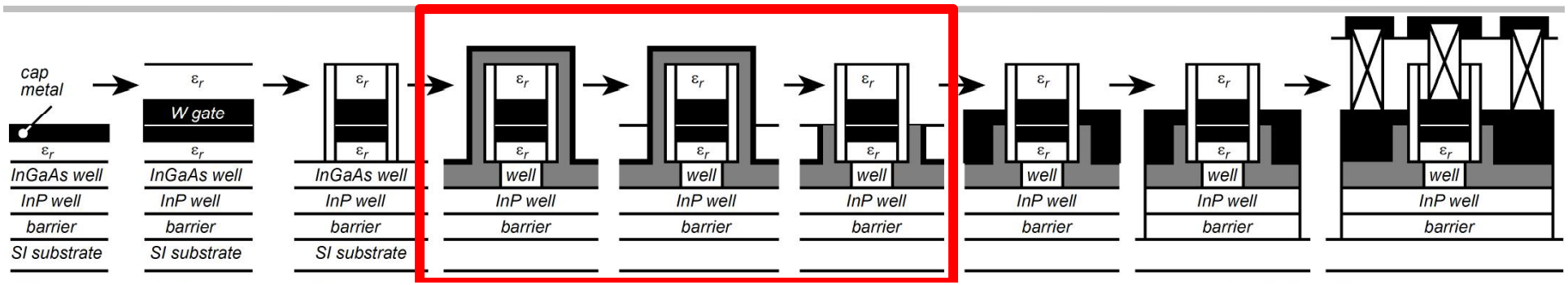
Images of MBE Regrowth (dummy sample)



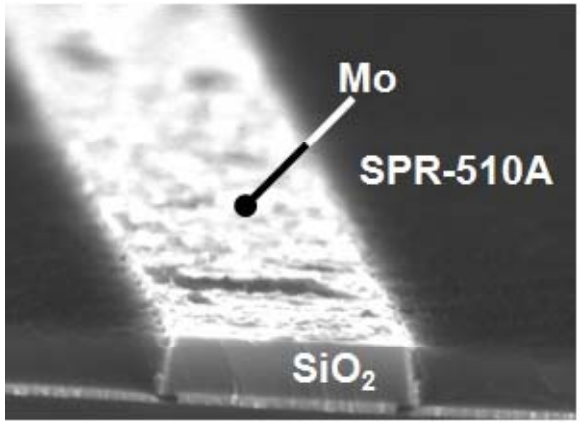
Regrowth process is still being de-bugged

growth on sidewall: bad !
to suppress, grow hotter

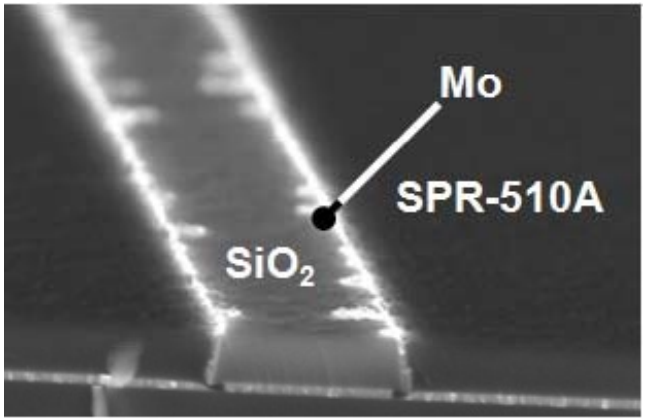
lateral regrowth under gate: good !



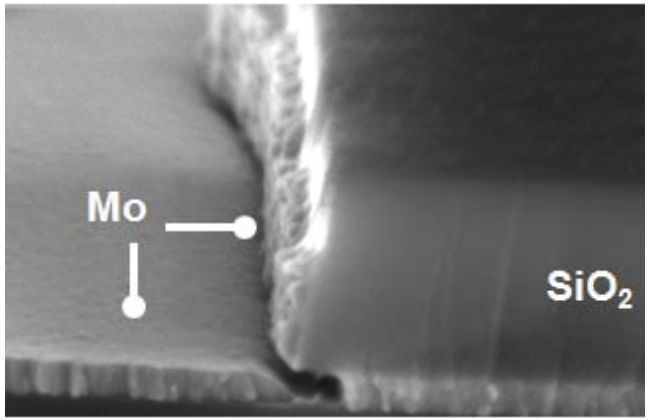
Planarization / Etch-Back Process



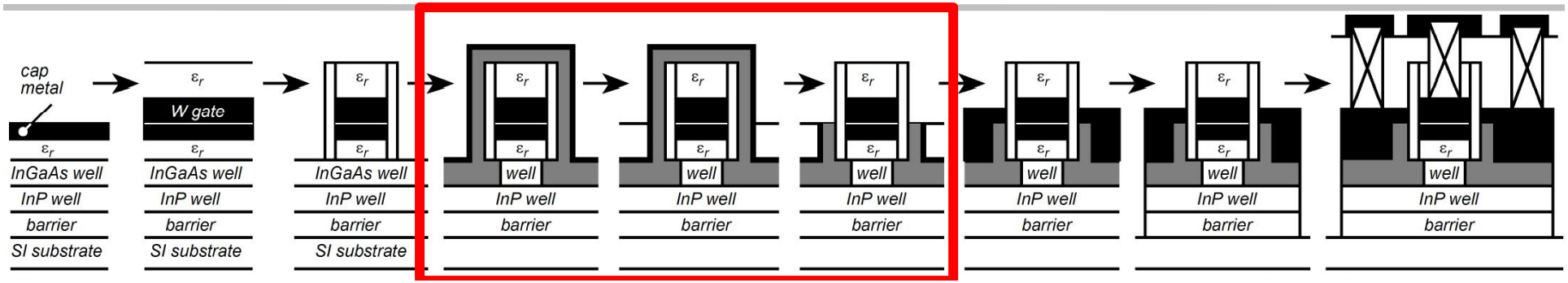
Ashed-back PR covers S/D contacts



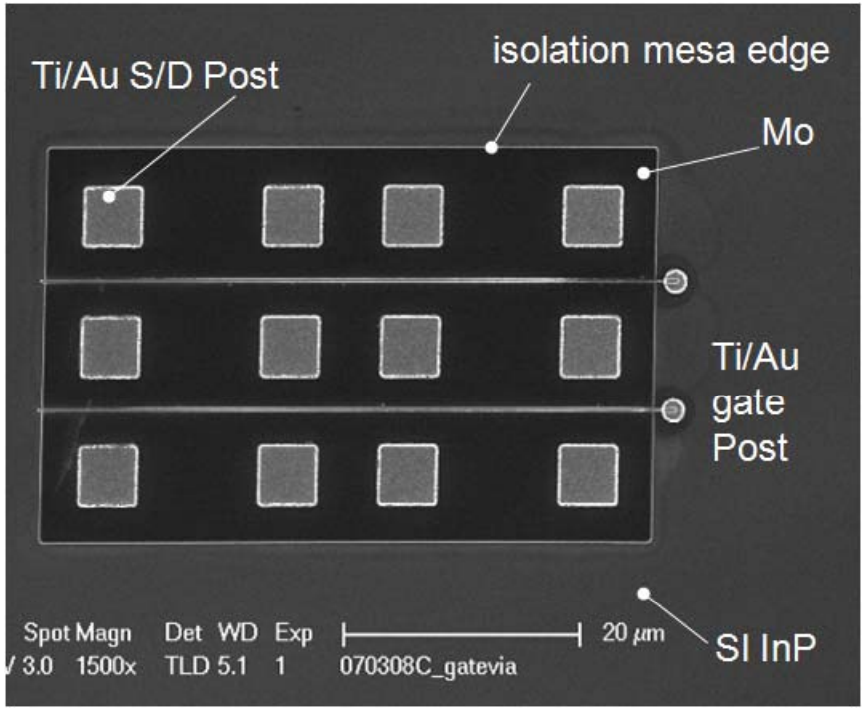
Mo etched in SF_6/Ar dry etch

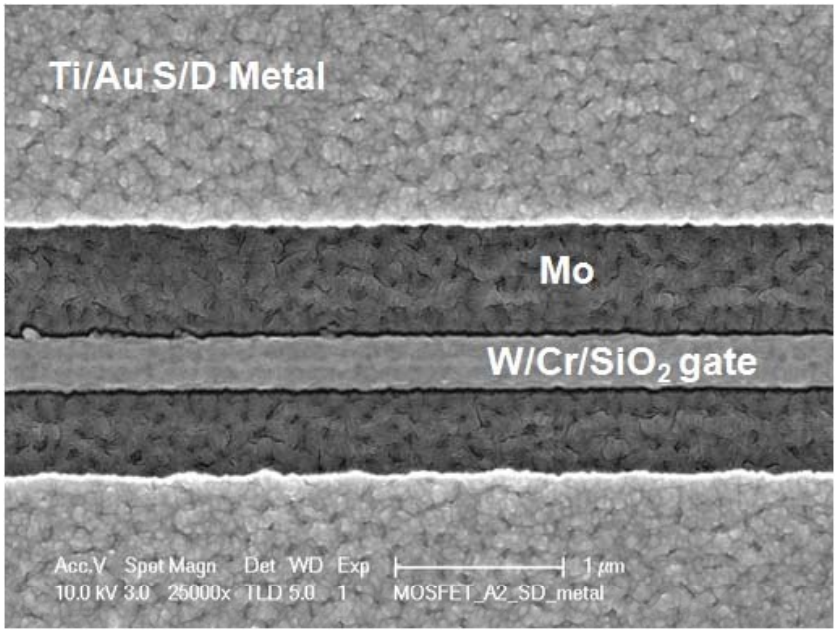


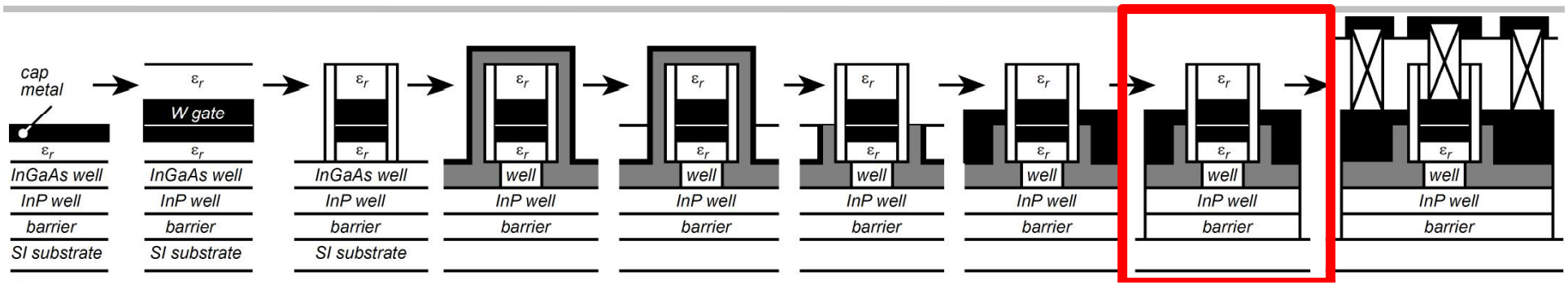
PR strip removes polymers.
Mo protects semiconductor
from descum plasma.



Images of Completed Device

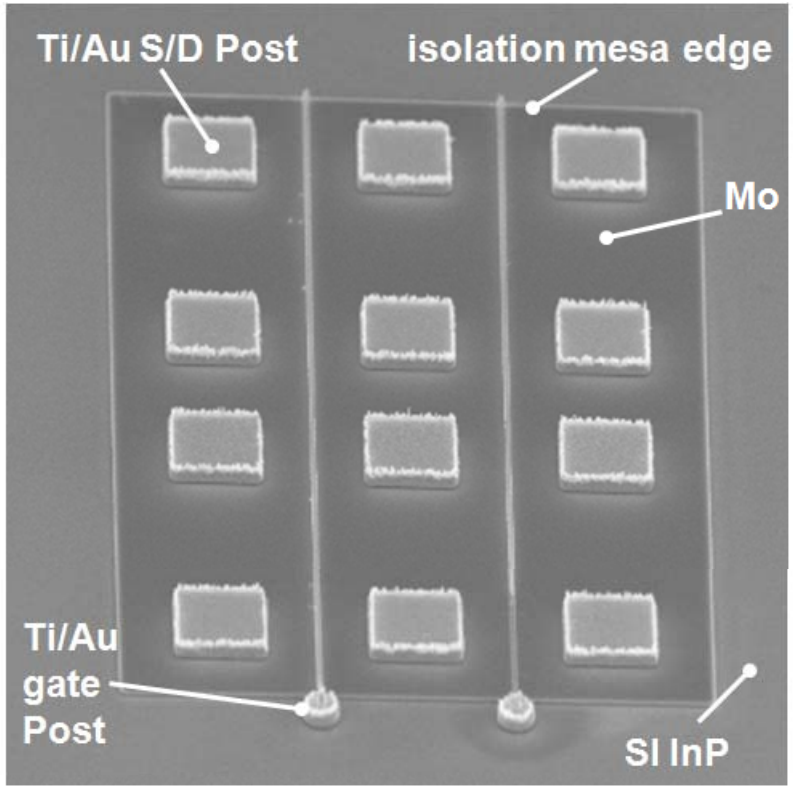






Results & Status

1st working devices: (ISCS submission)
MBE S/D regrowth
incomplete S/D growth under gate
→ high access resistance
→ low drive current (1 μA/μm !)



Cause of Problems
related to regrowth on InP subchannel
has impacted both MBE & CBE regrowth

...and is now resolved

New devices now in fabrication...stay tuned

InGaAs/InP Channel MOSFETs for VLSI

Low-m materials are beneficial only if EOT cannot scale below ~1/2 nm*

Devices cannot scale much below 22 nm Lg→ limits IC density

Little CV/I benefit in gate lengths below 22 nm Lg

Need device structure with very low access resistance
radical re-work of device structure & process flow

Gate dielectrics, III-V growth on Si: also under intensive development