# THz & nm Transistor Electronics: It's All About The Interfaces

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RUMORS of the death of Moore's law appear to be greatly exaggerated. Despite tremendous challenges, VLSI processes are still scaling rapidly. Processes at 45 nm lithographic half-pitch are in production. 22 nm VLSI now appears highly feasible. MOSFETs with 45 nm gate lengths have shown 450 GHz power-gain cutoff frequencies [1] ( $f_{max}$ ); smaller devices may well be faster. Facing such intense competitive pressure, transistors built from III-V semiconductors are also improving quickly. 340 GHz amplifiers [2] have been constructed from InGaAs field-effect transistors (HEMTs) having < 50 nm gate lengths and ~ 1 THz $f_{max}$. InGaAs/InP heterojunction bipolar transistors (HBTs) have reached 780 GHz $f_{max}$ [3] and 324 GHz HBT amplifiers have been demonstrated [4]. HBTs with ~2 THz $f_{max}$ appear feasible [3]. These demonstrated results and future trends are enabled by scaling; ***the key limits to such scaling are the attainable properties of semiconductor-metal and semiconductor-dielectric interfaces***.

Electron device bandwidths are determined by depletion layer transit times [5] and capacitances, and by bulk and contact resistivities; currents are limited by bulk, contact, and equivalent-space-charge resistances and by device heating. Device bandwidths are increased by reducing junction dimensions (lithographic scaling), reducing layer thicknesses (epitaxial scaling) and by reducing Ohmic contact resistivities and thermal resistivities.

First consider scaling of a PIN photodiode. To double bandwidth, we must reduce all capacitances and transit times 2:1 while maintaining constant the diode resistance, operating current, and voltage. To reduce carrier transit time 2:1, we reduce the depletion layer thickness 2:1. We have doubled the capacitance per unit area, hence to reduce the capacitance 2:1, we must now reduce the junction area 4:1. We seek to maintain constant contact resistance in the presence of 4:1 reduced junction area, and consequently must reduce the contact resistivity 4:1. The same current must be carried through a junction of 4:1 smaller area; thermal resistance per unit junction area must be reduced 4:1.

The design and scaling laws for bipolar transistors differs only trivially from the above [3]. Each doubling in device bandwidth demands a 2:1 thinning of epitaxial layers, a 4:1 reduction in junction widths, a 4:1 increase in current densities, and a 4:1 reduction in contact resistivities. In highly scaled devices, contact resistivities ***dominate*** over bulk resistivities. To attain 2-3 THz $f_{max}$ at the 32 nm scaling generation, we must attain ~1 $\Omega-\mu m^2$ resistivity contacts, and these must be stable at ~ 75 mA/ $\mu m^2$ current density.

Field-effect-transistor scaling follows similar laws. In the constant-voltage, saturated-velocity limit, each doubling of device bandwidth is obtained through a 2:1 reduction in gate length, gate width, and gate insulator equivalent thickness. Source and drain contact Ohmic resistivities must be reduced 4:1. The channel current per unit gate width, the transconductance per unit gate width, and the 2-DEG channel charge density are all doubled.

In addition to the requirement, common to bipolar transistor and PN diode scaling, of progressively improved contact resistivities, FETs also demand progressive improvements in gate insulators, with relatively constant leakage (tunneling) current densities being demanded of dielectrics having progressively increasing capacitance density. The key materials challenges, then, for future THz electron devices lie at the semiconductor surfaces. We desire semiconductor-metal interfaces with extremely low (~0.1-1 $\Omega-\mu m^2$) contact resistivities. We desire low-leakage semiconductor-dielectric interfaces with extremely high (~30-300 $fF/\mu m^2$) capacitance densities.

Many groups are now exploring semiconductor interfaces to high-K dielectrics; we have been exploring low-resistivity contacts. To date, we have attained <1 $\Omega-\mu m^2$ resistivity in contacts to N-InGaAs through either *in-situ* deposition of Mo contact metal during semiconductor MBE growth [6] or through *ex-situ* deposition of refractory TiW contacts after surface cleaning and passivation by soaking in concentrated ammonia [7]. We are now exploring similar processes for contacts to P-type materials. We have investigated ErAs/N-InGaAs semi-metal / semiconductor interfaces, anticipating that the contamination-free and defect-free coherent interface would show extremely low resistivity. Such interfaces show a disappointing 1.5 $\Omega-\mu m^2$ resistivity, possibly due to the low density of states associated with a semi-metal. Might an *in-situ* grown, coherent and lattice-matched metal-semiconductor interface provide lower resistivity ?

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