A 150 GHz Amplifier With 8 dB Gain and +6 dBm $P_{\rm sat}$ in Digital 65 nm CMOS Using Dummy-Prefilled Microstrip Lines

Munkyo Seo, *Member, IEEE*, Basanth Jagannathan, John Pekarik, *Member, IEEE*, and Mark J. W. Rodwell, *Fellow, IEEE*

***Abstract*—A 150 GHz amplifier in digital 65 nm CMOS process is presented. Matching loss is reduced and bandwidth extended by simplistic topology: no dc-block capacitor, shunt-only tuning and radial stubs for ac ground. Dummy-prefilled microstrip lines, with explicit yet efficient dummy modeling, are used as a compact, density-rule compliant matching element. Transistor layout with parallel gate feed yields 5.7 dB of MSG at 150 GHz. Measurement shows the amplifier exhibits 8.2 dB of gain, 6.3 dBm of $P_{\rm sat}$, 1.5 dBm of $P_{\rm 1dB}$ and 27 GHz of 3 dB bandwidth, while consuming 25.5 mW at 1.1 V. The dummy-prefilled microstrip line exhibits $Q_{TL} \cong 12$ up to 200 GHz.**

***Index Terms*—150 GHz amplifier, 65 nm, amplifiers, CMOS millimeter-wave integrated circuits, dummy modeling, matching loss, metal filling, millimeter-wave integrated circuits, MMICs, pattern density rules, silicon, transmission lines.**

I. Introduction

ADVANCED CMOS or SiGe technologies have been demonstrating millimeter-wave (mm-wave) circuits beyond 100 GHz [1]–[8]. Single-chip transceivers are demonstrated at 170 GHz [1] and 160 GHz [3] in 0.13 μm SiGe technology. In a 65 nm CMOS process, receivers up to 140 GHz [2], [9], [10], and amplifiers up to 150 GHz [5], [8], [11], [12] have been reported. Amplifiers in 90 nm CMOS processes are demonstrated up to W-band [4], [7], [13]–[15].

Radio applications beyond 100 GHz, such as high-rate communication links [16], [17], imaging systems [18], [19], and chemical sensors, will benefit from the high yield, the high levels of integration, and the co-integration with analog or digital signal processing blocks available in silicon technologies. Millimeter-wave systems in CMOS technologies are of particular interest, since they can take advantage of the continued device scaling.

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M. Seo was with the Department of Electrical and Computer Engineering, University of California at Santa Barbara. He is now with Teledyne Scientific and Imaging, 1049 Camino Dos Rios, Thousand Oaks, CA 91360 USA (e-mail: mseo@teledyne-si.com).

B. Jagannathan is with IBM SRDC, Hopewell Junction, NY 12533 USA.

J. Pekarik is with ST Microelectronics, Crolles Cedex, France.

M. Rodwell is with the Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA 93106-9560 USA.

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The design of mm-wave CMOS circuits are however challenging, especially beyond 100 GHz. First, available transistor gain is relatively low, since the frequency of operation is a significant fraction of $f_{\max}$. Second, passive elements have low quality factors at these high frequencies, increasing matching losses. Third, strict metal density rules generate metal dummies and holes. They alter passive element characteristics, thus interfere with the design and modeling of passive devices [1], [2], [20]–[23].

This paper presents design considerations and experimental characterization for a 150 GHz amplifier in a digital 65 nm CMOS technology [8]. A simple amplifier topology is chosen to reduce matching loss and modeling uncertainties. Dummy-prefilled microstrip line is proposed and used for compact matching networks, while meeting metal density rules.

In Section II, FET layout is discussed to minimize extrinsic gate resistance. Section III discusses transmission line based matching networks. In Section IV, an efficient approach is proposed to model the effect of dummy fillers on microstrip lines. Section V presents the amplifier design. Finally, S-parameter and power measurement results are presented in Section VI, including characteristics of dummy-prefilled microstrip lines up to 200 GHz.

II. Transistor Layout

Transistor layout is important in mm-wave circuit design to preserve intrinsic device performance, while minimizing parasitics arising from external metallizations and interconnects. In this work, the unit finger width is chosen 1 μm, from considerations of gate resistance and overall FET aspect ratio. Given total channel width, using smaller fingers can reduce gate resistance, but top-level wiring may be difficulty if the FET becomes excessively tall. Double-sided gate contacts are chosen for lower poly resistance: two rows of minimum-spaced contacts were placed on both ends of fingers. A Metal-1 ring ties both sides at the top and bottom of contact arrays. Substrate contacts are placed as close to the intrinsic transistor as possible.

Fig. 1 illustrates two wiring styles to connect multiple fingers. In series gate feed (SGF), the overall wiring is perpendicular to gate fingers, and the top-level interconnect can be made on top or bottom (or both) of the finger array. In parallel gate feed (PGF), the external feed is on one side of finger array (typically source side to avoid gate-drain capacitance), connecting

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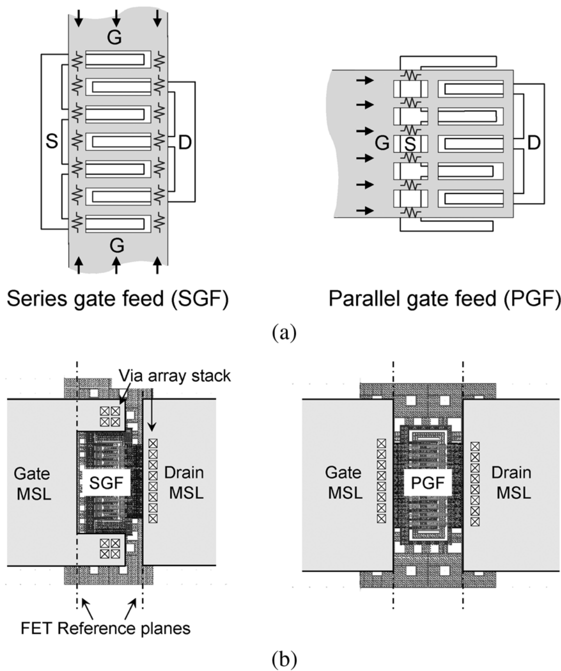

Fig. 1. Two representative multi-finger wiring styles: (a) Series gate feed (SGF) and parallel gate feed (PGF). Arrows represent gate current flow. (b) connection to top-level microstrip lines.

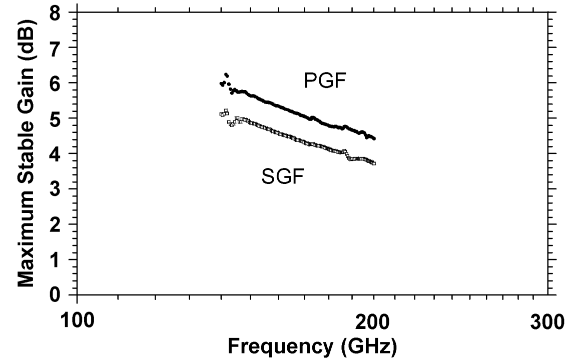

Fig. 2. Measured MSG of 65 nm FETs in two different wiring styles: SGF and PGF ($W_G = 10 \times 1\ \mu$m) at $V_{GS} = V_{DS} = 0.65$ V.

all fingers in parallel. PGF wiring, due to its asymmetric current flow with respect to finger ends, does not fully take advantage of double-sided contacts, resulting in higher poly resistance than SGF (top and bottom fingers, however, receive bridging currents from a Metal-1 ring, thus fully exploiting double contacts). Another difference between SGF and PGF, especially pronounced for large FETs, lies in how their external gate resistance $R_{g,\rm ext}$ scales with the number of fingers N: $R_{g,\rm ext}$ of a SGF and PGF FET scales as N and $1/N$, respectively, to first order. If *normalized to a single finger*, $R_{g,\rm ext}$ of SGF increases as N^2, whereas PGF's $R_{g,\rm ext}$ remains constant. First-order analysis shows that SGF's $R_{g,\rm ext}$ starts to limit FET gain for $N > 25$, when Mason's U reduces by more than 1 dB.

In this work, all FETs are embedded in a microstrip line (MSL) environment as a common-source (CS) configuration: the source terminal is directly connected to MSL ground plane composed of Metal-1 and Metal-2. Gate and drain nodes are tapered to the MSL signal line in top metal layer through a stack of via arrays. Sufficiently many vias are used at all levels to ensure their relative contribution to extrinsic gate and drain resistances are small. Specifically, gate and drain via stacks are designed for no more than 5 Ω of series resistance *per unit finger*. See Section V-F for a summary of 65-nm digital CMOS process used in this work.

S-parameters of SGF and PGF FETs were measured in 140–220 GHz band for two different gate widths: $W_G = 10\ \mu$m and 20 μm. On-wafer Thru-Reflect-Line (TRL) calibration was performed to define reference planes at the edge of top metal layer (see Fig. 1(b) and Section V-A3). FETs were conditionally stable in 140–220 GHz, and the measured MSG followed 10 dB/dec slope, as shown in Fig. 2. At 150 GHz, the PGF FET exhibits 5.7 dB of MSG for both $W_G = 10\ \mu$m and 20 μm, while the SGF has 0.8 dB and 0.4 dB less gain. SGF's $\mathrm{imag}(y_{12})$ is found 20% and 10% larger than PGF's, for $W_G = 10\ \mu$m and 20 μm, respectively. Therefore, the SGF's reduced MSG is attributed to its top-level wiring structure where gate and drain via stacks are closer than PGF's, picking up additional gate-drain capacitance (recall $\mathrm{MSG} = |y_{21}|/|y_{12}|$).

Measured U was rather noisy due to its inherent sensitivity to measurement or calibration errors (especially to resistive ones). For $W_G = 10\ \mu$m, both PGF and SGF FETs exhibit $U \sim 6$ dB at 150 GHz. For $W_G = 20\ \mu$m, $U \sim 7.5$ dB and 6 dB for the PGF and SGF FET, respectively. The measured current gain cut-off frequency, f_T, was 180 GHz. Measured U did not follow a 20 dB/dec curve, but an attempted extrapolation would give 280–320 GHz of $f_{\max}$.

III. On-Chip Microstrip Line Matching Network

A. Lumped Elements versus Transmission Lines

Impedance matching based on lumped elements has been recently demonstrated beyond 100 GHz [1]–[3]. While enabling compact IC layout, this approach requires accurate modeling of on-chip capacitors (MIM or metal finger), inductors and transformers, including their resonance frequency as well as resistive losses. On-chip transmission lines, such as co-planar waveguide lines (CPW) [4]–[6], [12], [19] or microstrip lines (MSL) [7], [8], [14], [15] can be used for impedance matching with more predictable parameters; a single section of transmission line of any length is fully modeled by four real numbers: $RLGC$ parameters or (Z_0, γ) pair. To model line discontinuities, such as bend, cross or T-junction, either compact CAD models can be used or selective 2.5D electromagnetic (EM) simulations can be run. The main drawback of transmission-line approaches is the relatively large physical size, on the order of $\sim \lambda$. Area penalty is, however, proportionately smaller at higher frequencies: at 150 GHz, one quarter-wavelength $((1/4)\lambda)$ in typical CMOS environment with $\epsilon_{\rm eff} = 4$ is $\sim 250\ \mu$m, resulting in $\times 2.5$ area reduction over similar 60 GHz designs where $(1/4)\lambda \cong 625\ \mu$m.

B. Co-Planar Waveguides versus Microstrip Lines

CPW lines provide two degrees of design freedom (Fig. 3): signal strip width (W) and signal-ground spacing (S). This is in contrast to an on-chip MSL where W can be still freely chosen

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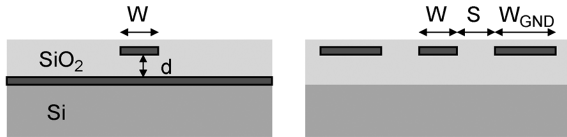

Fig. 3. On-chip microstrip line (left) and co-planar waveguide (right).

(under the design rule constraints), but the total dielectric thickness d is limited to 4–7 μm in typical CMOS back-end processes. Therefore, high impedance (Z_0) MSL lines are in general lossy, due to the small required W. CPW line structure, on the other hand, can provide more control over the conductor loss by independently choosing W and S. CPW lines, however, may be subject to substrate losses when the signal-ground spacing is larger than d, the dielectric thickness, due to the electromagnetic fields penetrating into the substrate. In an MSL, its ground plane prevents field penetration into the substrate, reducing substrate loss. In this work, the design of 150 GHz amplifier is based on MSLs for the following reasons.

First, MSLs enable more compact T-junctions than CPW lines. This not only eases design, but also helps to eliminate matching loss, as will be discussed later. For example, in a CPW with $W = 10$ μm, $S = 10$ μm and $W_{\rm GND} = 20$ μm, a T-junction will need $W + 2S + 2W_{\rm GND} = 70$ μm of minimum signal run to accommodate a shunt-tuning line, introducing $\sim$25 degree of phase shift at 150 GHz. With this considerable electrical length (and with associated ground straps), modeling accuracy will be important in CPW-based T-junctions. In an MSL, a T-junction can be as narrow as W, although extension may be desirable to reduce cross-talk between adjacent lines.

Second, an MSL provides a shorter grounding path to FETs than CPW lines regardless of substrate thickness, since typically, lowest metal layers (i.e., Metal-1 or Metal-2) constitute an MSL ground plane. In CPW, access from FETs to the ground strip is only through a stack of vias. As the frequency of operation approaches $f_{\max}$, where the available device gain is already low, the impedance of such via stack may degrade circuit performance, especially with thick substrates.

Either MSLs or CPWs, most on-chip transmission line structures are subject to the effects of metal filling and cheesing, as these will change the electrical properties of the dielectric medium and conductor strips or planes. More detailed discussion will follow in Section IV, where an efficient procedure is proposed for dummy modeling in MSL environment.

IV. Dummy-Prefilled Microstrip Lines

In most nanoscale CMOS processes, layouts are subject to strict *pattern density rules* to ensure density of layout patterns stays within a certain range for each metal layer. Density requirements are typically enforced as part of post-layout processing, upon either the global layout or local windows within a sliding checking-box (e.g., 100–200 μm) [24]. If the measured densities are too low (or too high), metal fillers (or holes) with predefined shapes are automatically generated, until no density violation is detected. Full compliance to such density requirements reduces variations in interlevel dielectric thickness [25], thus enhancing process yields and product reliability.

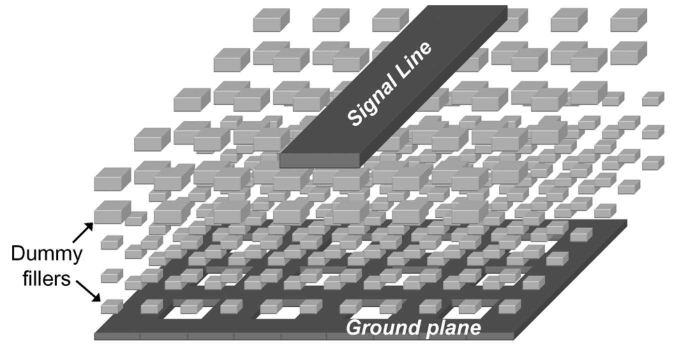

Fig. 4. Microstrip line in fine-line CMOS process after dummy filling and metal cheesing for pattern density control.

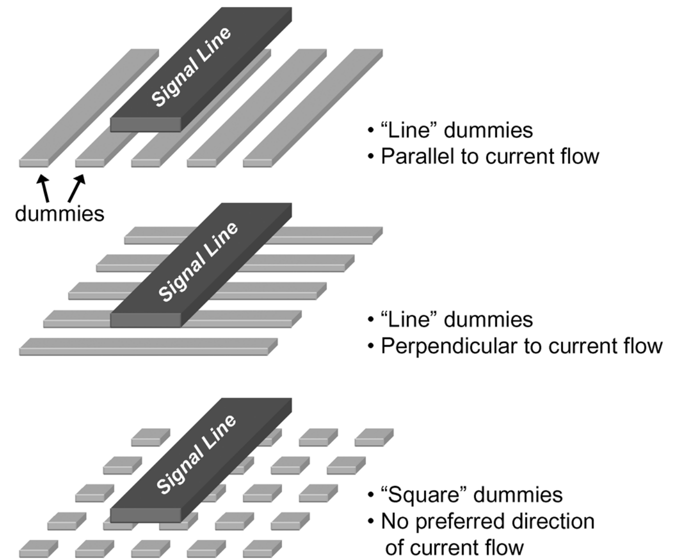

Fig. 5. Possible shapes of dummy prefillers.

Typically, local pattern density requirement could be as high as 30–35%, which can significantly alter MSL characteristics by increasing line capacitance. For example, an MSL will look like Fig. 4, after dummy filling and hole generation (called *cheesing*). Note that solid metal planes can no longer be used, as they have 100% local pattern density.

A. Dummy-Prefilling

For the sake of modeling accuracy, it is highly desirable to *prefill* and *precheese* all metal layers around an MSL, prior to post-layout processing. Using a sufficiently dense array of small fillers and holes can prevent further density enforcement (which is beyond circuit designer's control), thus guaranteeing design repeatability. Such dummy prefillers can be an array of lines or squares (Fig. 5). In practice, either line dummies perpendicular to signal line (Fig. 5, middle) or square fillers (Fig. 5, bottom) are of interest. Long dummies parallel to the signal line will induce significant image currents, thus decreasing line inductance and increasing line loss. Unlike line dummies, square-type prefillers do not prefer any particular direction of signal current flow. Signal lines thus can be independently routed with no regard to the orientation of adjacent fillers. In addition, square

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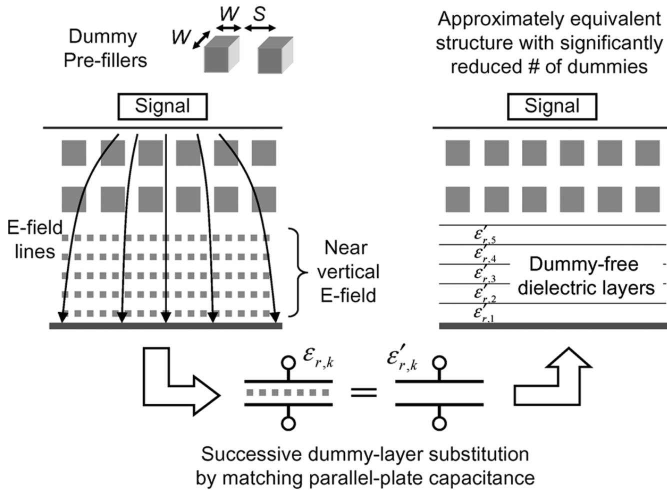

Fig. 6. Dummy reduction by equivalent layer substitution for efficient EM analysis.

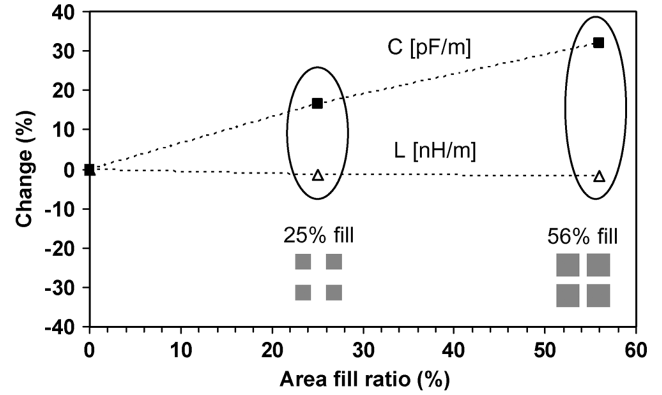

Fig. 7. Transmission line inductance and capacitance as a function of area filling ratios.

dummies allow straightforward prefilling under MSL discontinuities (e.g., bends) along with consistent EM environment, which would be difficult with line-shaped fillers. Note that perpendicular line dummies (Fig. 5, middle) have been used to prefill under an on-chip dipole antenna [1], and more popularly, as part of slow-wave transmission line structures [5], [26], [27], [44].

In this work, square prefillers are used for flexible MSL routing. The size of dummy prefillers are 1×1 μm^2 and 2×2 μm^2, for lower and upper metal layers, respectively. These are small compared to typical MSL dimension (e.g., $W = 10$ μm for a 50 Ω MSL), so *granularity effects* are negligible. Simulation suggests that Z_0 and β typically change by $\sim$1% if upper 2×2 μm^2 dummies are shifted by 1 μm (following the modeling approach in the next section). In general, using larger fillers allow more efficient EM modeling, but with more serious granularity effects (automatic cheesing will set an ultimate limit). Placing smaller dummies will further reduce image currents and granularity effects, but at the cost of increased line capacitance (even at the same area filling ratio), due to the enhanced fringing fields from dummy side-walls.

B. Modeling the Effects of Dummies

In MSL environment, the most notable effect of dummies is increased line capacitance. Dummies are typically too small to support image current, and thus do not significantly change the line inductance. Major challenge in dummy modeling is its large problem size: EM simulation of a full dummy-filled structure does not seem feasible or practical [20]. Furthermore, because of anisotropic dummy shapes, the effective dielectric constant $\varepsilon_{r,\rm eff}$ depends on E-field orientation, further complicating modeling.

Fig. 6 illustrates the proposed approach to efficient dummy modeling. Note that a majority of metal dummies will be located at the bottom dielectric region, due to the smaller thickness and pitches of lower metallization levels. In an MSL, the E-field is nearly vertical in this bottom dielectric region (Fig. 6), and this allows simple modeling of the bottom region. First, take one dummy layer, e.g., in Metal-k. By simulating a parallel-plate capacitor (with vertical E-field), with Metal-k dummies inside, an adjusted ϵ_r of an equivalent dummy-free layer can be obtained for the same capacitance per unit area. Similar substitutions are subsequently applied to intermediate filling layers. For the uppermost filling layers, the E-field is no longer vertical, hence such substitutions cannot be applied; the lines are modeled including these uppermost fillers. This layer-substitution process significantly reduces the number of dummies, enabling efficient top-level EM simulation. For example, a 100-μm-long MSL is filled with $\sim$2500 dummies before reduction. Layer substitution for five bottom layers eliminates 85% of fillers, leaving only 380 dummies in top layers.

Fig. 7 shows MSL parameters as a function of prefilling area ratios, obtained by EM simulation after such dummy reduction (see Section V-F for a summary of the 65-nm technology used in this work). For 25% and 56% of dummy-filling area ratios, the line capacitance increases by 16% and 32%, respectively, with no essential change in line inductance. Given $\Delta L/L$ and $\Delta C/C$, fractional changes in L(nH/m) and C(pF/m), line characteristics will change as follows:

$$\frac{\Delta Z_0}{Z_0} \simeq \left(\frac{\Delta L}{L} - \frac{\Delta C}{C}\right)/2, \quad \frac{\Delta \beta}{\beta} \simeq \left(\frac{\Delta L}{L} + \frac{\Delta C}{C}\right)/2, \tag{1}$$

where $\Delta Z_0/Z_0$ and $\Delta\beta/\beta$ are relative changes in Z_0 and β, respectively. Therefore, Z_0 and β will change by -8% and $+8\%$ at a 25% filling ratio, and by -16% and $+16\%$ at 56% dummy filling.

Note the proposed dummy reduction approach may underestimate line losses, since eddy currents inside bottom prefillers [28] are ignored. Effective dielectric constants of dummy-free bottom layers can also be estimated by empirical formulas, e.g., by [29].

C. Ground Plane

Fig. 8 shows the construction of MSL ground planes. The two lowest metal layers, i.e., Metal-1 and Metal-2, were strapped together to mimic a solid metal plane, while still meeting density rules. This lowers ground impedance, and can minimize

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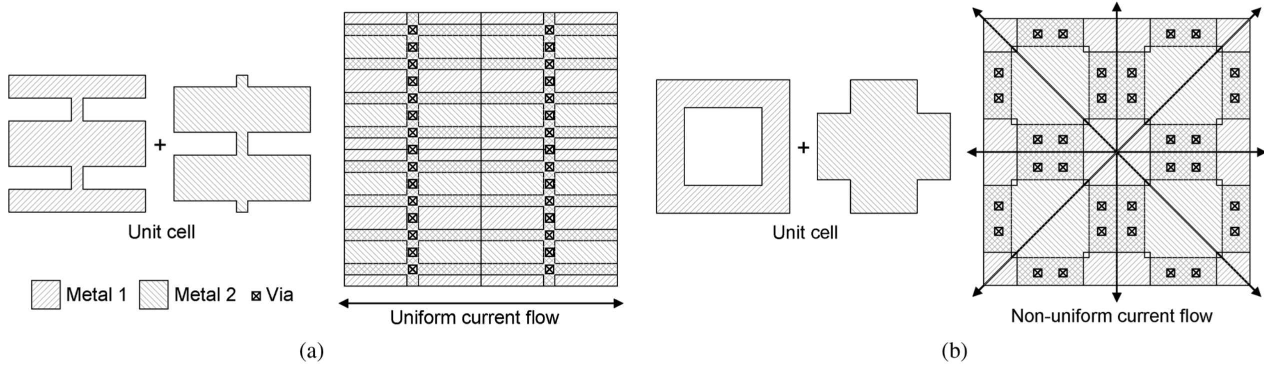

Fig. 8. Ground tiles for an MSL with (a) narrow holes where the current flow is uniform and orthogonal, and (b) square holes where the current flow is not uniform.

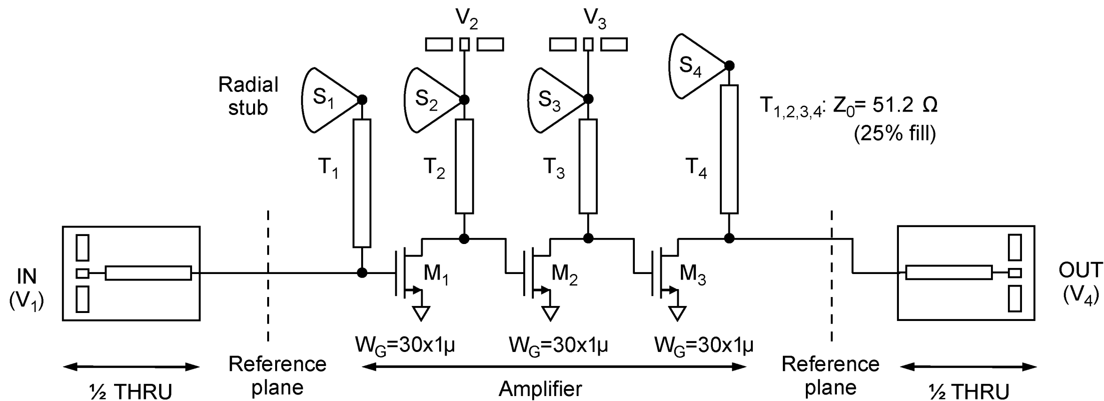

Fig. 9. Schematic of the three-stage 150 GHz amplifier.

E-field penetration to lossy substrate by having complementary hole shapes, thus reducing line losses (Ohmic losses in signal conductor may slightly increase for same Z_0 due to the reduced dielectric thickness). Depending on the expected current flow, either one of two predefined tiles are used: tiles with long narrow slots [Fig. 8(a)] [23] are used where the current flow is uniform (e.g., underneath an MSL). Ground tiles with square holes [Fig. 8(b)] are used under MSL discontinuities (e.g., bends, T-junction and cross), where the current flow is not uniform. Measurement shows that MSL losses at 150 GHz increase by 0.2–0.3 dB/mm if only Metal-1 tiles are used in the ground plane (see Section VI-A1).

V. 150 GHz Amplifier Design

A. Topology

With impedance matching alone, the highest gain that a single transistor can achieve, without compromising unconditional stability, is $\mathrm{MAG/MSG}$. In the case where the device has higher Mason's U than its $\mathrm{MAG/MSG}$, an external feedback can be employed to cancel transistor S_{12}, thus to *unilateralize* it (see, e.g., [30]–[32]). The resulting amplifier will be stable with $S_{21} = U$ and $S_{12} = 0$. For mm-wave CMOS amplifiers, this unilateralization technique may be difficult to apply. First, passive devices have relatively low quality factors at mm-wave frequencies, hence make the external feedback network lossy. This will partially offset the improvement in gain. Second, transistor internal feedback is subject to process variation (and substrate coupling), and therefore, its cancellation by external circuitry may not be effective.

In this work, multi-stage common-source (CS) configuration was chosen for the 150 GHz amplifier, as shown in Fig. 9. No unilateralization technique is considered because the Mason's U was not significantly higher than $\mathrm{MAG/MSG}$ at the design frequency. Simulation suggests that, beyond $\sim$120 GHz, a 65 nm CMOS cascode pair, while popularly used for 60 GHz designs up to W-band [7], [9], [10], [13], has no more gain than a CS transistor, especially under the requirement of low supply voltage, $V_{\rm DD} \leq 1.1$ V. (Note that cascode pairs have been used up to 170 GHz in 0.13 μm SiGe technologies [1], [3].)

All FETs are in PGF configuration, sized $W_G = 30\ \mu$m to simplify amplifier input and output matching, as will be discussed later. Dummy-prefilled MSLs with 25% filling ratio are used for impedance matching. Discussions on design features follow.

1) No dc-Block Capacitor: The three stages are dc-coupled (Fig. 9) with no dc-block capacitor, such that V_{DS} of a previous stage is equal to V_{GS} of the next stage. The degree of biasing freedom is only four, as opposed to six, forcing $V_{GS} = V_{DS}$ for M_1 and M_2. While this reduces the FET $\mathrm{MAG/MSG}$ by 0.4–0.5 dB relative to peak-gain drain bias, dc-coupling eliminates both losses and potential model errors associated with decoupling capacitors and their parasitic inductances, thereby easing design. Saturated output power $P_{\rm sat}$ is, however, not sacrificed since the final stage M_3 can have full drain bias up to $V_{\rm DD} = 1.1$ V. In this case, previous stages (M_1–M_2) can

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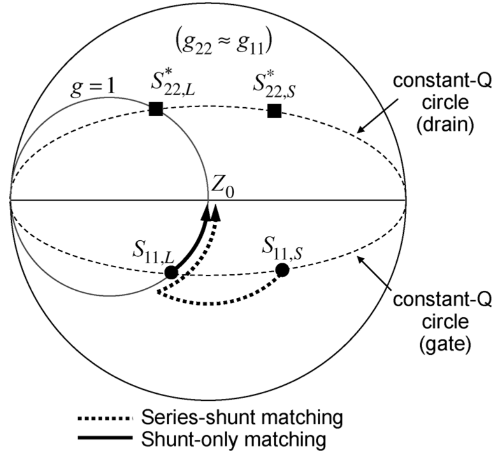

Fig. 10. Device sizing for low-loss input/output amplifier matching.

go into premature gain compression before M_3 fully saturates. Therefore, amplifier $P_{\rm 1dB}$ will be limited by front stages, and thus will not significantly increase with higher M_3 bias.

Two typical biasing schemes are as follows.

- $V_1 = V_2 = V_3 = V_4 = V_{\rm bias}$ ($V_{gs} = V_{ds}$ for all FETs);
- $V_1 = V_2 = V_3 = V_{\rm bias}$, with $V_4 = 1.1$ V (fixed);

2) Shunt-Only Impedance Matching: At the vicinity of design frequency, the 65 nm CS-FET exhibits nearly equal input and output conductance, i.e., $g_{11} \cong g_{22}$. This simplifies interstage matching to a single shunt inductor (T_2 and T_3 in Fig. 9) to tune out FET capacitances. No series element is necessary for impedance step-up or step-down, thus eliminating losses from series tuning as well as extending amplifier bandwidth.

At the amplifier input and output, FET S_{11} and S_{22} should be matched to Z_0, and series tuning may or may not be needed depending on the FET size. For relatively small FETs, series-tuning is necessary as illustrated by $S_{11,S}$ and $S_{22,S}$ in Fig. 10. As we increase the device size, S_{11} and S_{22} will move toward low-impedance regions along the constant-Q circle (thin dot lines). By appropriately sizing FETs ($W_G = 30$ μm for the present design), S_{11} and S_{22} will cross the unit-conductance circle (i.e., $S_{11,L}$ and $S_{22,L}$), allowing for shunt-only tuning (T_1 and T_4 in Fig. 9). Again, this eliminates losses from series element, as well as achieving wider bandwidth than series-shunt tuning. Similar shunt-tuning approach was considered in [12], [14], [20].

All shunt-tuning lines T_1–T_4 are ac-grounded by $(1/4)\lambda$ radial stubs S_1–S_4. Compared to 50 Ω $(1/4)\lambda$ MSLs, radial stubs have smaller series resistance $R_{\rm GND}$ on resonance, thus reducing matching loss as will be shown later. They present low input impedance over wider bandwidth too, than 50 Ω lines, which extends amplifier bandwidth.

3) Thru-Reflect-Line Calibration: In this work, TRL calibration method was employed with custom on-chip standards. The three-stage amplifier is layout between two 1/2-THRU's, which define input and output reference planes (Fig. 9). In TRL calibration, the effect of direct probe-probe coupling, which is more pronounced at higher frequencies, can be minimized by placing references planes sufficiently distant (e.g., 200 μm) from probe pads. In open-short type deembedding techniques, accurate subtraction of pad impedances is difficult without placing reference planes close to the pads, thus introducing substantial probe-probe coupling.

B. Effects of Lossy Matching Elements

With lossless conjugate matching networks, the gain of the three-stage amplifier would be $(\mathrm{MAG})^3$. In practice, losses from T_1–T_4 can create significant departure from this theoretical maximum gain. *Lossy* ac-ground, which terminates T_1–T_4, introduces further signal loss, due to $R_{\rm GND}$, its series resistance at resonance. For clarity, consider for now $R_{\rm GND} = 0$ (i.e., ideal ac-ground with zero impedance). Its effect will be accounted for later.

For simplicity, the following are assumed.

- M_1–M_3 are unilateral, i.e., $y_{12} = 0$ (this is only approximately true, especially near $f_{\rm max}$).
- M_1–M_3 have equal input and output conductance, i.e., $g_{11} = g_{22}$ (this is approximately true with 30 μm/65 n FETs at 150 GHz).
- T_1–T_4 have the same quality factor, $Q_{\rm ind}$.

Under these assumptions, it can be shown that the gain of a three-stage amplifier is given by

$$S_{21} = \left(G_{T,\max}\left(\frac{Q_{\rm ind}}{Q_{\rm ind}+Q_{11}}\right)\left(\frac{Q_{\rm ind}}{Q_{\rm ind}+Q_{22}}\right)\right)^3 \quad (2)$$

where $G_{T,\max} = |y_{21}|^2/4g_{11}^2 = |y_{21}|^2/4g_{22}^2$ is the maximum available gain of unilateralized FETs (recall it is assumed $g_{11} = g_{22}$). Q_{11} and Q_{22} are transistor input and output quality factors, respectively, defined as $Q_{11} = b_{11}/g_{11}$ and $Q_{22} = b_{22}/g_{22}$ ($y_{ij} = g_{ij} + jb_{ij}$ is the transistor y-parameter).

The effect of lossy matching networks is clearly seen in (2). For example, if $T_1 - T_4$ and FETs have the same quality factor, i.e., $Q_{\rm ind} = Q_{11} = Q_{22}$, the gain drop per stage is $|10\log_{10}(1/2)^2| \cong 6$ dB, making any transistor with less than 6 dB of maximum available gain a completely passive element. A tuning inductor with $\times 2$ and $\times 4$ the transistor quality factor introduces gain drop of 3.5 dB and 1.9 dB per stage, respectively. Note the gain reduction in (2) only depends on *the ratio of quality factors*, not their absolute values.

C. Effects of AC Ground Resistance

The ac-ground resistance $R_{\rm GND}$ can be conveniently lumped into the series resistance of $T_1 - T_4$ by defining $\overline{Q_{\rm ind}}$, inductor quality factor degraded by lossy ac termination, i.e.,

$$\begin{aligned}\overline{Q_{\rm ind}} &= Q_{\rm ind} \| Q_{\rm ind,GND} \\ &= \left(Q_{\rm ind}^{-1} + Q_{\rm ind,GND}^{-1}\right)^{-1}\end{aligned} \quad (3)$$

where $Q_{\rm ind,GND} = \omega L_{\rm tune}/R_{\rm GND}$ represents the maximum possible quality factor of a tuning inductance $L_{\rm tune}$, limited by ac-ground resistance $R_{\rm GND}$. Note that $\overline{Q_{\rm ind}}$ is bounded by the lesser of $Q_{\rm ind}$ and $Q_{\rm ind,GND}$. Therefore, any finite $Q_{\rm ind,GND}$ will further reduce the amplifier S_{21}. Now, $\overline{Q_{\rm ind}}$ can replace $Q_{\rm ind}$ in (2) to account for the effects of lossy ac-termination.

D. Simulated Amplifier Gain

The designed amplifier has the following parameters at 150 GHz.

- $G_{T,\max} \simeq 6$ dB.

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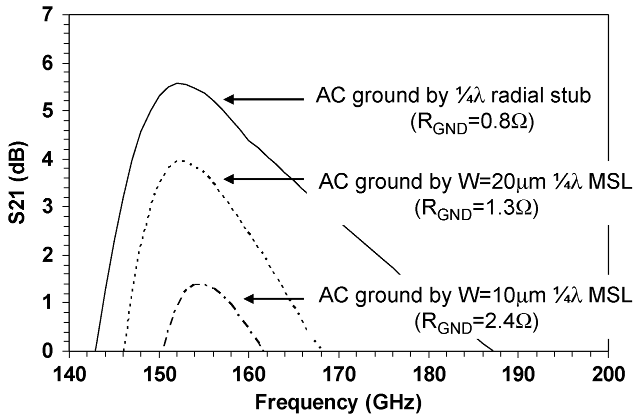

Fig. 11. Simulated gain of the 150 GHz amplifier. Series resistance of ac ground at resonance significantly degrades S_{21}. Wideband ac-ground extends amplifier 3-dB bandwidth: 25 GHz and 18 GHz for radial stubs and $W = 20\ \mu$m $(1/4)\lambda$ MSLs, respectively.

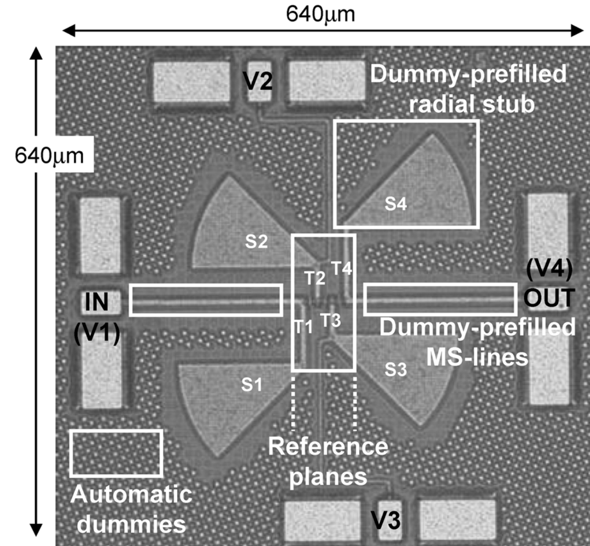

Fig. 12. Chip photograph for the three-stage 150 GHz amplifier.

- $Q_{11} \simeq Q_{22} \simeq 2.4$: Actual Q_{11} is 15% higher than Q_{22}, but this approximation simplifies calculation.
- $L_G \simeq L_D \simeq 30$ pH: Gate and drain tuning inductances needed to resonate FET capacitances.
- $Q_{\rm ind} \simeq Q_{TL} = 17$: Quality factor of dummy-prefilled MSLs for gate and drain tuning inductors.
- $R_{\rm GND} \simeq (5/3)0.8\ \Omega$: Actual series resistance of a single $(1/4)\lambda$ radial stub is 0.8 Ω. The factor 5/3 is due to the sharing of a single radial stub at inter-stages.

It follows that $Q_{\rm ind,GND} = \omega L_{G/D}/R_{\rm GND} \simeq 21.2$. Therefore, the series resistance of ac-ground is reducing the inductor quality factor by almost half, since $\overline{Q_{\rm ind}} = 17||21.2 \simeq 9.4$. Thus, the simple gain estimation (2) yields $S_{21} = 6.2$ dB. Simulation of the full schematic in Fig. 9 gives $S_{21} = 5.6$ dB (solid curve in Fig. 11), which is in close agreement with the simple prediction. With lossless ac ground ($R_{\rm GND} = 0$), S_{21} goes up to 11.1 dB and 10.5 dB, according to the prediction (2) and simulation, respectively.

If $(1/4)\lambda$ MSLs with $W = 20\ \mu$m and $W = 10\ \mu$m were used to define ac-ground, $R_{\rm GND}$ would be $(5/3)1.3\ \Omega$ and $(5/3)2.4\ \Omega$, respectively. Eq. (2) predicts 3.3 dB and −2.4 dB of amplifier gain, with resulting $\overline{Q_{\rm ind}}$ equal to 7.4 and 5.0, respectively. Full-schematic simulation gives 3.9 dB and 1.3 dB of gain, for each bias line, as shown in Fig. 11.

The behavior of ac-ground at resonance has strong effects on the amplifier bandwidth as well as its gain. Note that the use of radial stubs yields 25 GHz of amplifier 3-dB bandwidth, which is 40% improvement over $(1/4)\lambda$ MSLs-based bias lines. This is due to the smaller series inductance in radial stubs than $(1/4)\lambda$ MSLs with $W = 10\ \mu$m or $W = 20\ \mu$m.

For schematic simulation, Agilent Advanced Design System (ADS) was used along with transmission-line compact model (fit to the line data obtained in Section IV). Radial stubs were modeled by 2.5D EM simulator (Agilent Momentum), but its ADS compact model also gave reasonable correlation.

E. Layout

Fig. 12 shows the amplifier layout. All areas under MSLs, T-junctions, radial stubs, as well as probe pads, were prefilled at 25%. Prefilling under probe pads is especially important for accurate TRL calibration, as these are part of calibration structure. To maintain *Manhattan* geometry, radial stubs S_1–S_4 were drawn with staircase approximation in 1 μm resolution. Ground tiles and dummy prefillers (of multiple metal layers) are grouped as a 4 μm × 4 μm cell, and were copied throughout the layout (similar approach was used in [33]).

In Fig. 12, layout elements (T_1–T_4, S_1–S_4, and 1/2-THRUs) are spaced apart by at least $5d$ ($d \simeq 5\ \mu$m: MSL substrate thickness), so that their field coupling is negligible. For example, T_1 and T_3 (or T_2 and T_4) are 25 μm apart, and EM simulation confirms their crosstalk is below −35 dB. Similarly, S_2 and the input 1/2-THRU (or S_3 and the output 1/2-THRU) are 35 μm apart, and their interaction is also small. Design verification is therefore simplified, since top-level EM simulation with the entire layout is unnecessary.

The overall layout measures 640 μm × 640 μm = 0.4 mm^2 including four pads, but 0.16 mm^2 without pads. The core circuit without radial stubs is compact (85 μm × 170 μm = 0.014 mm^2), due to the absence of series tuning lines.

F. Technology

The amplifier was fabricated in IBM's 65 nm high-speed CMOS technology with the "4302" back-end metal stack (9Cu+1Al): four 1× thin metals and three 2× metals over low-k dielectric, two 4× layers over TEOS/FTEOS dielectric, and a ∼ 1.2 μm thick top aluminum layer. No special RF options such as MIM capacitors or ultra-thick top copper layer were used. Nominal supply voltages are 1.0–1.1 V.

Among the 10 metal layers available, only three layers are actively used in this work: the top aluminum layer for a MSL signal, and Metal-1/2 for MSL ground ($d \simeq 5\ \mu$m: substrate thickness). Other layers are essentially filled with dummy fillers or part of via stack.

VI. Measurement Results

S-parameter measurement was performed using two different VNA setups: Agilent PNA network analyzer for V-band

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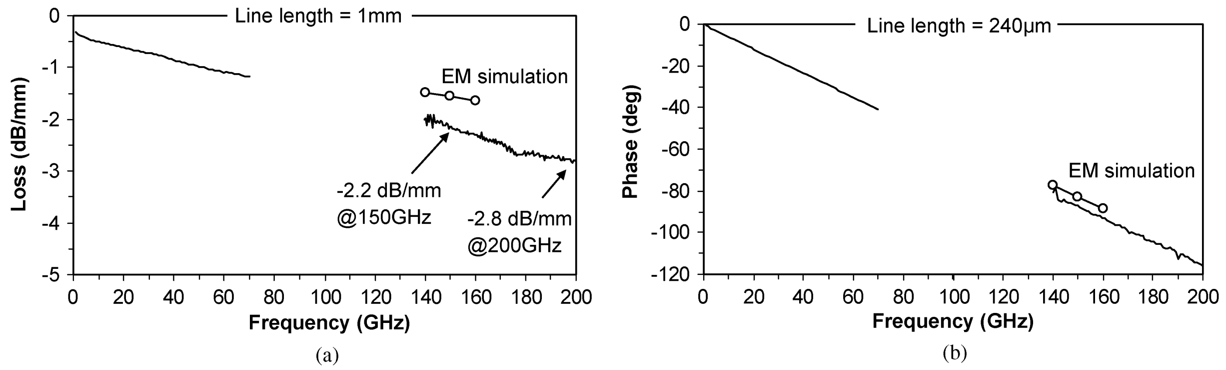

Fig. 13. Measured (a) loss and (b) phase characteristics of dummy-prefilled microstrip lines. Prediction from EM simulation is also shown.

measurement (1–67 GHz), and HP8510C VNA with mm-wave heads from Oleson Microwave Labs (V05VNA-T/R) for G-band characterization (140–200 GHz). For V-band measurement, pad capacitance was deembedded after probe-tip calibration using impedance standard substrate. G-band data rely on on-wafer TRL calibration. Re-measuring TRL standards after calibration results $S_{11,\rm THRU} < -40$ dB, $S_{21,\rm THRU} < 0.1$ dB and $S_{11,\rm LINE} < -35$ dB, confirming measurement repeatability. Direct probe-probe coupling was below -40 dB.

To characterize large-signal characteristics of the 150 GHz amplifier, custom measurement setup was used. GGB Picoprobes with 100 μm pitch were used for all measurements.

A. *Dummy-Prefilled Microstrip Lines*

Fig. 13 shows the measured characteristics of dummy-prefilled MSLs in two frequency bands.

1) Line Loss: In Fig. 13(a), the attenuation constant α, measured from a 1-mm-long line, is 2.2 dB/mm (=253 Np/m) and 2.8 dB/mm (=322 Np/m), at 150 GHz and 200 GHz, respectively, where $\gamma = \alpha + j\beta$ is the propagation constant. This corresponds to a transmission line quality factor $Q_{TL} = (\beta/2\alpha) \approx 12$. Since series line losses dominate the line attenuation, the inductive line quality factor [34] is also approximately 12. Measured line losses are 0.5–0.6 dB higher than what EM simulation predicts. This discrepancy can be attributed to a number of factors that were not considered in MSL modeling: substrate losses from field penetration through relative thin ground plane ($t \sim 2.5\delta_{\rm skin\ depth}$), ohmic losses in metal dummies due to eddy currents, losses in the ground plane due to surface roughness (Fig. 8), among others. MSLs with only Metal-1 ground tiles (Fig. 8) were measured for comparison. They exhibited 0.2–0.3 dB/mm higher losses than reference MSLs with Metal-1 and Metal-2 ground planes (10% reduction in Q_{TL}).

Measured losses of the proposed MSL are comparable or superior to previous on-chip transmission-line results in similar technologies: 1.5 dB/mm and 5 dB/mm at 110 GHz (65 nm CMOS) [26], 1 dB/mm (90 nm CMOS) and 1.4 dB/mm (SiGe) at 110 GHz [22], 3.5 dB/mm at 110 GHz (90 nm CMOS) [35], 5 dB/mm at 150 GHz and 10 dB/mm at 200 GHz (65 nm CMOS) [36] and 3 dB/mm at 110 GHz (0.13 μm CMOS) and 6 dB/mm (90 nm CMOS) [37]. Note that the proposed dummy-prefilled MSL structure is fully compatible with pattern density rules, with no metal fill or hole exclusion necessary.

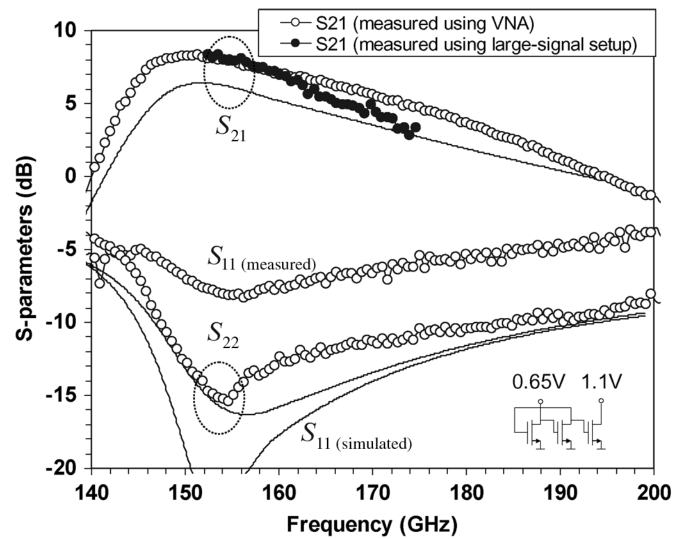

Fig. 14. Measured (circles) and simulated (solid lines) S-parameters of the three-stage 150 GHz amplifier ($P_{\rm DC}$ = 25.5 mW).

2) Phase and Characteristic Impedance: Fig. 13(b) presents the measured insertion phase of a 240-μm-long microstrip line (a LINE standard for G-band TRL calibration), and compares with prediction. Measured line phase stays within $\pm 26^\circ$ from the nominal 90° across 140–200 GHz, but is $\sim$6% greater than the simulation. To find out the possible cause, the V-band data set was taken to compute RLGC line parameters through the manipulation of $ABCD$ matrix parameters [38], and EM simulations were run at V-band for comparison (RLGC parameters are difficult to characterize directly in the G-band, since TRL calibration leaves the line impedance unknown, and accurate probe-pad deembedding is difficult otherwise at such high frequencies). The extracted C(pF/m) was $\sim$14% greater than the model, but there was less than 2% difference in L(nH/m). If we assume line capacitance is frequency-independent (or if the actual line capacitance follows similar frequency dependency to EM simulation), the increase in line capacitance (in V-band) can explain the extra line phase observed (in G-band), according to (1). The discrepancy in line capacitance may be due to possible inaccuracies in dielectric stack definition or process variations. From (1), the line impedance Z_0 is expected to reduce,

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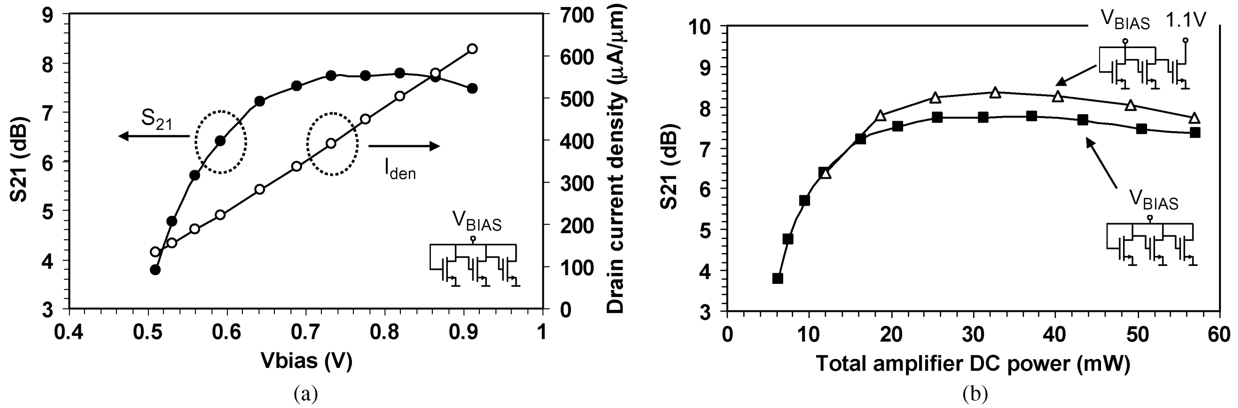

Fig. 15. Bias voltage sweep: Gain (S_{21}) at 150 GHz versus (a) drain current density and (b) total dc power.

too, by ~7%, which correlates well with the V-band measurements. S-parameters of the 150 GHz amplifier, to be discussed next, are renormalized taking this change in Z_0 into account.

Note measurements from two frequency bands in Fig. 13 are reasonably consistent, as the line loss or phase extrapolated from the V-band edge closely matches with the G-band data. In overall, measured data suggest that the proposed dummy-prefilled microstrip line may be adequate for low-Q impedance matching up to 200 GHz ($Q_{TL} \approx 12$), and that its characteristics can be predicted with reasonable accuracy by the proposed dummy modeling approach.

B. 150 GHz Amplifier

The performance of the 150 GHz amplifier was characterized in G-band, after moving the reference plane to the edge of 1/2-THRU by TRL calibration.

1) S-Parameter Measurement: Measurement results are plotted in Fig. 14, and compared with simulation. The measured S_{21} is 8.3 dB at 150 GHz with 27 GHz of 3 dB bandwidth (18% of fractional bandwidth). S_{21} remains above 0 dB until 194 GHz. S_{11} and S_{22} is less than -7 dB and -13 dB at 150 GHz, respectively. The reverse isolation, S_{12}, is below -18 dB. The amplifier remains unconditionally stable across the full band. The dc power consumption $P_{\rm DC}$ is 25.5 mW at the nominal bias point of $V_1 = V_2 = V_3 = 0.65$ V and $V_4 = 1.1$ V. The drain current density $I_{\rm den}$ is 340 μA/μm for M_1 and M_2, and 355 μA/μm for M_3.

The trade-off between amplifier gain and dc power consumption is examined. First, all FETs are set to an equal bias condition with $V_{gs} = V_{ds} = V_{\rm bias}$, i.e., $V_1 = V_2 = V_3 = V_4 = V_{\rm bias}$. S_{21} is measured while varying $V_{\rm bias}$, and plotted in Fig. 15(a) along with the associated FET I_{den}. A practical optimum is found $I_{den} \simeq 350$ μA/μm, since consuming more dc power gives only diminishing return in S_{21}. Note that this current density level is higher than reported in previous mm-wave CMOS amplifiers [2], [34], [39] where the drain is typically held at higher potentials, e.g., 1 V–1.1 V. For the designed amplifier, a better trade-off between S_{21} and $P_{\rm DC}$ is possible if M_3 is biased at full drain potential, i.e., $V_4 = 1.1$ V. Fig. 15(b) shows that separately biasing M_3's drain can increase S_{21} by 0.4–0.6 dB at similar $P_{\rm DC}$, once transistors are in saturation region.

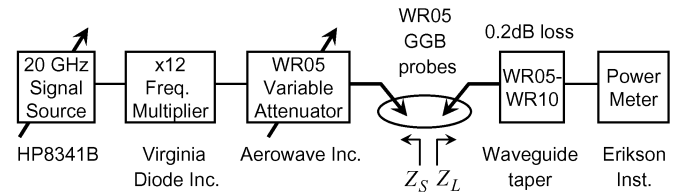

Fig. 16. G-band large-signal measurement setup (153 GHz to 173 GHz).

2) Large-Signal Measurement: Large-signal characteristics of the 150 GHz amplifier were measured using custom setup in Fig. 16. A multiplier diode module from Virginia Diodes, Inc. generates RF power from 153 GHz and above, and drives the amplifier through a WR05 variable attenuator. The amplifier output power is measured by a calorimeter from Erikson Instruments through a short section of WR05-to-WR10 waveguide taper. The setup can supply up to $+10$ dBm of input power with 35 dB of control range, which is sufficient to saturate the amplifier while still covering small-signal region. All power measurements are calibrated to the reference planes in Fig. 9 by separately measuring the on-wafer THRU standard, thus deembedding losses from the probes, probe pads and 200-μm-long 1/2-THRUs (~3.5 dB/port).

Fig. 17 summarizes power-sweep results at the nominal bias point of $V_1 = V_2 = V_3 = 0.65$ V and $V_4 = 1.1$ V ($P_{\rm DC} =$ 25.5 mW). Gain compression starts at $P_{\rm 1dB} = 1.5$ dBm and 2 dBm, with fully saturated output power $P_{\rm sat} = 6.3$ dBm and 6.7 dBm, at 153 GHz and 158.4 GHz, respectively. At $V_4 =$ 1.3 V, $P_{\rm sat}$ increases by 0.6–0.7 dB. The difference in $P_{\rm 1dB}$ and $P_{\rm sat}$ is ~5 dB, which is attributed to premature saturation of driving stages (Section V-A1). Measured power curves reasonably agree with simulation at 150 GHz where $P_{\rm 1dB} = 1$ dBm and $P_{\rm sat} = 4.4$ dBm was predicted. Peak power-added-efficiency (PAE) was measured 8.4% and 9.5%, at 153 GHz and 158.4 GHz, respectively.

The frequency of the input signal was swept from 153 GHz to 175 GHz at $P_{\rm in} = -10$ dBm. The resulting S_{21} curve (obtained from the large-signal setup, but still small-signal gain) closely follows the VNA measurement, as shown in Fig. 14. There is ~2 dB discrepancy above 160 GHz, which is partly due to power meter drifts, but mainly because the source and load impedances at the reference planes (Z_S and Z_L in Fig. 16) are not perfect

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TABLE I
COMPARISON OF STATE-OF-THE-ART mm-WAVE AMPLIFIERS IN SILICON AT OR BEYOND 77 GHz

	This work	[1]	[2]	[3]	[4]	[5]	[15]	[6]	[7]	[9]	[13]	[19]	[10]	[11]	[12]	[14]
Technology	**65nm CMOS**	0.13μ SiGe	65nm CMOS	0.13μ SiGe	90nm CMOS	65nm CMOS	90nm CMOS	0.12μ SiGe	90nm CMOS	65nm CMOS	90nm CMOS	0.12μ SiGe	65nm CMOS	65nm CMOS	65nm CMOS SOI	90nm CMOS
f center [GHz]	**150**	170	140	140	104	100	100	99	97	95	94	89	80	80	80	77
3dB BW [GHz]	**27**	14	10	18	2*	21	17	14	22	> 19	>20	17	20	6	28*	17.5
Fractional BW [%]	**18**	8	7	13	2	21	17	14	23	>20	>21	19	25	8	35	23
Gain [dB]	**8.2**	15	8	18	9.3	13	17	26	17.4	13	4.8	19	13.5	12	7.2	8.5
No. of stages	**3**	5	6	5	3	4	3	12	3	3	2	4	3	6	3	4
S_{11} [dB]	**-7.4**	-	-	-12#	-9.8	-8*	<-6	-15	< -15	-15	<-25	-7*	-20	-12	-11	-
S_{22} [dB]	**-13.6**	-	-	-19#	-5.5	-11*	<-14	-12	< -15	-	-10	-9*	-	-11	-9	-
V_{DD} [V]	**1.1**	3	1.2	3	1	1.2	3	2	2.5	1.5	1.8	1.5	1.5	1.2	1	1.2
P_{DC} [mW]	**25.5**	135	63	112	22	86	290	78	54	35	30	25.2	36.3	32	70	142.2
P_{sat} [dBm]	**6.3**	> 0	> -1.8	-	-	10	12	-	4	-	-	-0.5	4	-	-	6.3
P_{1dB} [dBm]	**1.5**	0	-5	-1	-	6	8	-0.1	2	> -6	-	-3	-1.6	-9	3.5#	4.7
Topology	**3CS**	3CC +2CE	3CS +3CG	3CC +2CE	3CS	4CS	1CC+ 2BCC	CCWA	3CC	3CC	2CC	4CE	3CC	6CS	3CS	4CS
Matching Elements	**MSL**	lumped	lumped	lumped	CPW	CPW	MSL	CPW	MSL	lumped	lumped	CPW	lumped	lumped	CPW	MSL
Area [mm^2]	**0.4 ×0.4**	0.29 ×0.15	0.3 ×0.2*	0.4 ×0.2	0.64 ×0.38*	0.18*	0.63 ×0.42*	0.12*	0.57 ×0.52*	0.12 ×0.12*	-	0.3 ×0.35	0.16 ×0.1*	0.48 ×0.2*	0.44*	0.94 ×0.36*

Simulation
* Estimate from either plots or chip micrographs (not including pads)
CS: Common-Source, CG: Common-Gate, CC: Cascode, CE: Common-Emitter, BCC: Balanced Cascode, CCWA: Cascaded Constructed Wave Amp.

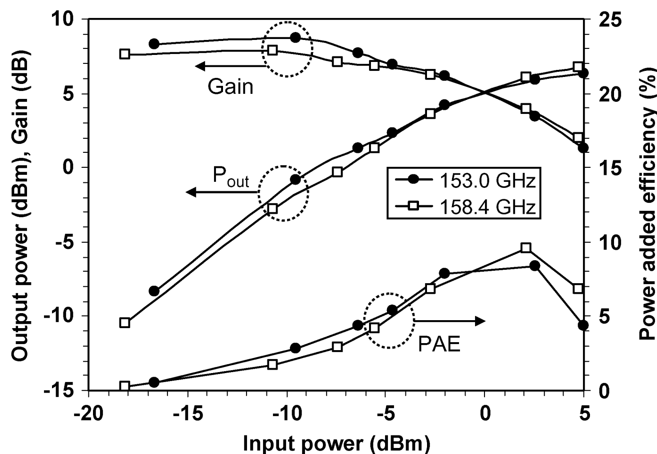

Fig. 17. Measured large-signal characteristics of the 150 GHz amplifier ($V_1 = V_2 = V_3 = 0.65$ V and $V_4 = 1.1$ V).

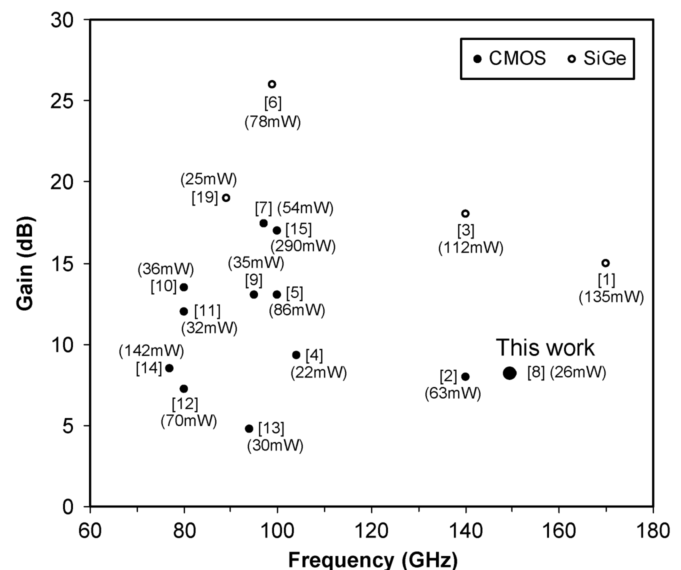

Fig. 18. Recently reported mm-wave amplifiers in silicon. DC power consumption is also shown.

50 Ω (or more precisely, Z_0 of the THRU lines), due to pad capacitances and reflections from the probes, among others.

3) Performance Comparison: Table I and Fig. 18 compare CMOS or SiGe mm-wave amplifiers at or beyond 77 GHz (SiGe amplifiers are considered only for W-band and beyond). Note simple CS topology has been preferred for CMOS amplifiers beyond 100 GHz. This work represents the highest frequency CMOS amplifier among reported, with state-of-the-art performance in $P_{\rm sat}$, $P_{\rm 1dB}$, $P_{\rm DC}$, and 3 dB bandwidth.

Comparison with compound semiconductor IC technologies will be interesting, where circuit bandwidth is enhanced by higher transistor $f_{\max}$: InP HEMT amplifiers have been demonstrated at 340 GHz with 15 dB gain (three-stage) [40] and 308 GHz with 4.4 dB gain (single-stage) [41]. InP HBT amplifiers have been reported at 324 GHz with 4.8 dB gain (single-stage) [42] and 255 GHz with 3.5 dB gain (single-stage) [43].

VII. CONCLUSION

A 150 GHz amplifier in digital 65 nm CMOS is presented, based on minimalistic topology to reduce matching loss (thus increasing output power) as well as modeling uncertainties. Shunt-only tuning also extends bandwidth due to the absence of impedance translation. Dummy-prefilled microstrip line

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is proposed and modeled by an efficient dummy-reduction approach.

Measurement of the amplifier and dummy-prefilled lines shows a close agreement between prediction and measurement, verifying the design approach. It further suggests that the dummy-prefilled lines can be used to even beyond 200 GHz. All measurement in this paper is from first silicon.

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Munkyo Seo (M'08) received the B.S.E.E. and M.S.E.E. degrees in electronic engineering from Seoul National University, Seoul, Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical engineering from the University of California, Santa Barbara (UCSB), in 2007.

From 1997 to 2002, he was a Research Engineer with LG Electronics Inc., where he designed RF and microwave subsystems for wireless communication. He was an Assistant Project Scientist with the University of California, Santa Barbara, where he worked on millimeter-wave circuit design in nanoscale CMOS and HBT technologies from 2008 to 2009. In 2009, he joined Teledyne Scientific and Imaging, Thousand Oaks, CA, where he is working on the design of high-resolution data converters and millimeter-wave circuits.

Dr. Seo won the 2008 UCSB Lancaster Dissertation Award for his dissertation in the area of Mathematics, Physical Sciences, and Engineering. He also received an Honorary Mention in the Student Paper Competition of 2008 IEEE MTT-S International Microwave Symposium for his work on distributed phased array techniques for energy-efficient wireless sensor networks.

Basanth Jagannathan received the Bachelor's degree from the Indian Institute of Technology, Kharagpur, India, in 1992 and the Ph.D. in electrical engineering from the State University of New York at Buffalo in 1998.

He is a Senior Engineer in IBM's Semiconductor Research and Development Center. He has over ten years of experience leading technology development and enablement for state-of-the-art silicon based RF and mm-wave products. His current focus is on technology, device design and modeling for RF applications in advanced CMOS technologies through 22 nm. Previously, he worked in SiGe BiCMOS technology development where he was leading HBT design and fabrication in 180 and 130 nm nodes. His work was pivotal in the development of the world's first silicon HBT operating is excess of 250 GHz. He has authored over 50 publications in leading journals and conferences and holds 24 patents.

Dr. Jagannathan was the recipient of IBM's patent portfolio award in 2008. He was also the recipient of the IEEE George E. Smith award for the best paper in IEEE ELECTRON DEVICE LETTERS in 2002. He served as the Technical Program Chair for the 2009 Silicon Monolithic Integrated Circuits for RF conference.

John Pekarik (M'92) received the B.S. degree in electrical engineering from Lehigh University, Bethlehem, PA, in 1985, the M.S. degree from Polytechnic University, Brooklyn, NY, in 1988, and the Ph.D. degree in electrical engineering from the University of California, Santa Barbara, in 1993.

He joined IBM in 1985 working on developing high-speed silicon bipolar technology at the East Fishkill, NY facility. Following an educational leave, he returned to IBM at the Burlington, VT facility in 1992. He has worked on technology development for DRAM and digital CMOS in bulk silicon and SOI, compact modeling of devices, and manufacturing engineering. His recent focus has been developing IBM's technology and design tools to better support RF applications. He currently works with IBM's partner, ST Microelectronics, in Crolles, France, developing RFCMOS technology. He serves as chairman of the Wireless Technology Working Group of the ITRS. He previously served as Adjunct Professor of electrical engineering at the University of Vermont.

Mark J. W. Rodwell (M'89–SM'99–F'03) received the B.S. degree from the University of Tennessee at Knoxville in 1980, and the M.S. and Ph.D. degrees from Stanford University, Stanford, CA, in 1982 and 1988, respectively.

He is a Professor and Director of the Nanofabrication Laboratory, the NSF Nanofabrication Infrastructure Network, and the SRC Nonclassical CMOS Research Center with the University of California, Santa Barbara. He was with AT&T Bell Laboratories during 1982–1984. His research focuses on high-bandwidth InP bipolar transistors, compound semiconductor field-effect transistors for VLSI applications, and millimeter-wave integrated circuit design in both silicon VLSI and III-V processes.

Prof. Rodwell received the 1997 IEEE Microwave Prize for his work on GaAs Schottky-diode ICs for millimeter-wave instrumentation.

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