200-nm InGaAs/InP TYPE I DHBT EMPLOYING A DUAL-SIDEWALL EMITTER PROCESS DEMONSTRATING f_{max} > 800 GHz AND f_τ = 360 GHz

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Abstract

Type I InP/InGaAs/InP double heterojunction bipolar transistors were fabricated using a simple mesa structure, where emitter junction widths have been scaled from 250 nm to 200 nm. These devices exhibit f_{max} in excess of 800 GHz, and f_τ = 360 GHz. Greater than fifty percent device yield was obtained by employing two 25 nm SiN_x sidewalls to protect and anchor the refractory metal emitter contact to the emitter semiconductor. A hybrid dry and wet etch process is used to form a vertical emitter mesa, causing reductions in both the emitter-base gap resistance R_{gap} and the spreading resistance beneath the emitter $R_{b,spread}$, leading to an expected and observed increase in f_{max}. Peak HBT current gains $\beta \approx$ 21-33, $BV_{ceo} \sim$ 4 V, $BV_{cbo} \sim$ 5 V, and J_e at low V_{cb} is over 10 mA/μm^2.

Index Terms—InP heterojunction bipolar transistor

I. Introduction

Lithographic and epitaxial scaling of key HBT dimensions results in increases to transistor performance, enabling digital logic and mixed-signal systems which operate at higher clock speeds and bandwidths [1]. Several key scaling challenges to increasing HBT current gain cutoff frequency f_τ, power gain cutoff frequency f_{max}, and digital logic speeds exist: fabricating narrow emitter-base junctions, reducing the emitter and base Ohmic contact resistivities, and being able to operate devices at high current densities close to the maximum current density set by the Kirk effect.

In this work, dry etches are used to pattern a refractory emitter metal contact and emitter semiconductor mesa, as the dimensions of features formed through evaporated metal lift-off and chemical wet etch processes become difficult to control when features are scaled below 250 nm. An additional challenge at this scaling generation is loss of emitter contact adhesion arising from both mechanical strain in the contact metal and narrow contact width. In order to increase device yield, these effects are mitigated by protecting and anchoring the contact to the emitter mesa through the formation of two dielectric sidewalls.

We report InP/InGaAs/InP double heterojunction bipolar transistors fabricated in a triple-mesa structure, where the emitter junctions have been scaled from 250 nm to 200 nm, and simultaneous f_{max} > 800 GHz and f_τ = 360 GHz have been demonstrated. To our knowledge, this is the highest f_{max} reported for a mesa HBT, as well as the narrowest reported emitter width. Previous record f_{max} reported was 755 GHz, and was observed at the 250 nm node [2].

II. Growth and Fabrication

The epitaxial HBT material was grown on a 4" semi-insulating InP wafer. These devices have an epitaxial structure identical to those reported in [2], which include a 30 nm InGaAs base and 150 nm collector region, consisting of a 24 nm InGaAs/InAlAs superlattice grade and InP drift collector.

The sample surface is prepared by a UV-ozone oxidation and a concentrated NH_4OH rinse immediately prior to sputtered emitter metal deposition. The sputtered metal stack consists of an interfacial 5 nm Ti layer, followed by 500 nm of $Ti_{0.1}W_{0.9}$ alloy. SiO_x 100 nm thick is then blanket deposited by PECVD, followed by 40 nm of Cr by e-beam evaporation. The Cr layer is patterned by I-line stepper lithography to form a Cr etch mask, which is used to define the TiW emitter contact by inductively coupled plasma (ICP) dry etch. A 25 nm SiN_x sidewall is formed by blanket PECVD deposition and anisotropic ICP dry etch. This sidewall protects the Ti layer of the emitter from etching in the subsequent InGaAs chemical wet etch. The N^{++} InGaAs cap is removed by an isotropic H_3PO_4:H_2O_2 chemical wet etch, which also forms a ~10 nm undercut beneath the contact. At this point, a second 25 nm SiN_x sidewall is formed using processes identical to those which formed the first sidewall. This sidewall adheres to the existing sidewall, the sides of the N^{++} InGaAs mesa, and the lateral undercut of the contact, anchoring the contact in place and increasing the yield of emitter contacts. The InP emitter is then etched in a hybrid ICP dry etch and H_3PO_4:HCl wet etch as described in [3]. The anisotropic ICP portion of the etch provides controllable emitter mesa undercut, while the wet etch is selective to InP versus InGaAs, permitting the etch to stop without damaging the surface of the base upon which

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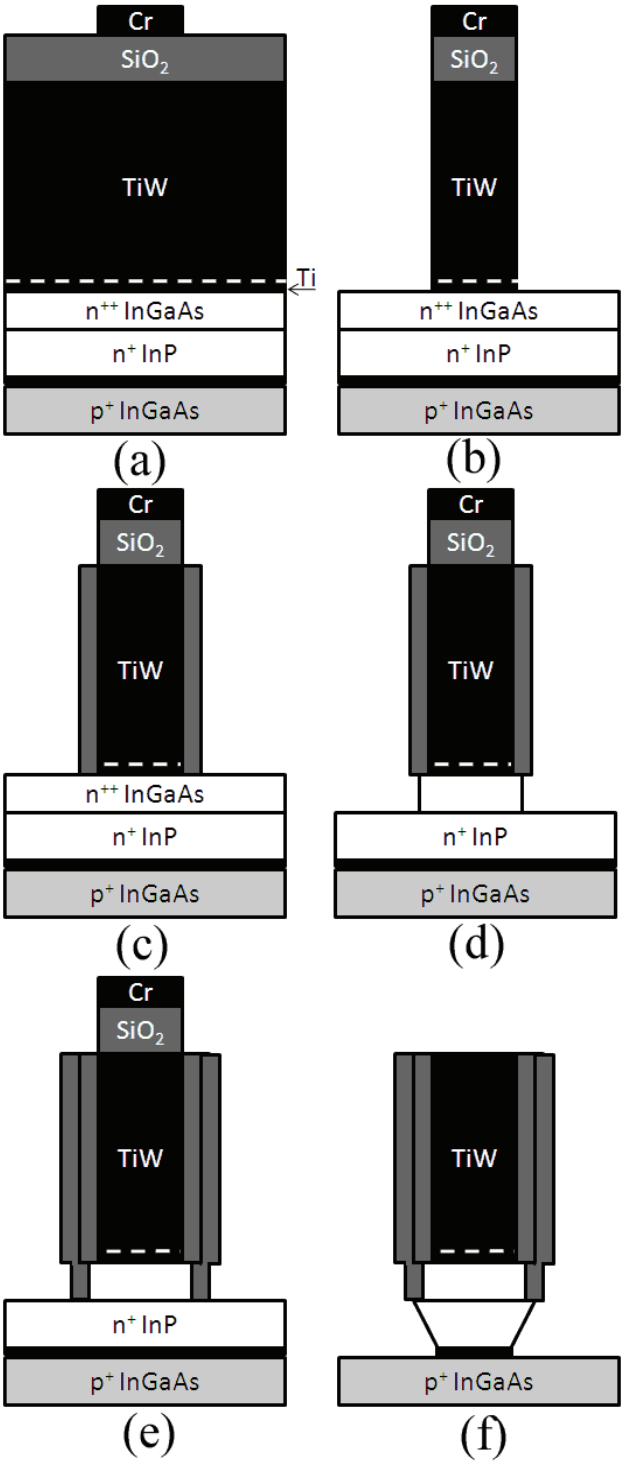


Figure 1: (a) Cr etch mask formation on blanket-deposited SiO_x and TiW, (b) SF_6 ICP etch through SiO_x and TiW, (c) Blanket PECVD SiN_x deposition and CF_4 ICP etch, (d) InGaAs H_3PO_4:H_2O_2 wet etch, (e) Second SiN_x sidewall, (f) Cl_2 ICP etch and H_3PO_4:HCl etch of InP, followed by HF SiO_x cap removal

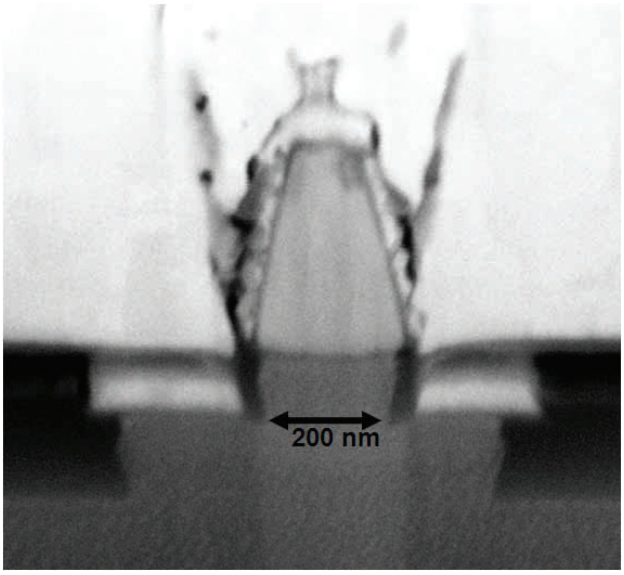


Figure 2: Cross-sectional SEM of emitter and base mesas of HBT with 200 nm wide emitter-base junction. Base + collector epitaxial thickness is 180 nm.

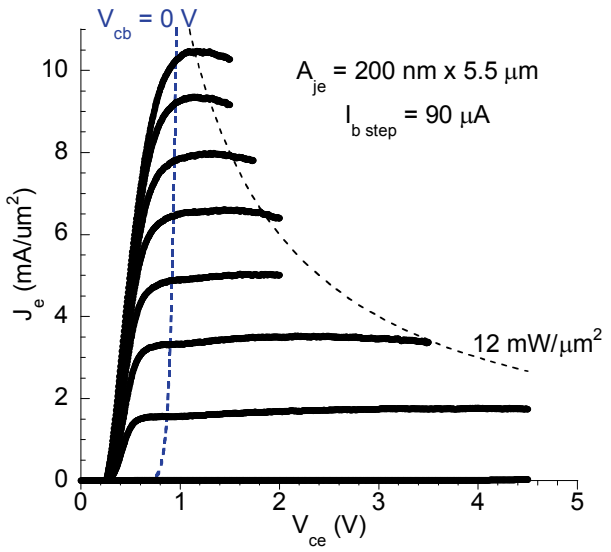
contacts will be deposited. Focused-ion-beam (FIB) cross sections of these devices inspected by SEM reveal emitter-base junctions as narrow as 200 nm, with ~30 nm of emitter mesa undercut, as shown in figure 2.

Remaining fabrication steps include base and collector mesas formed by wet chemical etches, and the base and collector contacts are formed through evaporated metal lift-off. Devices are passivated and the wafer planarized in benzocyclobutene (BCB), which also acts as a low-dielectric-constant spacer (ε_r = 2.7, T_{BCB} = 800 nm) between the device probe pads and the InP substrate.

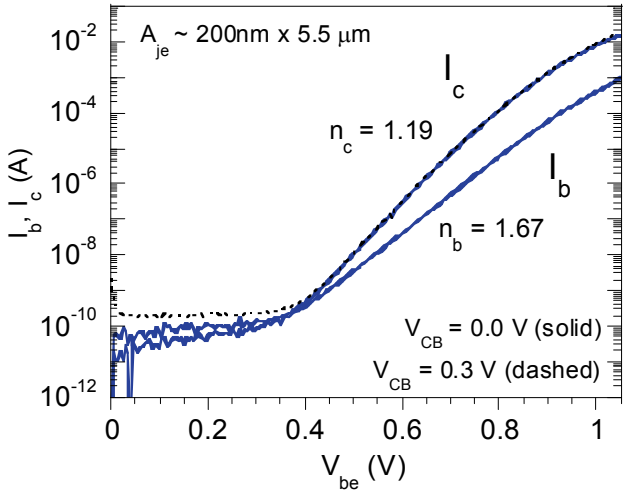
III. Measurements and Results

Standard TLM measurements show base sheet resistance ρ_s = 660 Ω/□ and specific contact resistivity ρ_c = 7 Ω·μm^2. For the collector, ρ_s = 10 Ω/□ and ρ_c = 23 Ω·μm^2. From RF parameter extraction, the emitter specific contact resistivity R_{ex} ≈ 9 Ω·μm^2. Common-emitter and Gummel characteristics are shown in figure 3. DC current gain β = 21 and 33 for 200 nm- and 300 nm-wide devices, respectively. At an emitter current density J_e = 1 kA/cm^2, common-emitter breakdown voltage BV_{ceo} = 4.34 V, and common-base breakdown BV_{cbo} = 4.93 V, while at J_e = 10 kA/cm^2, BV_{ceo} = 5.35 V.

DC to 67 GHz measurements were carried out after performing an off-wafer, probe-tip Line-Reflect-Reflect-Match (LRRM) calibration on an Agilent E8361A PNA. On-wafer, open- and short-circuit pad structures identical to those used by the devices were measured after calibration to de-embed their associated parasitic impedances using established methods [4]. At 67 GHz, the pad shunt conductance was ~0.15 mS and the pad series impedance was ~900 mΩ. Since these pad parasitics contain substantial dissipative as well as reactive elements, stripping them from device data increases the extrapolated f_{max} by ~250 GHz. We believe alternate



(a) Common-emitter characteristics



(b) Gummel characteristics

Figure 3: DC I-V characteristics of a 200 nm HBT

calibration structures will be necessary to accurately measure HBT bandwidths at higher frequencies when f_{max} exceeds 1 THz, and are pursuing alternate on-wafer calibration structures for future work.

Peak RF performance was obtained in a device having emitter junction area A_{je} = 200 nm × 3.5 μm, collector junction area A_{jc} ~ 750 nm × 5.2 μm (A_{jc} / A_{je} ≈ 7.4), at a bias of I_c = 6.96 mA and V_{ce} = 1.71 V (V_{cb} = 0.7 V, J_e = 9.9 mA/μm², C_{cb}/ I_c = 0.41 ps/V). Extrapolations from single-pole, least-squares fits to measured h_{21} and Mason's Unilateral Gain indicate f_τ = 360 GHz and f_{max} > 800 GHz. Determination of f_τ via Gummel's extraction method [5] produces the same result. A small-signal hybrid-π equivalent circuit was generated from RF data, and showed expected reductions in junction capacitances due to lithographic scaling compared to [2].

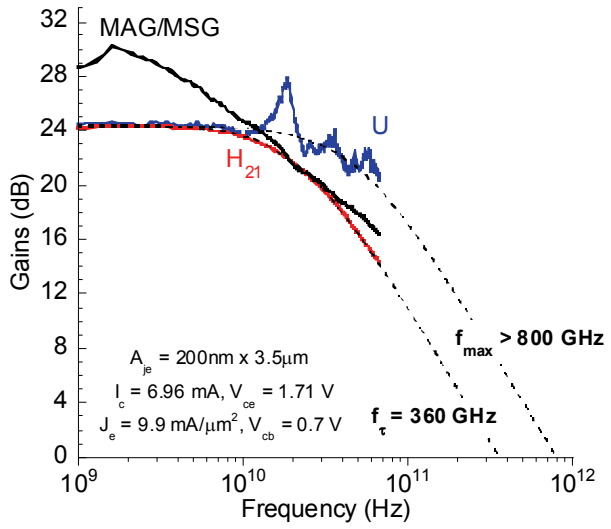
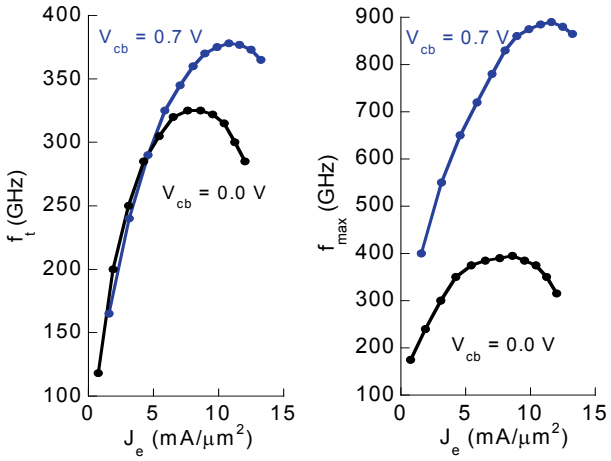


Figure 4: Measured RF gains at peak f_{max} bias point



(a) *(b)*

Figure 5: f_τ (a) and f_{max} (b) dependence on collector-base bias V_{cb} and emitter current density J_e for 200 nm HBT

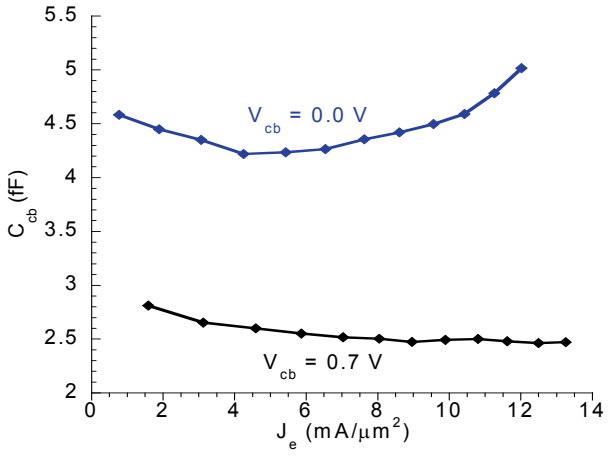


Figure 6: Variation of Ccb with V_{cb} and J_e for HBT with emitter-base junction area A_{je} = 150 nm × 3.5 μm

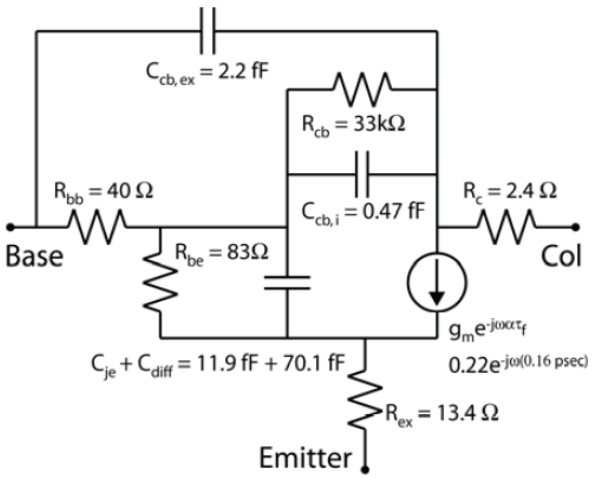


Figure 7: Hybrid-π equivalent circuit at peak RF bias for HBT with A_{je} = 200 nm × 3.5 μm and A_{jc} = 750 nm × 5.2 μm.

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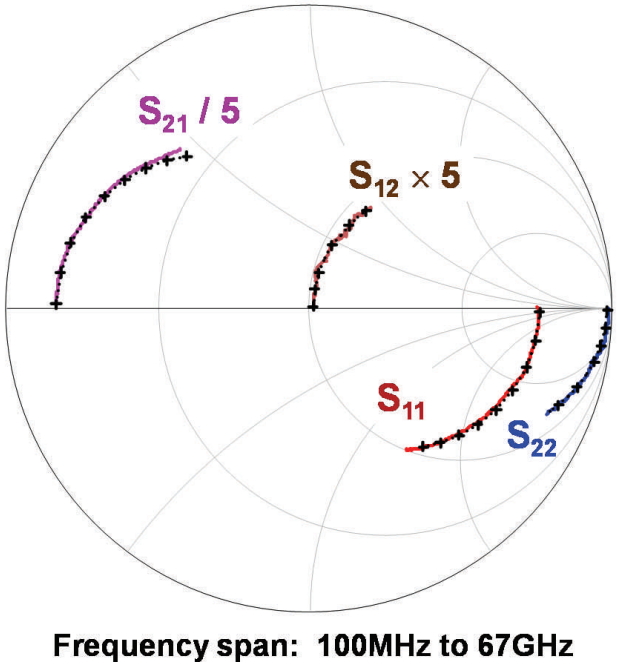

Figure 8: Comparison of measured S-parameter data (solid) and simulated S-parameters from the equivalent circuit model in figure 7 (dotted), at peak RF bias.