0.37 mS/μm $In_{0.53}Ga_{0.47}As$ MOSFET with 5 nm channel and Self-aligned Epitaxial Raised Source/Drain

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InGaAs has been extensively studied as a potential channel material for sub-22nm gate length VLSI MOSFETs because of its low electron effective mass (m^*) hence high electron velocity (v). At sub-22 nm gate lengths, a maximum 1 nm EOT dielectric and 5 nm thick channel with strong vertical confinement are required for high subthreshold slope and acceptably low drain induced barrier lowering (DIBL) [1,2]. Most reported InGaAs MOSFETs [3, 4] have ≥ 10 nm channel thickness. The source/drain (S/D) junctions must be very shallow (~5nm) with abrupt vertical and lateral profiles, yet extremely low (~20Ω−μm) source access resistance and consequently very low (~0.3 Ω−μm^2) contact and (~500Ω) sheet resistivities are required to minimize degradation of the drive current (I_d) and transconductance g_m [1]. Such parameters are difficult to achieve in InGaAs by ion implantation of the N+ S/D , particularly if an InAlAs bottom confinement layer is used. S/D contacts must be self-aligned to the gate, yet there is no known equivalent of self-aligned silicides in III-V materials. Addressing these requirements, we had reported [5, 6] InGaAs MOSFETs with self-aligned S/D access regions and self-aligned metal contacts formed by MBE regrowth and *in-situ* metal deposition, though these showed low 0.02 mS/μm transconductance. Here we report greatly improved devices with 0.37 mS/μm transconductance at 0.8 μm L_g.

Fig. 1 shows the process flow and device schematic cross-section. The device has self-aligned N+ InGaAs S/D regions formed by MBE regrowth, and self-aligned refractory Mo S/D contacts. *In-situ* Mo contacts to regrown InGaAs have shown very low 2.5 Ω−μm contact resistivities [7]. The 5 nm $In_{0.53}Ga_{0.47}As$ channel and an InAlAs bottom barrier were grown by molecular beam epitaxy. To compensate for any surface/interface effects, the InAlAs bottom barrier was pulse doped with Si (Fig. 4). The wafer was capped with arsenic before removal from the MBE chamber. The cap was desorbed *in-situ* in an atomic layer deposition (ALD) chamber at 480 ºC, and 4.7 nm of Al_2O_3 (~ 2.0 nm EOT) deposited. W(50nm)/Cr(50nm)/SiO_2(350nm) gates with L_g=0.3μm–10μm were defined in an alternating dry etch scheme (Fig. 1) minimizing etch damage to the thin channel [5]. A 20 nm SiN_x sidewall was formed by a low power anisotropic RIE etch. The Al_2O_3 dielectric was then selectively wet etched in dilute KOH, stopping on the InGaAs channel. The wafer was then cleaned by exposure to UV-ozone, followed by a 1 minute dilute HCl treatment and a DI rinse. Following cleaning, the wafer was immediately loaded into the MBE chamber and cleaned with atomic H. A (4×2) surface reconstruction was seen in RHEED before regrowth, indicating an epi-ready surface. 50 nm of 4×10^{19} Si doped n^{++} InGaAs was grown at 540 °C by migration enhanced epitaxy. The wafer was then transferred under UHV to an electron beam evaporator and 20 nm of Mo was deposited to form S/D contacts. Because the Mo is also deposited on the gate top surface, the source and drain are short-circuited. The wafer was therefore planarized with photoresist and the Mo on the gate removed with a height-selective etch [8]. S/D pads were then deposited, and devices mesa-isolated. To contact the gates, the silicon dioxide on top of the gate pads was removed by etching in buffered HF.

The cross-section SEM (Fig 5.) shows a slope in the regrowth surface next to gate, but no gap is observed between the N+ regrown material and the gate edge. The regrowth is quasi-selective, i.e. material is deposited on the gate top surface, but there is little growth on the gate sidewalls. The DC characteristics of a 0.8 μm L_g FET (Figs. 5,6) show a maximum 0.95 mA/μm I_d at V_{gs}=3.5 V and V_{ds}=2.0V. The maximum g_m is 0.37 mS/μm at V_{gs}= 0.5V. We believe the gate current (Fig. 7) is dominated by the leakage through the SiN_x sidewalls. From measurements of zero-bias on-resistance (Fig. 8), a 0.50 kΩ−μm source resistance is determined. TLMs patterns on the regrown material located far from MOSFET showed 28 Ω/□ sheet resistance and 12 Ω−μm Mo/InGaAs (lateral) contact resistance. The large discrepancy between the source resistance observed in the FET and lateral access resistance observed in TLM patterns may indicate that the regrown InGaAs close to the gate has higher resistivity than in the far field. MBE is a line-of-sight deposition technique, hence growth adjacent to the gate may be disturbed by shadowing. Possible causes of high source resistance include lack of Si doping next to gate, lattice mismatched growth next to gate causing dislocations which deplete electrons, or high defect density at the regrowth interface. Experiments to evaluate the electrical properties of regrowth next to gate are in progress. Any defects induced at Al_2O_3/InGaAs interface during regrowth will deplete electrons in the channel under the sidewall. This will also increase the source resistance. A recessed S/D regrowth FET (Fig. 9) where the n^{++} regrowth reaches below sidewalls can compensate the defects in the channel under the sidewall and thereby reduce the source resistance.

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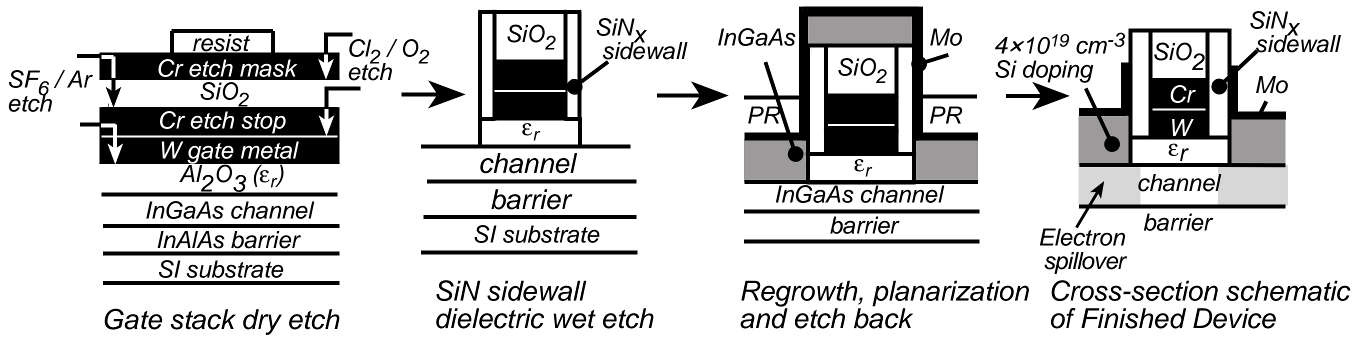

Fig. 1: Schematic of the gate process, regrowth and planarization

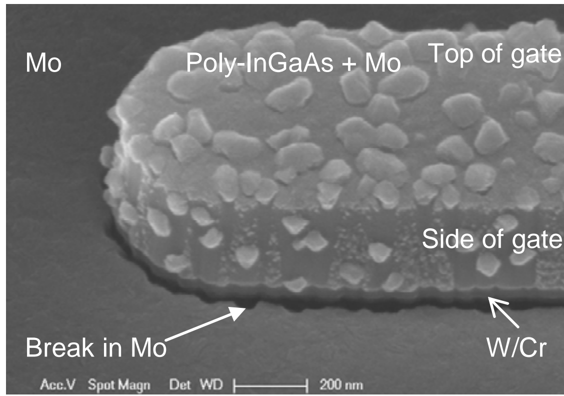

Fig. 2:Oblique view SEM of MOSFET after regrowth and Mo depostion

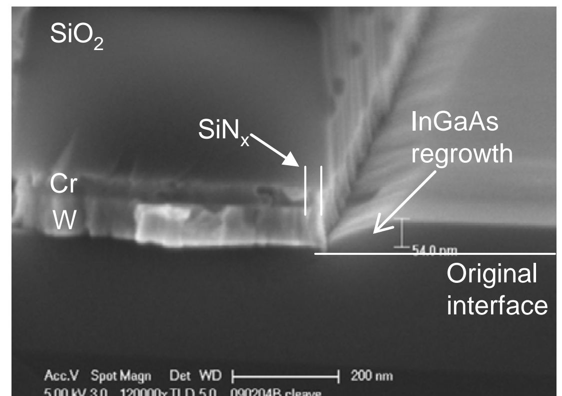

Fig. 3:X-section SEM after regrowth before Mo deposition

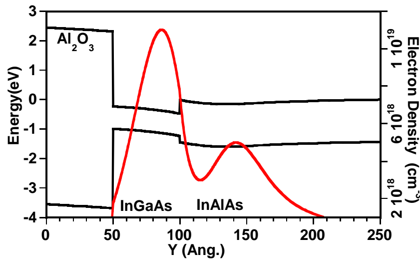

Fig. 4: Band diagram of the MOSFET

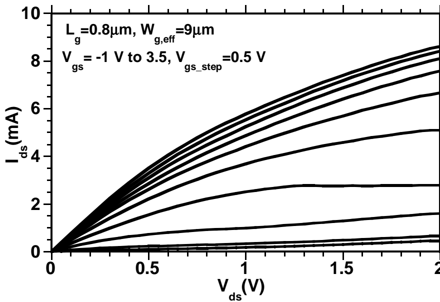

Fig. 5: Output characteristics of L_g=0.8 µm and W_g=9 µm device

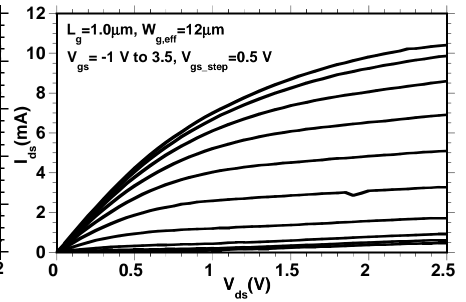

Fig. 6: Output characteristics of L_g=1.0 µm and W_g=12 µm device

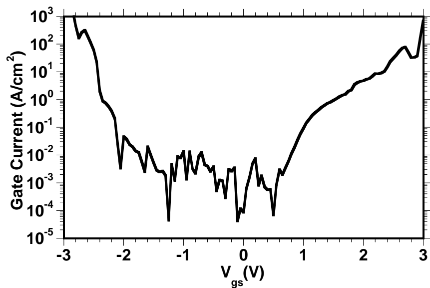

Fig. 7: Measured gate to source leakage

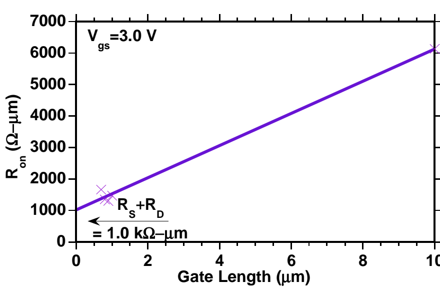

Fig. 8:FET S/D on resistance at Vds=0

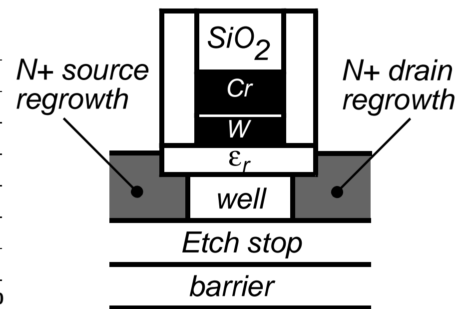

Fig. 9: X-section schematic of recess S/D regrowth FET