Ultralow resistance, nonalloyed Ohmic contacts to *n*-InGaAs

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The authors report ultralow specific contact resistivity (ρ_c) in nonalloyed, *in situ* Ohmic contacts to heavily doped *n*-type $In_{0.53}Ga_{0.47}As:Si$ layers with 6×10^{19} cm^{-3} active carrier concentration, lattice matched to InP. The contacts were formed by depositing molybdenum (Mo) immediately after the $In_{0.53}Ga_{0.47}As$ growth without breaking vacuum. Transmission line model measurements showed a contact resistivity of $(1.1\pm0.6)\times10^{-8}$ Ω cm^2 for the Mo/InGaAs interface. The contacts show no observable degradation in resistivity after annealing at 300 and 400 °C for 1 min duration. © *2009 American Vacuum Society.* [DOI: 10.1116/1.3182737]

I. INTRODUCTION

With the continued scaling of transistors to obtain increased transistor bandwidth and packing density, achieving very low resistance metal-semiconductor contacts becomes crucial. The base and emitter contact resistivities in heterojunction bipolar transistors (HBTs) must decrease in proportion to the inverse square of the transistor cutoff frequency.[1,2] Similarly for field-effect transistors (FETs), progressive reduction in contact resistivity is required for both increased speed of operation and increased device packing density. Contact resistivities less than 1×10^{-8} Ω cm^2 are required for III-V HBTs and FETs for having simultaneous 1.5 THz current-gain (f_τ) and power-gain (f_{max}) cutoff frequencies.[1,2] Owing to higher electron velocity, higher transistor bandwidths are more readily obtained in InGaAs than in Si,[3,4] hence there is strong motivation to develop low resistance Ohmic contacts to InGaAs.

Contact resistivity strongly depends on surface preparation,[5] and obtaining resistivities $<1\times10^{-8}$ Ω cm^2 requires a significant attention to removal of semiconductor surface oxides before the contacts are made. A 4.3×10^{-8} Ω cm^2 contact resistivity to *n*-InGaAs was achieved with Ti/Pt/Au layers by Ar^+ sputter cleaning the semiconductor surface before contact deposition.[6] Ti contacts diffuse[7] into InGaAs at high temperatures and hence can impair reliability,[8] particularly in high-f_{max} devices, where semiconductor junctions typically lie within 20–30 nm of the contact surface. While *ex situ* Ohmic contacts can provide low resistivity, reproducibility is often problematic. Resistivity can be highly sensitive to surface preparation and to the time interval between the surface preparation and metal deposition, factors which may be difficult to control experimentally. *In situ* contact formation prevents surface contamination and oxidation; metal is deposited on the semiconductor immediately after semiconductor growth without exposing the samples to air. Highly degenerate semiconductor doping is also desirable,[9] as this decreases the contact barrier (depletion) depth and increases tunneling probability.

For low resistance Ohmic contacts the Schottky barrier height at the metal-semiconductor interface should be as low as possible. A barrier height of approximately 0.2 eV was predicted from intrinsic interface state theory[10] for metal/*n*-InGaAs contacts. The low Schottky barrier height suggests that it should not be very difficult to prepare low resistivity contacts to nInGaAs. Also, refractory metal can be used for making Ohmic contacts to ensure the thermal stability. Singisetti *et al.*[11] have demonstrated the use of refractory metal, molybdenum (Mo), for making stable *in situ* Ohmic contacts to nInGaAs. Mo has a high (~2623 °C) melting temperature and has an $\sim4.6\pm0.15$ eV work function[12] close to the conduction band edge of InGaAs (electron affinity of ~4.5 eV).

The InGaAs active carrier concentration was 3.5×10^{19} cm^{-3} in the results reported by Singisetti *et al.*[11] for *in situ* Mo contacts. Here we report contact resistivity of *in situ* Mo Ohmic contacts to *n*-InGaAs with increased (6

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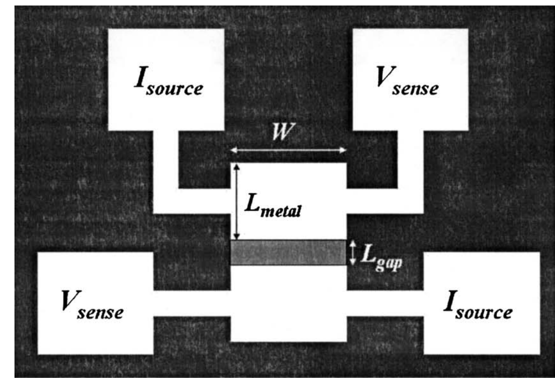
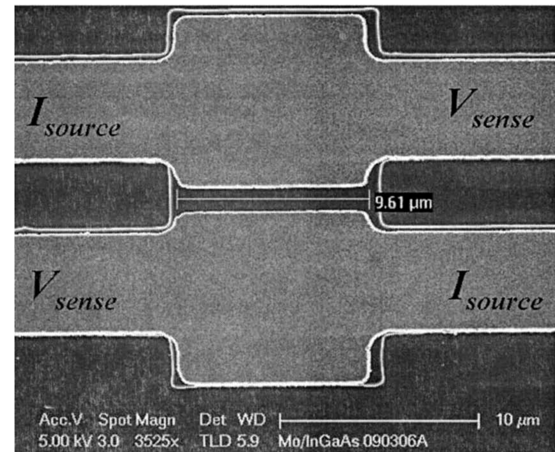
Layer
50 nm ex-situ Ni
150 nm ex-situ Au
20 nm ex-situ Ti
20 nm in-situ Mo
100 nm $In_{0.53}Ga_{0.47}As$:Si, n~$6x10^{19}$ cm^{-3}
150 nm $In_{0.52}Al_{0.48}As$: NID buffer
SI InP Substrate

FIG. 1. Cross-section schematic of the metal-semiconductor contact layer structure used for TLM measurement. The Mo was deposited in an electron beam deposition system connected to MBE under ultrahigh vacuum. Ti/Au/Ni is deposited by *ex situ* sputtering.



(a)



(b)

FIG. 2. (a) Schematic of the TLM pattern used for the contact resistivity measurement. Separate pads were used for current biasing and voltage measurement; (b) magnified SEM image of the TLM pattern with 10 μm width and 800 nm gap.

$\times 10^{19}$ cm^{-3}) active carrier concentration achieved by low temperature (420 °C) InGaAs growth with a high (100:1) V/III flux ratio. The observed contact resistivity was $(1.1 \pm 0.6) \times 10^{-8}$ Ω cm^2.

II. EXPERIMENTAL PROCEDURE

The semiconductor epilayers were grown by a Gen II solid source molecular beam epitaxy (MBE) system. A 150 nm undoped $In_{0.52}Al_{0.48}As$ layer was grown on a semi-insulating InP (100) substrate, followed by 100 nm of silicon doped $In_{0.53}Ga_{0.47}As$. Six samples were grown at 440 °C substrate temperature, with the Si cell temperature varying from 1246 to 1348 °C. A single sample was grown at 420 °C substrate temperature and 1348 °C Si cell temperature. After the InGaAs growth, the wafer was cooled and transferred under UHV to an electron beam evaporator chamber, where 20 nm of molybdenum (Mo) was deposited on half the wafer through a shadow mask. The active carrier concentration, mobility, and sheet resistance were obtained from Hall measurements by placing indium (In) contacts on samples taken from the half of the wafer not coated with Mo. The portion of the wafer coated with Mo was processed into transmission line model (TLM) structures for contact resistance measurement. Doping concentration was thus measured on pieces of the same growth samples as those used for resistance measurement; this avoids experimental errors resulting from variation in doping concentration between growth samples.

For the TLM structures, as shown in Fig. 1, Ti/Au/Ni contact pads were patterned on the samples coated with Mo using in-line optical photolithography and lift-off after a single pump-down e-beam deposition of 20 nm Ti, 150 nm Au, and 50 nm Ni. Mo was then dry etched in a SF_6/Ar plasma using Ni as an etch mask. The TLM structures were then isolated using mesas formed by photolithography and a subsequent wet etch. A schematic of the TLM pattern is shown in Fig. 2(a).

Resistances were measured using the TLM method,[12] a four-point (Kelvin) probe technique, and an Agilent 4155C semiconductor parameter analyzer. The TLM contact geometry was designed to measure contact resistivities of the order of 1 Ω μm^2. Kelvin probing measures only that fraction of the resistance within the circuit branch shared between the current biasing contacts and the voltage measurement contacts; for each TLM contact pad, separate probe contact pads are provided for current biasing and for voltage measurement, with approximately 10 μm shared path length on the *IC* interconnects [Fig. 2(b)]. Contact separations were varied from 500 nm to 25 μm. This ensures that lateral contact resistance is at least 40% of the total measured resistance at the smallest contact separation. At large contact separations, sheet resistance term dominates. After processing, the TLM pattern lengths and widths were verified using a scanning electron microscope (SEM). The *n*+ layers are kept thin, at ~100 nm, to reduce the spreading resistance contribution from two-dimensional current flow within the semiconductor. In the evaluation of contact resistance measurement methods of Ref. 13, the TLM method was found to be the most precise.

The measured sheet and contact resistivities are small, hence the effects of metal interconnect resistance must be considered in determining the true contact resistivity. In the Kelvin probing structure [Fig. 2(a)], both hand analysis and numerical finite-element analysis indicate that the observed resistance is $R_{measured} = 2\rho_c / W L_T + \rho_s L_{gap} / W - \rho_m W / 3 L_{metal} T_m$,

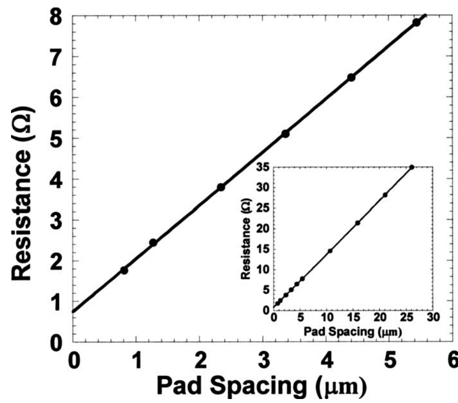


FIG. 3. Measured TLM resistance as a function of pad spacing for *in situ* molybdenum Ohmic contacts on *n*-InGaAs. The inset plots measured TLM resistance vs pad spacing ranging from 0.8 to 27 μm.

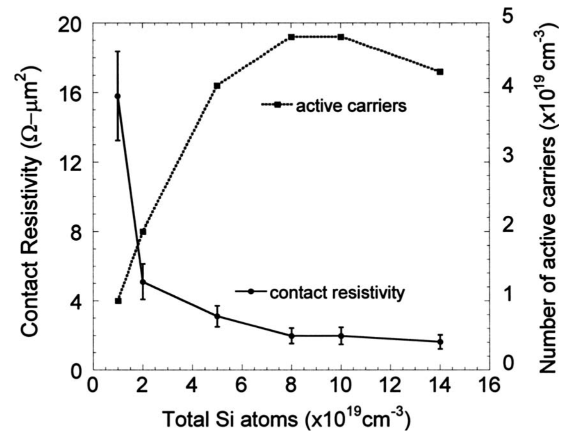


FIG. 4. Variation of contact resistivity and number of active carriers with total number of Si dopants. Error bars are indicated on the respective contact resistivity values.

where ρ_c is the metal-semiconductor contact resistivity, ρ_s the semiconductor sheet resistivity, $L_T=\sqrt{\rho_c/\rho_s}$ is the transfer length, ρ_m the bulk metal resistivity, and T_m the contact metal thickness. The dimensions W, L_{gap}, and L_{metal} are defined in Fig. 2(a). Note that a term $\rho_m W/3L_{\text{metal}}T_m$ involving the metal bulk resistivity must be *added* to the measured resistance in order to correctly extract the data; to determine the magnitude of this term ρ_m is separately measured using on-wafer test structures, and the relative magnitude of this correction term is made small by restricting W to at most 10 μm. This metal resistance correction was not included in the earlier reported data of Singisetti *et al.*,[11] and the contact widths were larger (W=25 μm); the present publication both extends the reported contact resistivities to higher Si dopant concentration and corrects the Mo/InGaAs contact resistivities reported in Ref. 11.

Extraction of the specific contact resistivity ρ_c from the observed lateral access resistivity ρ_H and semiconductor sheet resistivity ρ_s is only accurate if the semiconductor sheet resistivity in regions below the Ohmic contacts is the same as that in the space between the contacts. In the fabrication of the TLM test structures reported here, the surface of the semiconductor between the contacts is exposed to the SF_6/Ar plasma dry etch which removes the Mo contact metal. To verify that this exposure does not significantly change the sheet resistance, two InGaAs samples were grown by MBE. 14.1 Ω sheet resistance was immediately measured by Hall method on the control sample. On the second (test) sample, *in situ* Mo was first deposited by evaporation and removed by SF_6/Ar plasma dry etching; this showed 14.5 Ω sheet resistance.

III. RESULTS AND DISCUSSION

The variation in TLM test structure resistance with contact separation is shown in Fig. 3. This sample was grown at 420 °C substrate and 1348 °C Si cell temperature. Using the methods of Ref. 14, we find a $(1.1\pm0.6)\times10^{-8}$ Ω cm^2 specific contact resistivity (ρ_c) and 13.2 Ω sheet resistivity (ρ_s). The transfer length is 280 nm, 2.8:1 larger than the N+ layer thickness, hence resistance analysis assuming one-dimensional current flow is appropriate. Hall measurements on the sample indicate 6.0×10^{19} cm^{-3} active carrier concentration, 740 cm^2/V s mobility, and 14.1 Ω sheet resistivity, correlating closely to the sheet resistivity determined from TLM measurements.

Figure 4 shows specific contact resistivity and the total active carrier concentration as a function of the total incorporated Si dopant concentration. These $In_{0.53}Ga_{0.47}As$ samples were grown at 440 °C substrate temperature. For dopant concentrations below 8×10^{19} cm^{-3}, active carrier concentration increases with increased Si dopant concentration, while contact resistivity decreases rapidly. For 440 °C growth, the lowest observed contact resistivity was $(1.6\pm0.9)\times10^{-8}$ Ω cm^2 for an active carrier concentration of 4.2×10^{19} cm^{-3}. Note that the contact resistivity obtained by Singisetti *et al.*[11] was $(2.0\pm0.9)\times10^{-8}$ Ω cm^2 (after correcting for metal resistance) for an active carrier concentration of 3.5×10^{19} cm^{-3}. InGaAs was grown at 460 °C for these samples.

Noting that the lowest contact resistivity, $(1.1\pm0.6)\times10^{-8}$ Ω cm^2, was obtained at the highest active carrier density (6×10^{19} cm^{-3}, 420 °C growth), we speculate that increasing the ionized donor concentration decreases the Schottky barrier thickness, increasing the probability of tunneling through the junction.

The samples were annealed under N_2 flow for 1 min at 300 and 400 °C to study contact thermal stability. Contact current-voltage characteristics remain linear after annealing, and the observed variation in contact resistivity was less than the margin of error in measurement.

IV. CONCLUSIONS

In conclusion, we report a contact resistivity of $(1.1\pm0.6)\times10^{-8}$ Ω cm^2 obtained with *in situ* Mo Ohmic contacts to heavily doped *n*-InGaAs. The data suggest that the observed low contact resistivities result from high carrier concentration and from a metal-semiconductor interface free of oxides and other contaminants. The contacts are thermally stable for anneal to as much as 400 °C.

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