Improved Migration-Enhanced Epitaxy for Self-Aligned InGaAs Devices

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Parasitic contact and access resistances limit the bandwidth of high speed electronic and optoelectronic devices. Molecular beam epitaxy can provide very highly doped layers and in-situ Mo deposition for low resistance contacts [1]. But regrowth of contacts next to a finished device often results in undesirable gaps. On the other hand, self-aligned contacts provide the shortest electrical path from external contacts to a device, and they require no critical lithography.

In this study, we examine regrowth of n^{++} InGaAs for self-aligned contacts next to SiO_2 gate structures as a function of temperature, V/III ratio, and pulsed deposition. Growth is challenging because Si doping above $5x10^{19}$ cm^{-3} is required for contact resistances below 10^{-8} Ω-cm^2, but this produces either extremely rough films or gaps near the gate, depending on temperature.

On the other hand, a modification of migration-enhanced epitaxy (MEE) at high temperature with continuous arsenic flux produced smooth films. Single monolayers of Group III atoms were deposited with a flux ratio V/III~3, separated by a 15 sec soak under a 2-$5x10^{-6}$ torr As_2 flux. At temperatures below 520 °C, significant crosshatching occured near the gate, which we attribute to preferential migration of In from the SiO_2 to the substrate, resulting in compressive strain and relaxation. Growth at 540-560 °C does not show significant relaxation roughening in SEM. Indium evaporation at these temperatures requires 10-34% additional indium to maintain lattice-matched conditions. In contrast to Shen's results on InAs [2], we find that increasing substrate temperature leads to [111] faceted growth rather than a uniform "rising tide." Growth at 540 °C with alternating 4x2 - 3x1 - 4x2 RHEED patterns produced films which were both smooth in the far field and showed no apparent gap near the gate.

High levels of silicon doping ($8x10^{19}$ cm^{-3}) initially raised two concerns. First, Si concentrations are well above the solid solubility limit in InGaAs. MEE provides increased time for relaxation processes to occur during growth, and the high temperatures tend to drive toward thermodynamic limits. Second, Si is only a donor when sitting on a Group III lattice site, but MEE creates Group III-rich surfaces. However, electron concentrations as measured by Hall were virtually identical whether the Si was provided simultaneously with Group III atoms or in the middle of the As soak. It appears that Si preferentially takes surface Group III sites even on an arsenic-poor surface.

Using these self-aligned regrowth techniques, we have fabricated the first III-V MOSFETs with self-aligned regrowth of source-drain contacts. These techniques will enable lateral scaling of future III-V MOSFETs and HEMTs to tens of nanometers.

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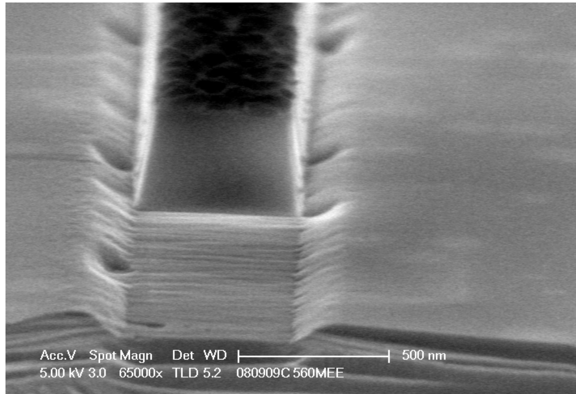
[1] U. Singisetti, et al., *Appl. Phys. Lett.*, **93**,183502 (2008).

[2] X. Q. Shen, et al., *J. Cryst. Growth* **146**, 374 (1995)



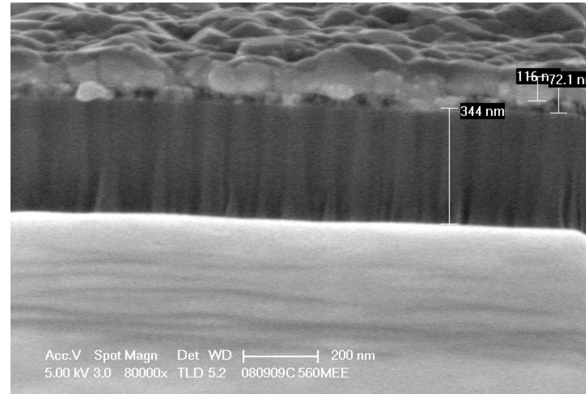


Fig. 1. Migration-enhanced epitaxial regrowth next to SiO2 dummy gate at 560 °C. (left) End view with part of gate removed, showing (111) faceted growth up to gate. (right) Side view showing clean sidewalls.

	[Si] (cm^{-3})	n (cm^{-3})	μ ($cm^2V^{-1}s^{-1}$)
Conventional MBE	$8x10^{19}$	$4.8x10^{19}$	847
Si during Group III pulse	$8x10^{19}$	$4.3x10^{19}$	1258
Si during As soak	$8x10^{19}$	$4.2x10^{19}$	1295

Fig. 2. Hall measurements of samples grown by conventional MBE (nonstop) and MEE.

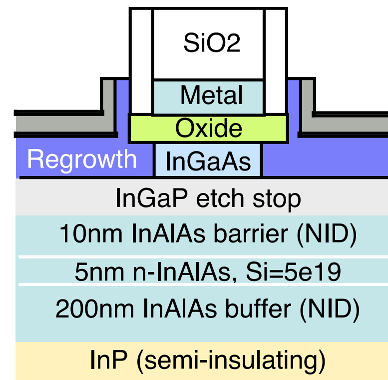
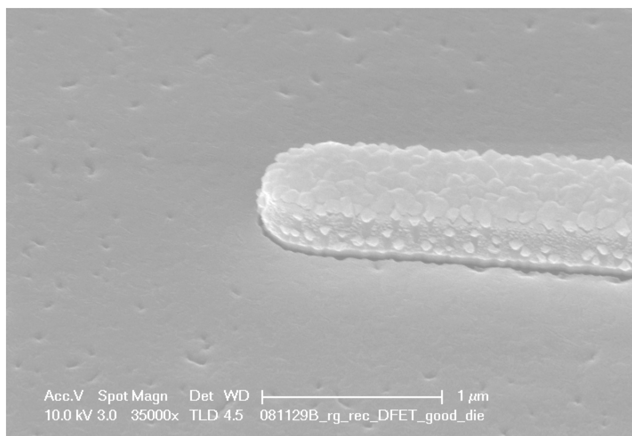


Fig. 3. Depletion-mode InGaAs MOSFET structure (not to scale).



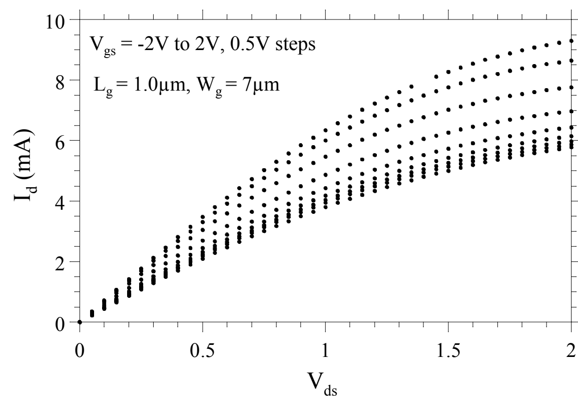


Fig. 3. Depletion-mode InGaAs MOSFET. (Left) Oblique view SEM after InGaAs regrowth and in-situ Mo deposition, before mesa isolation. (Right) Id-Vds. High off-state currents are due to conduction through the doping layer, which is 17 nm away from the gate.