TRANSFERRED-SUBSTRATE InP/InGaAs/InP DOUBLE HETEROJUNCTION BIPOLAR TRANSISTORS WITH f_{max}=425 GHz

S. Lee, H. J. Kim, M. Urteaga, S. Krishnan, Y. Wei, M. Dahlström and M. Rodwell

Department of ECE, University of California, Santa Barbara, CA 93106

Abstract **-- We report InP/InGaAs/InP Double Heterojunction Bipolar Transistors (DHBT) with f_{max} = 425 GHz and f_{τ} = 141 GHz using transferred-substrate technology. This is the highest reported f_{max} for a DHBT. The breakdown voltage BV_{CEO} is 8 V at J_C = 5 ×10^4 A/cm^2 and the DC current gain β is 43.**

I. INTRODUCTION

Very wide bandwidth Double Heterojunction Bipolar Transistors (DHBT) will enable high-power amplifiers at 94 and 180 GHz, microwave analog digital converters, microwave direct digital frequency synthesis, fiber optic transmission at >40 Gb/s and wireless data networks at frequencies above 100 GHz.[1]

InP/InGaAs/InP DHBT with record f_{max} = 425 GHz have been fabricated using transferred substrate method.[2] Transferred substrate single heterojunction bipolar transistors (SHBTs) have demonstrated very high bandwidth and are potential candidates for very high speed integrated circuit applications.[2,3]. The transferred substrate SHBTs, however, have very low breakdown voltage, BV_{CEO} ~ 1.5 V. This letter reports a InP/InGaAs/InP transferred substrate DHBT with record f_{max} and a high breakdown voltage, BV_{CEO} = 8 V at J_C ~ 5×10^4 A/cm^2.

Extrapolating at 20dB/decade, the power gain cut-off frequency f_{max} = 425 GHz and the current gain cut-off frequency f_{τ} = 141 GHz. The record f_{max} results from the scaling of HBT emitter and collector junction widths.

II. EPITAXIAL STRUCTURE AND FABRICATION

Table. I shows the MBE grown layer structure. As heat flows through the emitter, a thin 300 Å InGaAs emitter contact layer was used for low thermal resistance. We used compositionally graded InGaAs/InAlAs layers at each interface between InP and InGaAs layers. The base layer is 400 Å thick and is Be-doped at 4×10^{19}/cm^3. To reduce the base transit time, we designed the base layer with 50 meV band gap grading, introduced by varying the Ga:In ratio.

Layer	Material	Doping	Thickness (Å)
Emitter Cap	InGaAs	1×10^{19} : Si	300
Grade	InGaAs/ InAlAs	1×10^{19} : Si	200
N^{++} Emitter	InP	1×10^{19} : Si	900
N^{-} Emitter	InP	8×10^{17} : Si	300
Grade	InGaAs/ InAlAs	8×10^{17} : Si	233
Grade	InGaAs/ InAlAs	8×10^{17} : Be	67
Base	InGaAs	4×10^{19} : Be	400
Grade	InGaAs/ InAlAs	1×10^{16} : Si	480
Delta Doping	InP	1.6×10^{18} : Si	20
Collector	InP	1×10^{16} : Si	2500

Table I - Layer structure of MBE grown InP/InGaAs/InP DHBT

The 0.5×8 μm^2 emitter contact metal was defined by optical projection lithography. The emitter-base mesa was formed by selective wet etching and nonselective citric-based wet etching. Undercutting of the emitter metal during emitter etching results in a ~0.4×7.5 μm^2 emitter junction area. Subsequent steps are similar to [2]. Selective wet etching was used for base mesa isolation. The 1.2×8.75 μm^2 Schottky collector contact was made on a 3000 Å thick InP collector layer after removing the S.I. InP substrate.

I. Results

Fig. 1 shows the common emitter DC characteristic of a device with 0.5×8 μm^2 emitter and 1.2×8.75 μm^2 collector mask dimensions. The offset

voltage was 0.2 V and $V_{ce,sat}$ was 1 V as shown in Fig. 1(a), while the DC current gain β = 43. Fig. 2 (b) represents the BV_{CEO} for a typical device with the same junction dimensions. The BV_{CEO} = 8 V at $J_C \sim 5 \times 10^4$ A/cm^2.

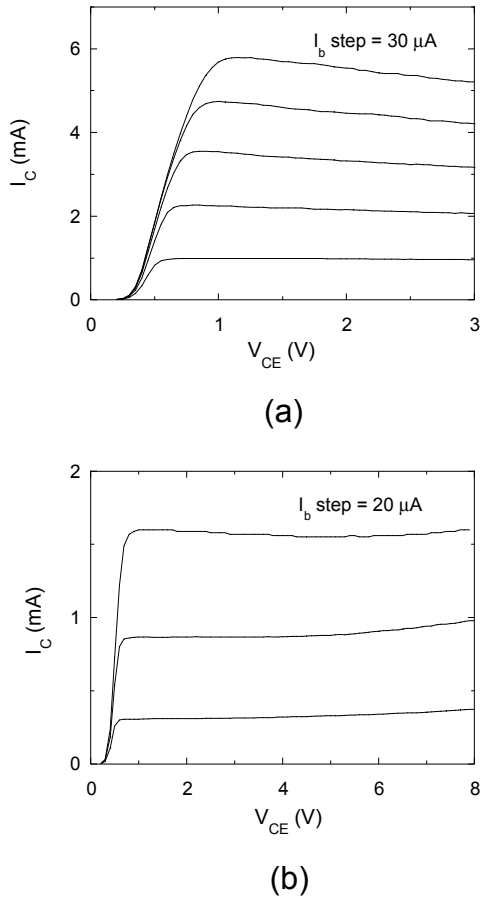

Fig. 1. – Common Emitter DC characteristics of 0.5×8 μm^2 emitter and 1.2×8.75 μm^2 collector devices. (a) I_b step = 30 μA and DC gain β = 43 and (b) I_b step = 20 μA and BV_{CEO} = 8 V at $J_c \sim 5 \times 10^4$ A/cm^2

Fig 2 shows the RF characteristics of the device of which DC data was shown in Fig. 1(a) The devices were characterized by on-wafer network analysis from 1 - 45 GHz and 75 - 110 GHz. The cut-off frequencies f_τ = 139 GHz and f_{max} = 425 GHz were measured at I_C = 4.5 mA and V_{CE} = 1.9 V (Fig. 2). With high-f_{max} HBTs, C_{cb} is low, resulting in a low reverse transmission S_{12}. Small measurement errors in S_{12} arising from parasitic probe-probe electromagnetic coupling then result in significant measurement errors in determination of the transistor C_{cb} and f_{max}. To obtain accurate measurements, the network analyzer was calibrated with on-wafer line-reflect-line (LRL) microstrip calibration standards. Reference planes are offset from the probe pads by 230 μm, resulting in a minimum 460 μm probe-probe separation, and reduced probe-probe coupling.

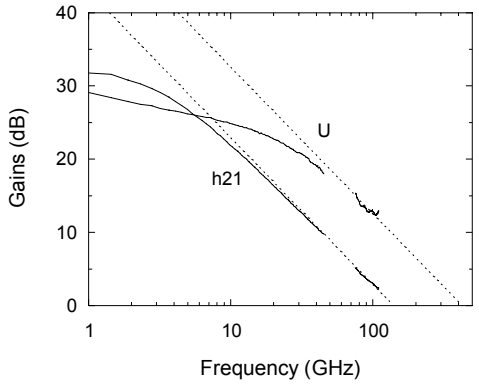

Fig. 2 - Small signal current and power gains vs. frequency at I_C = 4.5 mA and V_{CE} = 1.9 V

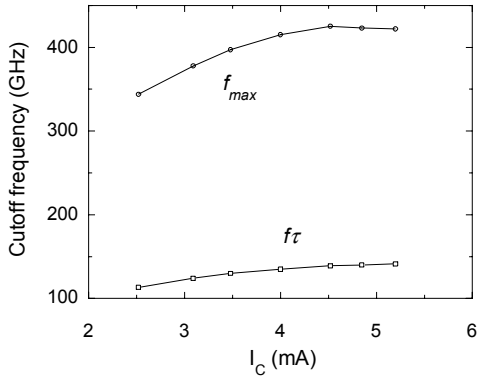

Fig. 3 - Variation of f_τ and f_{max} with collector current at V_{CE} = 1.9 V

Fig. 3 shows the collector current dependence on cut-off frequencies. The highest f_τ =141 GHz was measured at I_C = 5.2 mA and V_{CE} = 1.9 V. Because of the offset-reference-plane on-wafer LRL calibration, the 1 - 45 GHz data is well matched to the 75 - 110 GHz data and gain slopes are close to the expected -20 dB/decade.

III. SUMMARY

We have demonstrated InP/InGaAs/InP double heterojunction bipolar transistor with record f_{max} = 425 GHz using transferred substrate technology. Measured DC gain was 43. RF characteristics were

successfully measured for 1 – 45 GHz and 75 – 110 GHz frequency range with on wafer LRL calibration method.

For further improvement on f_{max}, it is feasible to adopt carbon doped base at $>10^{20}/cm^3$, improving both the base sheet and contact resistance. Also, the improved design of the collector-base grade should improve the transistor f_τ.

ACKNOWLEDGMENT

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