A 204.8GHz Static Divide-by-8 Frequency Divider in 250nm InP HBT

Zach Griffith, Miguel Urteaga, Richard Pierson, Petra Rowell, Mark Rodwell, and Bobby Brar

***Abstract*—We present a static divide-by-8 frequency divider with a record maximum clock frequency of 204.8GHz, designed and fabricated using 250nm InP HBTs (400GHz f_τ, 650GHz f_{max}) with a 4-metal layer, inverted thin-film microstrip wiring environment. The divider is fully static down to 4.0GHz operation. The total power dissipation is 1.82W, of which 592mW is consumed by the input-stage divider. The divider latches are formed using emitter-coupled-logic (ECL), and inductive peaking is used in series with the load resistance R_L to minimize gate delays for highest possible divider clock rates. The circuit contains 108 HBTs and its size is 0.68×0.45-mm^2.**

***Index Terms*—Static Frequency Divider, Divide-by-8, 250nm InP HBT**

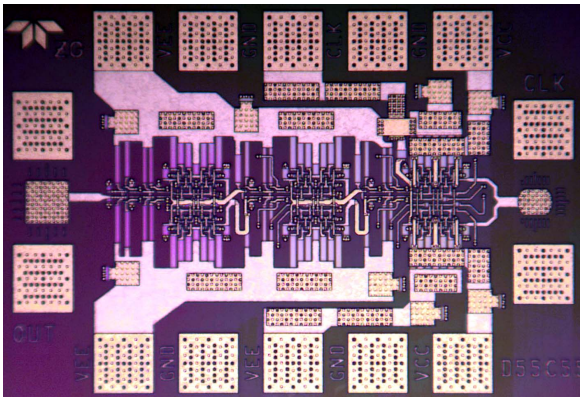

Fig. 1. IC micrograph of the static divide-by-8 frequency divider (prior to top-most metal deposition). Die area, 0.68×0.45 mm^2.

I. Introduction

InP based double heterojunction bipolar transistors (DHBT) have been aggressively pursued because of their superior material transport properties compared to SiGe. This is demonstrated by the increased value of small-signal unity current gain f_τ and unity power gain f_{max} that InP devices possess over SiGe at a given scaling generation. The gate delay of a digital IC in contrast is not determined by an algebraic function of f_τ and f_{max}, but instead by a set of time constants of which $C_{cb}\Delta V_{logic}/I_c$ is a majority contributor. For a given technology, the maximum clock rate of a static frequency divider is used as a digital benchmark circuit as it reflects the highest data rate a latch may support in a digital IC. In order to increase the bandwidths of this circuit, lateral device scaling is required to reuce the total base-collector capacitance (C_{cb}), done simultaneously with reductions to the HBT contact resistances, as well as forming the IC with reduced signal path lengths. At Teledyne Scientific, recent fabrication advancements and process developments have made possible InP HBTs having 250nm features with the requisite features to support our efforts towards 200GHz digital clock rates.

We report here a static divide-by-8 frequency divider operating to f_{clk} = 204.8GHz in 250nm InP HBT – this is the highest reported frequency operation for such a circuit. The devices showed peak figures-of-merit of 400GHz f_τ and 650GHz f_{max}. At a bias associated with 204.8GHz operation, the circuit is fully static down to 4.0GHz f_{clk}. The entire divide-by-8 consumes 1.82W, of which 592mW is dissipated by the input divider (no buffers included) operating at the highest clock rate, and employs 108 HBTs. Increases to the divider clock rate compared to [1] are due to aggressive lateral device scaling, reductions to the transistor parasitic contact resistances, and a 50% reduction of the divider signal path lengths.

II. Device Design and Technology

The HBT structure is grown using molecular beam epitaxy (MBE) on 4-inch semi-insulating InP substrates. The emitter contact is patterned by electron-beam lithography (EBL) and formed using a Au-based electroplating process. An initial benzocyclobutene (BCB, ε_r = 2.7) spin is used to passivate transistors and planarize the wafer. An RIE etchback of the BCB is performed to requisite thickness. Vias are pattern-etched to access the HBT terminals and thin-film-resistor (TFR, 50Ω/sq) contacts. The first layer of metal interconnect (and subsequent interconnect layers) is patterned and formed

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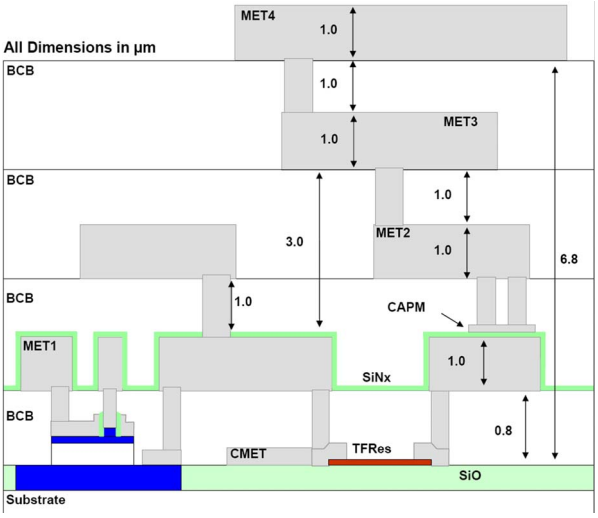


Fig. 2. Cross-section of the TSC mixed-signal InP HBT process with multiple-interconnect layers formed by BCB ($\varepsilon_r = 2.7$).

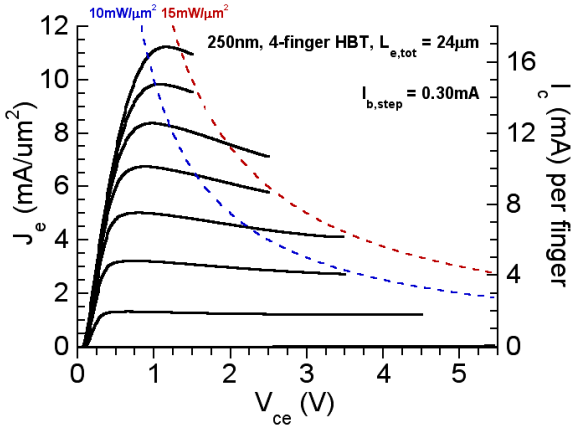


Fig. 3. Common-emitter characteristics – 4-finger, 250nm × 6um HBT.

by Au-based electroplating, providing electrical contacts to the HBT and TFR. The inter-metal interconnect separation by BCB is 1 µm. MIM capacitors (SiN_x, 0.3fF/µm^2) are formed between the first and second level interconnect metal. A technology cross-section of the Teledyne Scientific mixed-signal InP HBT process is shown in figure 2, where further details can be found in [2].

The HBT epitaxy utilizes a 30nm carbon-doped base layer and a 150nm InP collector region. The collector design is described in detail in [3]. Common-emitter characteristics for a 4-finger, 250nm × 6µm HBT is shown in figure 3. Unlike measurements of a single device, this fine-pitch multi-finger HBT with 6µm finger separation captures the effects of device self-heating similar to those experienced by HBTs closely spaced in a digital latch. The RF figures-of-merit for this device show peak 400GHz f_τ and 650GHz f_{max} at J_e = 9.5mA/µm^2 and V_{ce} = 1.6V.

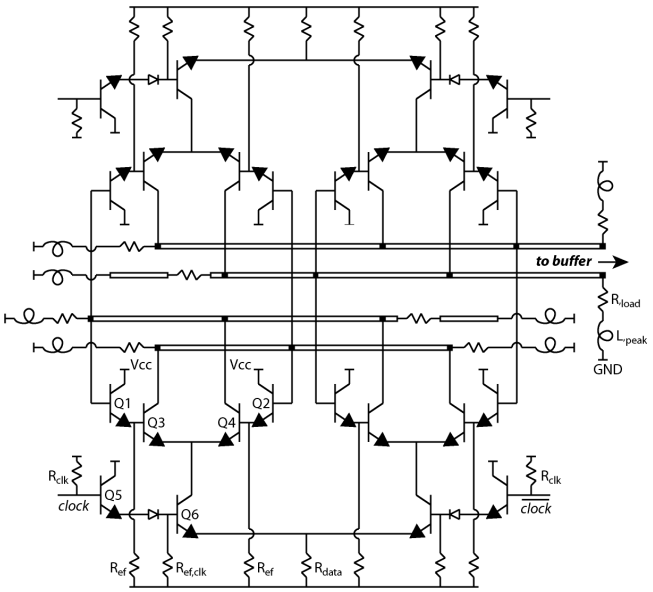


Fig. 4. Circuit schematic of the emitter-coupled-logic (ECL) flip-flop configured as a static divide-by-2 frequency divider.

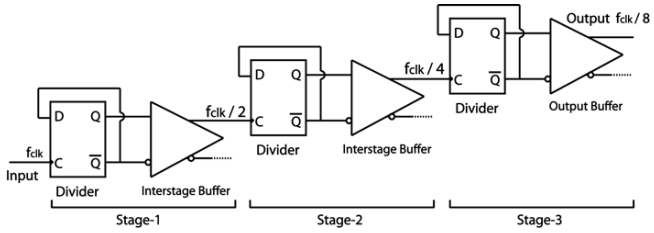
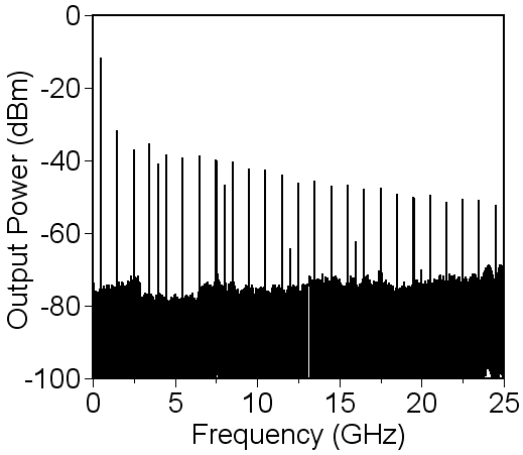


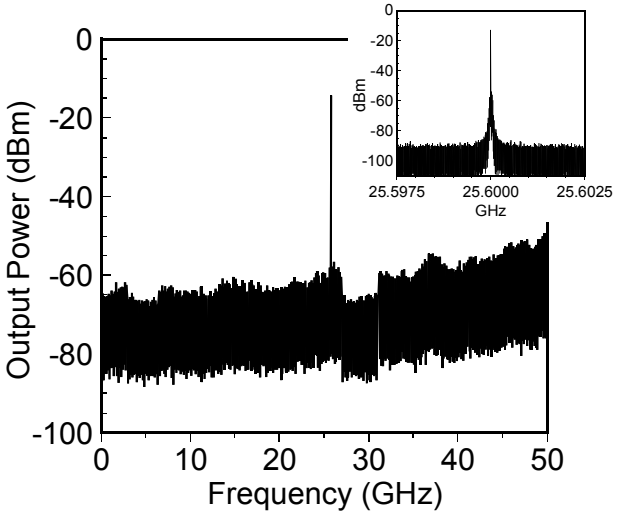
Fig. 5. A top-level block diagram of the static divide-by-8 frequency divider.

III. CIRCUIT DESIGN

The circuit consists of a master-slave flip-flop with the output cross-coupled to the input to generate $f_{clk}/2$ frequency division of the clock signal, shown in figure 4. Two-stages of differential output signal buffering are used to keep small capacitive loading on the signal bus from subsequent circuitry. To form the divide-by-8 output of the input clock signal, three dividers are cascaded together – a top-level schematic is shown in fig. 5. All flip-flops employ single-buffered emitter-coupled-logic (ECL). Bias currents are established using pull-down resistors, rather than current mirror HBTs, to avoid capacitive loading by such devices. For the input-stage divider only, the collector terminal of emitter-followers Q1-Q2 may be biased to a voltage $V_{CC} > 0$V to minimize their base-collector capacitance C_{cb} and reduce their delays. The first divider (stage-1) is composed of 4µm long (L_e) HBTs for Q1-Q2 and Q3-Q4, and 6µm HBTs for Q5-Q6 – all 250nm in width. The second and third divider stages all employ 250nm × 5µm HBTs. The switching paths of the signal bus are only 50µm in length (located at the center of the IC) – doubly terminated with 50Ω resistors and 22pH of peaking inductance. Interconnects are formed using inverted thin-film microstrip,



(a) Divider output, f_{clk} = 4.0GHz, f_{out} = 500MHz



(b) Divider output, f_{clk} = 204.8GHz, f_{out} = 25.60GHz

Fig. 6. Output spectrums for the static divide-by-8 frequency divider at the lowest (4.0GHz) and highest (204.8GHz) achievable toggle rate. Measurements were performed at identical bias conditions: V_{EE} = -3.8V, $I_{EE,tot}$ = 463mA, V_{CC} = 0.5V

where the top-most metal layer acts as the ground plane. An IC micrograph of the fabricated static divide-by-8 frequency divider (ground plane omitted) is shown in figure 1. The circuit employs 108 HBTs and its dimensions are 0.68×0.45 mm^2.

IV. TEST AND MEASUREMENT

Divide-by-8 measurements for clock frequencies spanning the divider limits were performed, where the clock signal is presented single-ended (not differential, 50Ω input matched) to the circuit and an input clock DC voltage offset of -450mV (Q5, fig. 4) is required. The bias voltage for all stages (dividers and buffers) is V_{EE} = -3.8V, and $I_{EE,total}$ = 463mA. V_{CC} for the input divider is 500mV. The measured bias current from an input-stage latch $I_{EE,latch}$ = 70mA. The overall DC

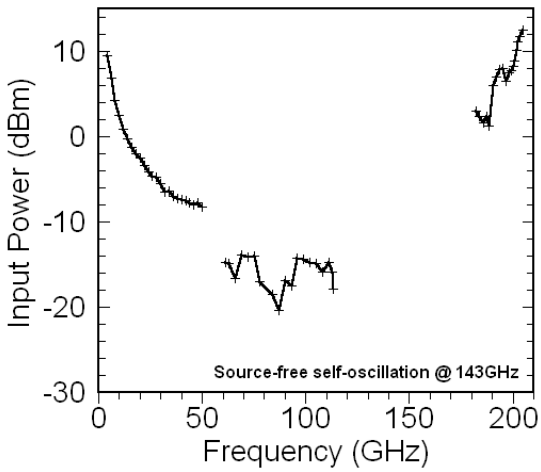


Fig. 7. Input sensitivity with frequency for the 204.8GHz static divide-by-8 frequency divider.

power for the divide-by-8 is 1.82W, where 592mW is associated with the input divider only (no output buffers). All measurements were performed at room temperature ~ 25°C and at identical biases across the measurement bands. At low-frequencies, a DC-50GHz synthesizer directly drives the clock input. The divider was clocked as low as 4.0GHz (P_{clk} = 9.0mW) to demonstrate that it is fully static; the output spectrum is shown in figure 6(a). Also note for this input frequency, the output stage divider is operating at a lower 1.0GHz clock signal (350mV$_{p\text{-}p}$ differential drive). For 61.5-113.25GHz measurements, the synthesizer drives a frequency tripler and the signal is delivered on wafer though a GGB WR-10 waveguide coupled probe. For 160-175GHz measurements, the synthesizer drives a Virginia Diodes (VDI) 12× frequency extension module. The output is adapted through a WR-06 to WR-05 transition, passes through an Aerowave WR-05 mechanical waveguide attenuator, and is delivered on-wafer through a WR-05 waveguide coupled probe. For 181.6-210GHz measurements, the synthesizer drives a VDI 8× frequency extension module, where the output passes through the same WR-05 waveguide attenuator and WR-05 probe before reaching the divider. The maximum clock rate achievable is 204.8GHz for a P_{clk} = 17mW; the output spectrum from DC-50GHz is presented in figure 6(b), clearly showing the expected f_{clk}/8 signal at 25.60GHz without any spectral content at lower frequencies.

Divider input clock sensitivity measurements were performed and are summarized in figure 7. For this 204.8GHz divider, the meta-stable source-free self-oscillation (circuit DC biased, no clock signal) referenced to the clock input is 143GHz.

TABLE I
SUMMARY OF THE FASTEST REPORTED STATIC FREQUENCY DIVIDERS

Max. Clock Freq. (GHz)	Division Rate	Technology	Scale (nm)	Reference
110	4	SiGe HBT	140	Infinion [4]
151.6	4	InP HBT	400	HRL [5]
152.0	2	InP HBT	500	Teledyne [1]
152	4	InP HBT	500	Lucent [6]
200.6	2	InP HBT	250	NGAS [7]
204.8	8	InP HBT	250	Teledyne, this work

V. CONCLUSION

A fully static divide-by-8 frequency divider having a record maximum clock frequency of 204.8GHz has been demonstrated in the Teledyne Scientific 250nm InP HBT technology, supported by a low-loss, 4-metal interconnect wiring environment. The scaling of the HBT from 500nm to 250nm features, combined with reductions to the HBT parasitic contact resistances and aggressive scaling of the circuit signal path lengths is responsible for the increased divider clock rate. Table-I summarizes the state-of-the-art results reported to date for static frequency dividers.

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