

InP HBT Integrated Circuit Technology for Terahertz Frequencies

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Abstract—We report on the development of a 0.25 μm InP HBT technology suitable for integrated circuit demonstrations at the lower end of the THz frequency band (0.3-3THz). Transistors demonstrate an extrapolated f_{max} of >800GHz while maintaining a common-emitter breakdown voltage (BV_{CEO}) >4V. The transistors have been integrated in a full IC process that includes three-levels of interconnects, backside wafer thinning to 50 μm with a through-wafer via process, and a backside etch singulation process that allows for the formation of free-standing integrated waveguide probes. The technology has been utilized to demonstrate amplifiers, fixed-frequency and voltage controlled oscillators and dynamic frequency dividers all operating at >300GHz.

Index Terms—InP HBT, terahertz, TMICs.

I. INTRODUCTION

INDIUM phosphide (InP)-based high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) have attained the highest reported transistor bandwidths, with power gain cutoff frequencies (f_{max}) approaching or exceeding 1 THz [1,2]. Taking advantage of these record bandwidths integrated circuits have recently been demonstrated in the submillimeter-wave and terahertz frequency bands (0.3-3 THz) [3,4]; frequency regimes that were previously accessible only with two terminal devices such as Schottky diodes. Terahertz monolithic integrated circuits (TMICs) based on HEMT and HBT technologies will enable new and emerging applications in imaging, radar, spectroscopy and communications.

Compared to InP HEMTs, double-heterojunction bipolar transistors with wide bandgap InP collectors offer a higher breakdown voltage at a give current gain cutoff frequency (f_i).

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InP HBTs have also demonstrated the highest reported bandwidths for digital circuit building blocks static frequency divider circuits operating at >200GHz [5,6]. Further, at frequencies approaching a significant fraction of the transistor bandwidth, input shot noise no longer dominates the transistor noise characteristics, and InP HBTs operated at 10-20% of their peak current density should have comparable noise figure to HEMTs of similar bandwidth. These characteristics make the HBT technology capable of realizing all necessary transmit and receive components (LNA, VCO, mixer, LO PLL) in a single IC platform. Single-chip THz transmitters and receivers will eliminate lossy waveguide interconnects and transitions and permit the construction of receiver arrays with single-wavelength element spacing.

In addition to wide bandwidth transistors, a TMIC technology requires a compact low-loss interconnect environment, wafer thinning and through-wafer vias for substrate mode control, and methods for efficiently coupling THz signals on-to and off-of the wafer. In this work, we describe the development of the various technical aspects of a 0.25 μm InP HBT TMIC technology, and report on a number of >300GHz integrated circuit designs.

II. INP HBT TECHNOLOGY

The HBTs are fabricated on 4" InP substrates and epitaxial layers are grown by molecular beam epitaxy. The 0.25 μm technology described here utilizes a 30nm carbon-doped base layer with 50 meV of compositional grading to reduce base transit time. Chirped super-lattice grading (InGaAs/InAlAs) is used at both base-emitter and base-collector heterojunctions to smooth the conduction band discontinuity between the wide bandgap InP emitter/collector and narrow bandgap InGaAs base. The total N- collector thickness is 150nm and the base-collector junction design has been optimized to support high current density operation (>10mA/ μm^2) [7].

The first step in the HBT fabrication is the formation of the emitter contact. Electron-beam lithography is used to define the 0.25 μm emitter contact, which is deposited using an Au-based electroplating process [8]. The electroplating process provides a larger height-to-width ratio and straighter sidewalls than can be obtained in standard evaporation and liftoff processes. These traits are beneficial for the sidewall spacer process used to form the self-aligned base-emitter junction. After plating, a combination dry/wet etch process is used to

form the emitter mesa. A thin emitter semiconductor stack (<80nm) minimizes lateral undercut in wet etch steps. Dielectric sidewall spacers are then formed on the emitter contact using a conformal dielectric deposition followed by an anisotropic dry etch. The sidewalls passivate the base-emitter junction and facilitate the formation of a self-aligned base contact. I-line photolithography is used for all process steps after the emitter contact and the remaining process flow follows that of a standard triple-mesa HBT, with particular attention paid to minimizing the transistor parasitic capacitances.

Fabricated HBTs demonstrate a DC beta (β) of approximately 25, and a common emitter breakdown voltage of >4.0 V ($J_E = 10\mu\text{A}/\mu\text{m}^2$). The transistors support high current and power densities. This is illustrated in the common-emitter IV characteristics (Fig. 1) that show the transistor operating at current densities of >10 mA/ μm^2 , and power densities of >20 mW/ μm^2 .

Fig. 2 shows the measured RF power gains of a $0.25\times 4\mu\text{m}^2$ HBT biased for peak RF performance. S-parameter measurements were performed on-wafer to 50GHz. An LRRM calibration was performed using a commercial calibration substrate, and pad parasitics were deembedded from the measurements using open and short test structures. The maximum current gain cutoff frequency (f_i) and maximum power gain cutoff (f_{max}) are extracted from least-squares fits to single-pole transfer functions of the measured H_{21} and unilateral power gain (U), respectively. The extrapolated f_i and f_{max} of the transistor are 392GHz and 859GHz, respectively, at a bias condition of $V_{CE} = 1.8\text{V}$ $I_C = 13\text{mA}$.

Accurate transistor measurements at THz frequencies (>300GHz) are difficult due to the small transistor parasitics and challenges in obtaining accurate on-wafer calibrations due to spurious modes generated in an on-wafer wiring environment. Transistor models are therefore extracted from low frequency measurements. Models based on the Agilent HBT model [9] have been developed to accurately describe the unique characteristics of III-V bipolar devices. The model includes all relevant transistor parasitic elements and should scale well to frequencies approaching the transistor cut-off frequencies; an assertion that is supported by the good agreement that we have observed between measurements and simulation for >300GHz IC designs.

III. INTERCONNECTS AND BACKSIDE PROCESSING

Integrated THz receiver and transmitters will require a mixture of circuits including both traditional distributed microwave (PA, LNA) and analog-type ICs (Gilbert-cell mixers, frequency dividers). A thin-film 3-level IC wiring environment has been developed to support both circuit types. The wiring utilizes a benzocyclobutene (BCB) interlayer dielectric with a low dielectric constant ($\epsilon_r = 2.7$) and electroplated Au-based metallization. The technology also includes MIM capacitors and thin-film resistors.

Lumped analog blocks require low-delay, low parasitic

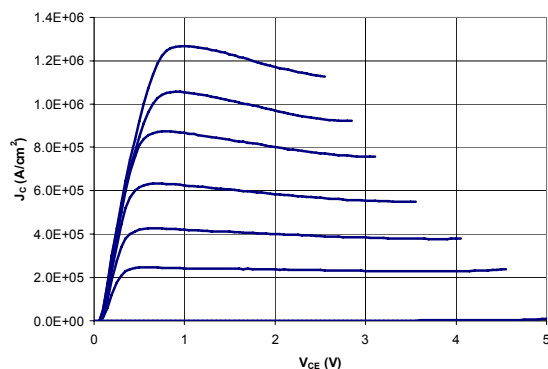


Fig. 1. Measured common-emitter IV characteristics of $0.25\times 4\mu\text{m}^2$ HBT

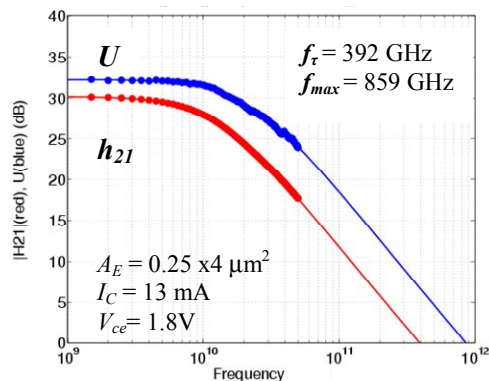


Fig. 2. Measured short circuit current gain (H_{21}) and Unilateral power gain (U) of 250nm InP HBT.

wiring and interconnects for these circuits must support narrow lines and fine pitch. This wiring can be achieved in the lower two metallization levels (M1,M2) which are separated by a $1\mu\text{m}$ BCB layer. Distributed sub-mm-wave circuits require high Q and low loss transmission lines. To achieve this, the upper level metallization (M3) is separated from M1 by a thicker $10\mu\text{m}$ BCB layer. This permits the realization of low-loss microstrip lines using either standard (M3 signal, M1 ground) or inverted (M1 signal, M3 ground) configurations.

The use of thin-film wiring on the top side of the InP substrate permits the substrate thickness to be kept relatively thick ($50\mu\text{m}$) to support handling ruggedness. Dry-etched substrate vias are added to IC designs with sufficient density to suppress modes that could be excited from parasitic RF leakage into the substrate. Substrate mode control is particularly important when packaging IC chips in waveguide blocks.

To facilitate waveguide packaging, we have developed a backside etch singulation process that is used to form non-rectangular IC die. This process permits the formation of narrow InP extensions that can be extended into rectangular waveguide channels. The extensions minimize breaks in the waveguide sidewall and permit a larger overall IC die size. Additionally, the backside etch process can be used to remove the InP substrate directly beneath waveguide probes (waveguide-to-chip transitions), improving probe performance. Fig. 3 shows a chip photograph of a fabricated InP LNA after completion of the backside singulation process.

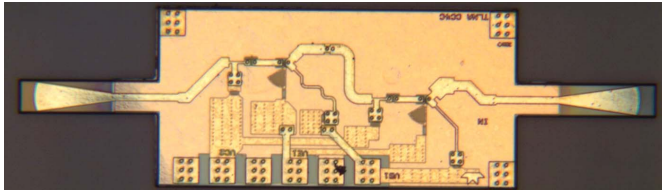


Fig. 3. Chip photograph of 300GHz LNA design with integrated waveguide probes after backside etch singulation process. Chip dimensions are $1000 \times 500 \mu\text{m}^2$

Waveguide probe designs have been separately characterized with through-line test structures in waveguide blocks. Probe insertion losses of $<1\text{dB}$ per transition have been measured in the WR-3 waveguide band.

IV. TMIC DESIGNS

Our goal is to extend the complexity and functionality found in current modern microwave RFIC designs to the THz frequency regime. To that end, we have designed and fabricated building block circuit elements required for transceiver systems targeting $>300\text{GHz}$ operation.

A. Oscillator Circuits

Both fixed frequency (SFO) and voltage controlled (VCO) fundamental oscillator TMICs have been demonstrated in our InP HBT technology [10]. The differential oscillator topology utilizes series-tuned (T-network) feedback because it is less affected by layout parasitics than a traditional Colpitts configuration. Voltage controlled designs utilize varactors formed with the HBT base-collector junction. Fig. 4 shows a chip photograph of a fabricated VCO. An inverted microstrip wiring environment is used to provide a controlled impedance environment.

Fixed frequency oscillators operating at 310GHz demonstrated a single-ended output power of -6.2dBm (corrected for probe loss) and 300GHz voltage controlled oscillators demonstrated 12GHz of tuning bandwidth. Phase noise measurements performed on a 286GHz oscillator demonstrated -96.6dBc/Hz phase noise at a 10MHz offset.

The maximum reported frequency of our previously reported oscillator results (up to 346GHz) was limited by the test set-up that was being utilized which consisted of WR3 waveguide ($220\text{-}325\text{GHz}$) probes coupling to a WR3 harmonic mixer (OML Inc.) We have recently tested oscillator circuits operating to much higher frequencies [11]. For these designs, oscillator output frequencies have been confirmed using integrated down converting mixer circuits and also directly using Fourier transform spectroscopy (FTS). Fig. 5 shows the measured FTS output for a 440GHz oscillator design. For this test, the oscillator output was taken off-wafer with a WR-3 waveguide probe (over-moded) and coupled quasi-optically to an FTS system that utilized a Golay detector cell.

B. Dynamic Frequency Divider Circuits

Dynamic frequency divider circuits operating to 331GHz have also been demonstrated in our InP HBT technology [12].

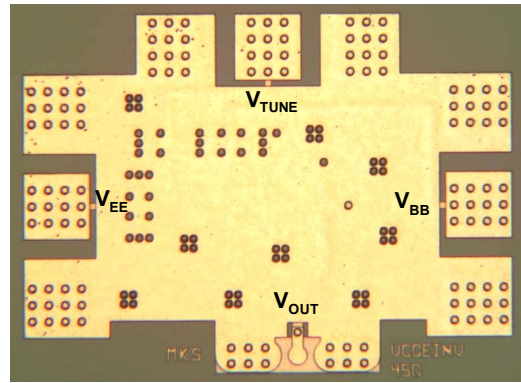


Fig. 4. VCO chip photograph ($740 \mu\text{m} \times 550 \mu\text{m}$). The entire circuit except pad areas is covered by a M3 ground plane.

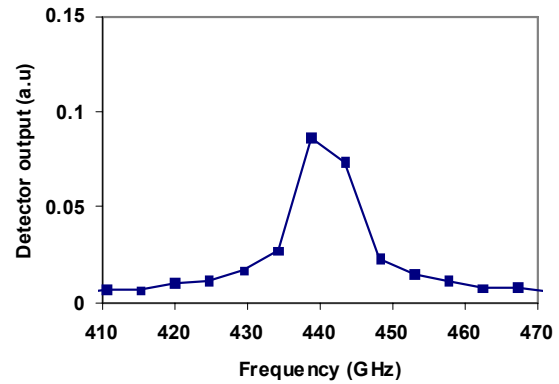


Fig. 5. Oscillator frequency measurement by Fourier-Transform Spectroscopy (FTS). Plot shows the detector output after Fourier-Transform for a 440GHz oscillator design.

The divider is based on a regenerative feedback loop formed with an active mixer. Typically, such regenerative divider circuits are realized using either resistors or transimpedance stages as a mixer load. In this work, short transmission lines are used as an inductive load. This topology results in a compact layout and increases the maximum divider operating frequency by more than 20% in simulation.

Divide-by-two circuits were fabricated and tested on-wafer. A Virginia Diodes WR-3 diode multiplier module was used to drive the circuit, and the output was measured using a WR-5 sub-harmonic mixer from OML Inc. Fig. 6 shows the measured output spectrum with a 328.8GHz clock input. A maximum operating frequency of 331GHz was demonstrated. In this test configuration, the minimum operating frequency was 304.8GHz but this was limited by the lower range of the diode multiplier chain. Circuits with integrated fixed-frequency and voltage controlled oscillators were also fabricated and these circuits operated to a minimum frequency of 270GHz . The total power consumption of the divider circuit was 85.5mW .

C. Amplifier Circuits

Amplifier designs have been fabricated using both single-ended and differential design topologies. At THz frequencies, our HBTs demonstrate significantly higher maximum available gain in a common-base configuration. A differential topology

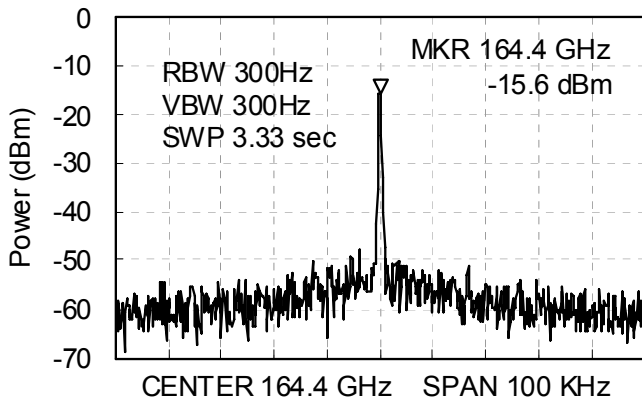


Fig. 6. Measured output spectrum of dynamic divider circuit with 328.8 GHz clock input.

can minimize grounding inductance at the base node and improve circuit stability. In [13], a 6-stage driver amplifier was demonstrated in a differential common-base topology with 17.3dB gain at 290GHz. The design utilized a cascaded topology that permitted current sharing (no DC blocking capacitors) and operation from a single-DC supply.

Single-ended low noise amplifiers have been fabricated demonstrating good agreement between measured and simulated noise figure. A single-stage cascode design was demonstrated with 8.4dB at 288GHz [4]. The design had a 1dB bandwidth of 19GHz with a total DC power consumption of 23mW. Noise figure measurements were performed on-wafer using a technique similar to that described in [14]. A noise figure of 11.2dB was measured at 300GHz, in good agreement with the simulated value of 12.1dB.

A two-stage cascode LNA design has recently been demonstrated based on the previously reported single-stage design. The amplifier demonstrates a peak gain of 20.5dB at 315GHz. On-wafer measurements of the amplifier S-parameters are shown in Fig. 7. The amplifier has a 3dB-bandwidth of 17GHz with a total DC power consumption of 60mW.

V. CONCLUSION

We have presented a high performance 0.25 μm InP HBT IC technology suitable for >300GHz applications. The initial demonstration of key circuit building blocks presents a promising path for developing fully integrated THz transmitter and receiver circuits. Designs are presently in fabrication to demonstrate integrated receiver circuits and phase-locked loop circuits at >300GHz. Additionally, a 128nm HBT technology is in development for operation at even higher frequencies.

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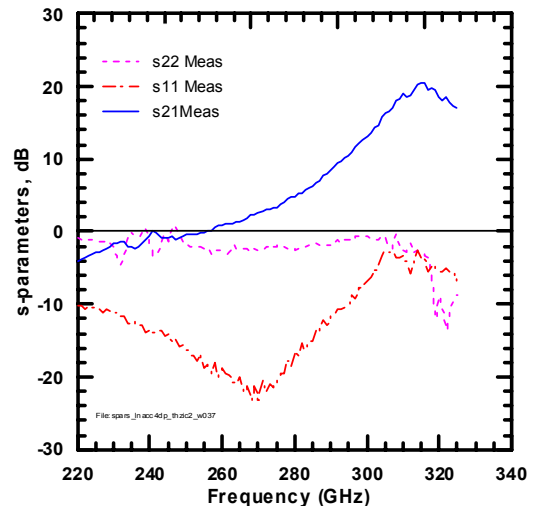


Fig. 7. S-parameter measurements of 2-cascode stage LNA circuit. Circuit consumes 60mW of DC power

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