

An Optical Phase-Locked Loop Photonic Integrated Circuit

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Abstract—We present the design, fabrication, and results from the first monolithically integrated optical phase-locked loop (OPLL) photonic integrated circuit (PIC) suitable for a variety of homodyne and offset phase locking applications. This InP-based PIC contains two sampled-grating distributed reflector (SG-DBR) lasers, semiconductor optical amplifiers (SOAs), phase modulators, balanced photodetectors, and multimode interference (MMI)-couplers and splitters. The SG-DBR lasers have more than 5 THz of frequency tuning range and can generate a coherent beat for a wide spectrum of frequencies. In addition, the SG-DBR lasers have large tuning sensitivities and do not exhibit any phase inversion over the frequency modulation bandwidths making them ideal for use as current controlled oscillators in feedback loops. These SG-DBR lasers have wide linewidths and require high feedback loop bandwidths in order to be used in OPLLs. This is made possible using photonic integration which provides low cost, easy to package compact loops with low feedback latencies. In this paper, we present two experiments to demonstrate proof-of-concept operation of the OPLL-PIC: homodyne locking and offset locking of the SG-DBR lasers.

Index Terms—Coherent optical communications, integrated optoelectronics, optical phase-locked loops (OPLLs), tunable semiconductor lasers.

I. INTRODUCTION

EVER SINCE the first demonstration of an optical phase-locked loop (OPLL) [1], a significant research effort has been invested in developing the system for a wide range of applications, as shown in [2]–[4] and references therein. In optical communications, the OPLL allows synchronous coherent receivers where mixing the received signal with a high-power local-oscillator (LO) laser provides high sensitivity and out-of-band noise suppression [5]–[7]. For carrier-suppressed modulation schemes, a Costa's loop can be used [8]. OPLLs are commonly used for optical clock recovery in digital telecommunication systems [9]. They have also been developed for generation of stable channel offsets in dense wavelength-division multiplexed (DWDM) systems [10]. In microwave photonics, an

OPLL can form a microwave single-sideband optical source [2] with the potential for endless microwave phase adjustment. This is an attractive property for implementation of a phased array microwave system. OPLLs also find applications in free-space optical systems such as LIDAR systems, where they allow coherent combination of several coherent optical sources [3], potentially to form large swept optical phase arrays.

Compared to fiber lasers and solid state lasers with narrow linewidths, semiconductor lasers are generally favored because of their small sizes, low costs, and high efficiencies [2], [11]. In addition, the phase and frequency tuning of a semiconductor laser, which is necessary for the laser to be used in the negative feedback loop of an OPLL, is easily achieved by current injection. So far, the central difficulty in realizing OPLLs using semiconductor lasers has been the strict relation between laser phase noise and feedback loop bandwidth. The wide linewidths observed in semiconductor lasers, typically in the megahertz range, require sufficiently wide loop bandwidths, i.e., small loop delays. In the past, this has been addressed by using low-linewidth external cavity lasers that allow longer feedback loop delays [12], [13], or by construction of compact OPLLs using miniaturized bulk optical components to meet the delay restrictions arising from the use of standard semiconductor lasers [2], [14]. Other efforts include relaxing this restriction by combining an OPLL with optical injection locking, thereby gaining the wide locking bandwidth of optical injection, while a slow phase-locked loop with a long delay allows long-term stability [15].

Recent progress in device design and fabrication has enabled distributed-feedback (DFB) lasers to have sub-megahertz linewidths, without external cavity linewidth reduction schemes, [3], [8], [14], [16]–[18]. Consequently, the delay in fiber-based OPLLs is not the bandwidth limiting factor in locking the standard DFB lasers. Rather, the loop bandwidth is limited by the phase reversal in the FM response, which is characteristic for DFB lasers and occurs at frequencies between 0.1 and 10 MHz [2], [16], [19], [21], as explained in Section III. While this lower loop bandwidth is sufficient for locking of DFB lasers even in fiber-based OPLLs, it is still a limiting factor in achieving high-performance OPLLs with very small phase errors because the benefits of locking are constrained to the narrow bandwidth determined by the phase reversal [2], [11], [16]. In the applications such as the coherent beam combining [16], where several lasers are locked, the cumulative phase error increases with the number of lasers, and it is important to minimize it.

In order to overcome the phase-inversion-limited FM bandwidth of standard narrow-linewidth DFB lasers, new types

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of semiconductor lasers have been developed for their use in OPLLs. Complex-coupled DFB lasers have been shown to have flat FM responses without phase inversion between 10 kHz and over 20 GHz [22]. The requirement for precise control of the lasers' bias current and the fact that the FM-response uniformity and sensitivity depend on the output power level are disadvantageous for OPLL applications [19]. Multi-section tunable semiconductor lasers have been very popular in the past in OPLLs [2], [17], [19], [23], [25]. Here, the phase tuning section is separated from the gain section and the Bragg section, which minimizes the thermal tuning issues responsible for the phase inversion in DFB lasers.

Integration of an OPLL is considered to be beneficial for a wide range of applications by researchers in the field [2], [3], [10], [13], [14], [17], [25]. Monolithic integration of the optical components in an OPLL can improve its robustness to temperature and environmental variations, which can be detrimental in fiber-based systems [16]. These variations have smaller cumulative effects on light when it propagates through a robust and compact, monolithically integrated optical components. In addition, the whole photonics integrated circuit (PIC) that includes the semiconductor lasers and the optical components of the OPLL can be maintained at a constant temperature by the same temperature controller. Typical integrated optical waveguides and devices preserve the polarization of light, so that no polarization alignment between the components is necessary in order to maximize the interference between the integrated lasers in the applications where multiple lasers are being locked. Furthermore, integrated waveguides are immune to long term polarization drifts. Also, compared to the miniature bulk optics OPLLs [2], no alignment between the components needs to be performed. The compactness and ease of packaging of integrated OPLLs can improve their cost effectiveness. This is especially true for the applications where multiple lasers are locked together [3], [11], [26].

Monolithic integration of multi-section lasers is strongly motivated by two factors. First, in multi-section lasers the passive phase and Bragg sections are already integrated with the active gain section. In order to achieve this, a regrowth or some other type of post-growth bandgap engineering technique, such as quantum-well intermixing, is necessary [27], thereby facilitating integration of additional active devices, such as semiconductor optical amplifiers (SOAs) and photodetectors, and passive devices, such as modulators and multimode interference (MMI) couplers and splitters. Second, compared to DFB lasers, multi-section lasers have larger linewidths, in the several-megahertz range. Although, a state-of-the-art OPLL performance has been achieved with multi-section lasers and miniature bulk optics [2], monolithic integration can offer further performance improvement by reduction of the loop delay. Monolithic integration can also enable a variety of other types of wide-linewidth lasers to be used in OPLL applications, such as widely-tunable sampled grating distributed feedback (SG-DBR) lasers.

So far, monolithic integration has focused on the receivers and on the electronic components rather than the optical components of an OPLL [10], [28], [29]. In this paper, we demonstrate for the first time, an OPLL photonic integrated circuit (OPLL-PIC) in which all required optical components are monolithically inte-

grated, including: lasers, passive optical waveguides, MMI couplers/splitters, high-speed photodetectors, and high-speed optical phase modulators. Moreover, the OPLL-PIC uses widely-tunable SG-DBR lasers that have a wavelength tuning range greater than 5 THz [30]. This is a key feature for several applications. First, it allows the development of homodyne coherent receivers in the form of Costa's loop, with an optical bandwidth exceeding the entire C-band. The relative simplicity of the Costa's loop also allows scaling to high data rates, exceeding 100 Gbps. Second, an OPLL with 5 THz wavelength tuning range can be used for coherent beam forming for sub-millimeter resolution LIDAR applications. Third, together with a THz photodetector and electronics, it allows optical heterodyne signal generation with a DC to 5 THz frequency range. Applying optical phase or amplitude modulation to one optical line can be used to generate a coherent phase or amplitude modulated THz signal. The rest of the paper is organized as follows: the design and fabrication of the OPLL-PIC is described in Section II, the SG-DBR laser performance is described in Section III, proof-of-concept homodyne and offset locking OPLL demonstrations are presented in Section IV, and the conclusion remarks are presented in Section V.

II. OPTICAL PHASE-LOCKED LOOP PHOTONIC INTEGRATED CIRCUIT

A. OPLL Basics

An OPLL has both parallels and fundamental differences when compared to its RF equivalents. In a microwave loop, it is a voltage-controlled oscillator that typically tracks the input signal. In an OPLL, wavelength tuning of a laser takes this role, achieved typically by current injection [3]. An RF phase-locked loop (PLL) can be built using spectrally pure oscillators, which allow stable operation in a narrowband loop to enable filtering, or it can be built using compact integrated circuits to have a substantial fractional loop bandwidth compared to the carrier frequency, allowing agile tracking of a frequency modulated signal. In contrast, an OPLL is built using less compact optical components, leading to a smaller loop bandwidth, and with a carrier frequency of ~ 193 THz (1550 nm), which results in low loop bandwidth to carrier frequency ratio. As a result, acquiring locking is less straightforward in an OPLL as the slave laser must be tuned to the master laser wavelength with high accuracy.

Fig. 1 shows a simple schematic of the OPLL architecture demonstrated in this paper. Two widely tunable SG-DBR lasers are monolithically integrated on a single InP substrate along with all of the other optical components needed to form the OPLL. One laser takes the role of a master laser, while the other takes the role of a slave laser. The outputs of the two lasers are first combined using a 2×2 optical coupler. The combined beat signal is then amplitude modulated for offset-locking using an integrated optical modulator and envelope- detected using an integrated photodetector. The current output from the photode-

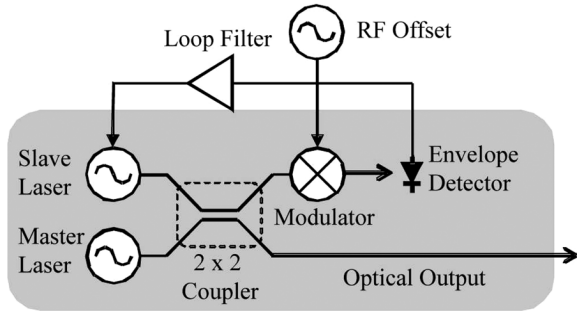


Fig. 1. Schematic of an OPLL heterodyne offset locking experiment.

tor is filtered and fed back into the slave laser. The resulting slave laser frequency tuning is then given by

$$\frac{d\varphi_s}{dt} = h_m * h_d * f_{LF} * h_s * (2R\sqrt{mP_mP_s} \sin(\varphi_m - \varphi_s)) \quad (1)$$

where the terms in the convolution: h_m , h_d , f_{LF} , and h_s are the impulse responses of modulator, detector, loop filter, and slave laser frequency tuning, respectively. R is the detector responsivity, P_m and P_s are the master and slave laser powers incident on the photodetector, and φ_m and φ_s are the phases of the master and slave laser respectively. Also, m is the relative power of the modulation sidebands used for offset locking after optical modulation. For zero offset locking, i.e., homodyne locking, no optical modulation needs to be applied and $m = 1$. Assuming locked condition and small phase error ($\varphi_m \approx \varphi_s$), the equation can be linearized ($\sin(x) \approx x$) and the Laplace transform applied

$$\begin{aligned} \varphi_s &= \frac{H_m H_d F_{LF} H_s 2R\sqrt{mP_mP_s}}{s} (\varphi_m - \varphi_s) \\ &= G(s)(\varphi_m - \varphi_s). \end{aligned} \quad (2)$$

Here, $G(s)$ is the open-loop gain function from which stability and operation of the loop can be evaluated. It is interesting to note that offset locking of our OPLL could also be achieved without the on-chip modulation of the two laser outputs, but rather by mixing the photodetector current with an external RF reference. In our method, the generated sidebands carry only a fraction of power of the laser outputs and thus produce small interference extinction ratios when mixed together, incurring additional noise penalty. The advantage is that no RF electronics is required.

B. OPLL-PIC Design

Fig. 2(a) and (b) show schematics of our two different OPLL-PIC designs. The design shown in Fig. 2(a) is intended for locking of an on-chip tunable laser to an external laser, while the design shown in Fig. 2(b) is intended for offset locking of two on-chip tunable lasers. Each OPLL-PIC design comprises of three sections that are labeled in Fig. 2(a) and (b) as: Laser Section, Middle Section, and Output Section. We choose the SG-DBR laser because of its wide tuning range, large frequency-modulation (FM) tuning sensitivity,

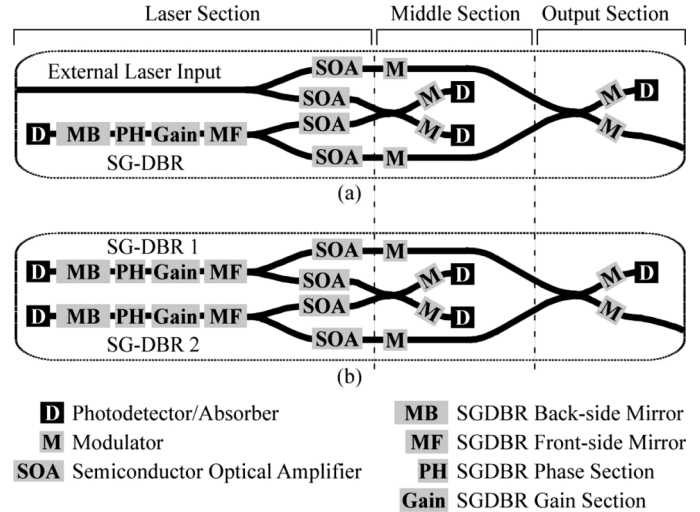


Fig. 2. Schematic of (a) an OPLL-PIC for locking to an external laser and (b) an OPLL-PIC for offset locking of two on-chip lasers.

and absence of phase inversion in the frequency response, as explained in Section III.

In Fig. 2(a) and (b), we explicitly show the constituent components of the SG-DBR laser: front-side mirror (MF), gain section, phase section (PH), back-side mirror (MB), and back-side absorber/photodetector (D). Light from each laser is first split using 1×2 MMIs into two half-power components. One of the two half-power components from each laser is directed into a 2×2 MMI, which is a part of the feedback loop, and which is located in the Middle Section of the OPLL-PIC. The remaining half-power component from each laser is directed into a 2×2 MMI in the Output Section of the OPLL-PIC. Each of the four half-power optical paths has an SOA to adjust the optical power in each path. Each optical path at the output of the 2×2 MMI coupler in the Middle Section of the OPLL-PIC contains a phase modulator (M), followed by a photodetector (D), which can be used in a balanced receiver configuration. Similarly, each optical path at the two outputs of the 2×2 MMI in the Output Section of the OPLL-PIC contains a phase modulator. One of these two output waveguides ends upon a photodetector that can be used for electrical-domain monitoring of the interference resulting from the beating of the two lasers. The other output waveguide extends to the edge of the OPLL-PIC to enable coupling into an optical fiber and can be used for optical-domain beat monitoring. The 2×2 MMI in the Output Section has phase modulators on its input waveguides as well, which can be used for additional phase control.

Fig. 3(a) shows a scanning electron microscope (SEM) image of an OPLL-PIC based on the schematic shown in Fig. 2(b), which enables offset locking, after it has been mounted on a carrier and wire-bonded. The distinct OPLL-PIC sections mentioned above are marked for identification. The OPLL-PIC is 6.6 mm long and 0.45 mm wide.

The Laser Section of the OPLL-PIC is shown in greater detail in Fig. 3(b). The abbreviations used in labeling the various components of this section are explained in Fig. 2. This section

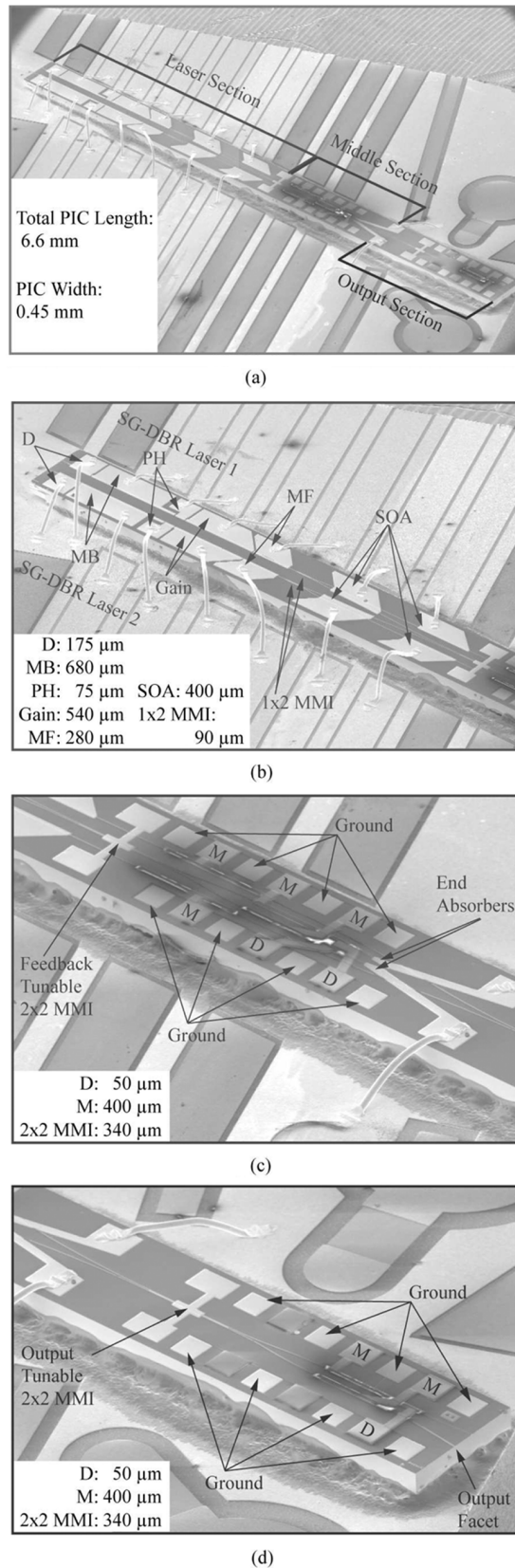


Fig. 3. SEM images of the OPLL-PIC and its various sections. (a) Whole OPLL-PIC. (b) Laser Section of the OPLL-PIC. (c) Middle Section of the OPLL-PIC. (d) Output Section of the OPLL-PIC.

also includes the two 1×2 MMI splitters and the four SOAs. As shown in Fig. 2, there are four SOAs in the PIC, one on each

output of both 1×2 MMI splitters. Some variations of the PIC, approximately one third of the devices, were designed to have only two SOAs, one for each laser, placed at inputs of the 1×2 MMI splitters. Although additional biasing is required, the advantage of having four SOAs at the outputs of the 1×2 MMI splitters is that they can be used to equalize the lasers' output powers for better, more efficient interference. In this work, however, due to the test bench limitations, the SOAs were wire-bonded together to the same pad on the carrier.

Fig. 3(c) shows the Middle Section of the OPLL-PIC. The 2×2 MMI in this section can be tuned by current injection [31], [32], although we have not done it in this work. The modulator and photodetector at the output of the 2×2 MMI connect to RF pads that are arranged in a G-S-G-S-G-S-G configuration for direct probing, with 150 μm pitch and 100 $\mu\text{m} \times 100 \mu\text{m}$ surface area per pad. Two 200 μm long curved (7°) active sections with grounded pads, absorb light that is not absorbed in the two photodetectors.

Fig. 3(d) shows the Output Section of the OPLL-PIC. The two modulators and the photodetector at the outputs of the 2×2 MMI connect to RF pads that are arranged in the same way as those in the Middle Section of the OPLL-PIC, except that here there are three unused pads. The output waveguides that enable coupling into an optical fiber are angled at 7° with respect to the direction normal to the cleaved facet, and anti-reflection coatings are applied in order to minimize facet reflections.

C. OPLL-PIC Fabrication

For monolithic integration of the SG-DBR lasers with the other components of the OPLL-PIC, an integration platform that is often referred to as "Offset Quantum Well (OQW)" Platform [27] is used. In this platform, light is guided by a "passive" 1.4Q bulk layer that forms a basis for waveguiding, as well as modulation through current injection [33] or the Franz-Keldysh effect if reverse biased [34]. Above this layer, light couples evanescently to an "active" multiple-quantum-well (MQW) layered structure that is present only in the regions that form SOAs, gain sections of SG-DBR lasers, and photodetectors [27].

Fig. 4 shows details of the base epitaxial layer structure used in the OQW platform that is grown on a 2-inch S-doped InP wafer by metal-organic chemical vapor deposition (MOCVD). A 2 μm thick Si-graded-doped InP buffer is grown on the substrate to reduce the overlap of the optical mode confined to the 1.4Q waveguiding layer with the heavily doped substrate and minimize the free-carrier-induced optical propagation loss in the waveguide. The buffer doping is graded from $\sim 1e19 \text{ cm}^{-3}$, close to the substrate, to $\sim 1e18 \text{ cm}^{-3}$, close to the 1.4Q waveguide core layer. A 300 nm thick, unintentionally doped (UID), 1.4Q waveguiding layer is epitaxially grown over the graded InP buffer, followed by a 20 nm thick 1.2Q separate confinement heterostructure (SCH) layer, a 10 nm thick InP etch-stop layer, an active region comprised of multiple quantum wells (MQW) layers with a total thickness of 119 nm, another 30 nm thick 1.2Q SCH layer, a 60 nm thick UID InP spacer, and a 150 nm thick Zn-doped ($1e18 \text{ cm}^{-3}$) InP cap. The thin InP spacer underneath the Zn-doped InP cap helps prevent diffusion of Zn

	150 nm InP, Zn ($1e18 \text{ cm}^{-3}$)
	60 nm InP, UID
	30 nm 1.2Q, UID
"active layer"	119 nm MQW, UID
	10 nm InP, UID
	20 nm 1.2Q, UID
"passive layer"	300 nm 1.4Q
	2000 nm InP, graded Si-doped
	S-doped InP substrate

Fig. 4. "OQW" base epitaxial structure.

dopant into the active MQW layer, and the Zn doping in the InP cap helps in controlling the position of the p-i-n junction formed after regrowth. The photoluminescence peak of the active MQW layers was measured to be $\sim 1560 \text{ nm}$.

The 2-in wafer is cleaved into four different quarters and each quarter is processed separately. In Fig. 5(a)–(e), we illustrate the processing steps used in the fabrication of the OPLL-PIC. Starting from the base epitaxial structure shown again in Fig. 5(a), Fig. 5(b) illustrates the active/passive wet etch step, where the "active" regions are etched away everywhere on the wafer except in the areas that define the SOAs, gain sections of the SG-DBR lasers and the photodetectors. A 100 nm thick Silicon Nitride (SiN_x) layer is deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD), and $5 \times$ Stepper Lithography is used to define the active regions by patterning photoresist that is spun on top of the SiN_x layer. All SiN_x depositions in this work are done at 250°C . The pattern is transferred to SiN_x by CF_4/O_2 -based Reactive Ion Etching (RIE). The SiN_x hard mask protects the InP cap, spacer layers at the top of the wafer, and the active MQW and SCH regions during wet etching steps that selectively remove these layers elsewhere. The SiN_x mask is subsequently removed using buffered hydrofluoric acid (BHF).

The gratings in the SG-DBR sections are defined in the passive 1.4Q layer using a Methane/Hydrogen/Argon (MHA)-based RIE, as shown in Fig. 5(c). The targeted grating depth is around 100 nm and duty cycle is 50%. The gratings are patterned onto a high-resolution photoresist using electron-beam lithography. The grating pattern is transferred to a 50 nm thick SiO_2 layer using CHF_3 -based RIE, which, in turn, is used as a hard-mask for the MHA RIE step that etches the grating into the 1.4Q layer. The grating period is targeted to be $\sim 240 \text{ nm}$ so that the center wavelength of the SG-DBR laser is close to 1550 nm. The sampled gratings are used in both the front-side and back-side mirrors of the SG-DBR lasers. The front-side mirror consists of 5 grating bursts, each burst being $6 \mu\text{m}$ long, that repeat periodically with an interval of $61.5 \mu\text{m}$. The back-side mirror consists of 12 grating bursts, each burst being $4 \mu\text{m}$ long, that repeat periodically with an interval of $68.5 \mu\text{m}$. More details about the wide wavelength tuning using

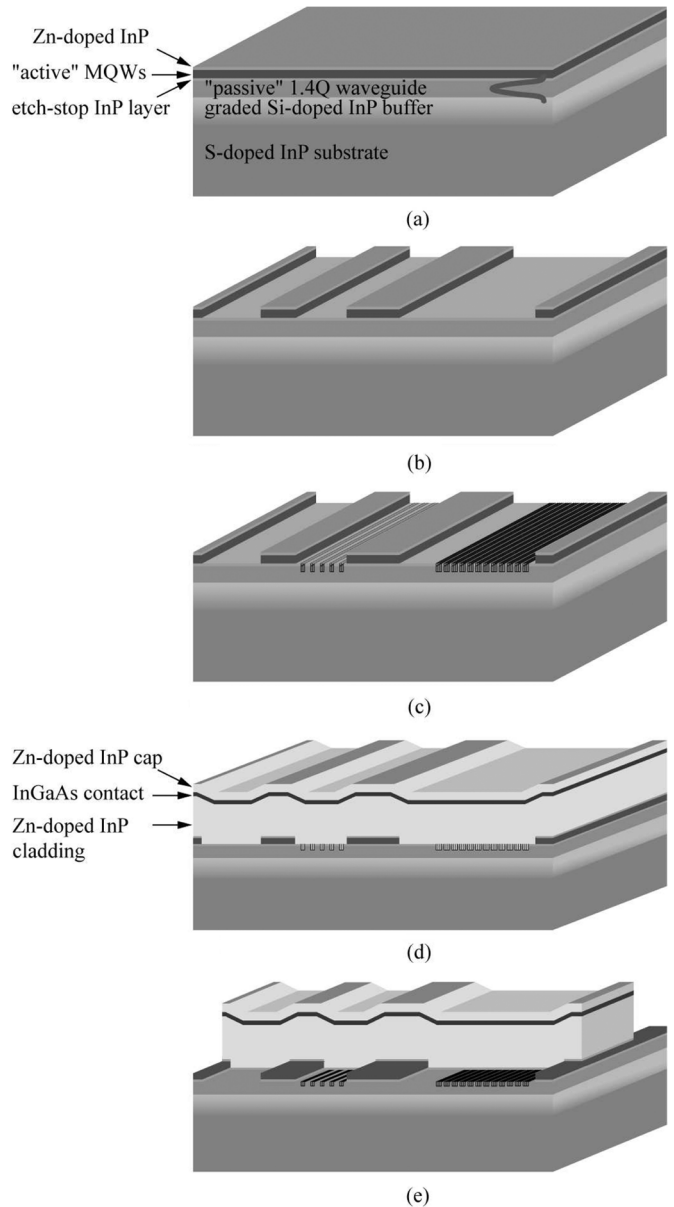


Fig. 5. "OQW Platform": schematics of the main processing steps starting with the base epitaxial structure. (a) Base epitaxial structure. (b) Active/passive wet etch. (c) Gratings etch. (d) P cladding regrowth. (e) Surface-ridge waveguide etch.

the Vernier effect achievable with SG-DBR lasers can be found in [35]. The SiO_2 layer is subsequently removed using BHF, and the sample is thoroughly cleaned in UV-ozone prior to the regrowth step.

The following step is the regrowth step, as shown in Fig. 5(d). The regrowth layers comprise of a 50 nm thick UID InP spacer that helps prevent diffusion of Zn from p-doped cladding into the underlying MQW layers in the active regions and the 1.4Q layer in the passive regions of the OPLL-PIC, a 2000 nm of Zn-doped InP cladding, where the doping is $7e17 \text{ cm}^{-3}$ in the lower half of the cladding and $1e18 \text{ cm}^{-3}$ in the upper half of the cladding, a 100 nm thick Zn-doped ($1e19 \text{ cm}^{-3}$) InGaAs contact layer followed by a 200 nm thick Zn-doped ($1e18 \text{ cm}^{-3}$) sacrificial InP cap layer, on the top of the wafer, which is used to

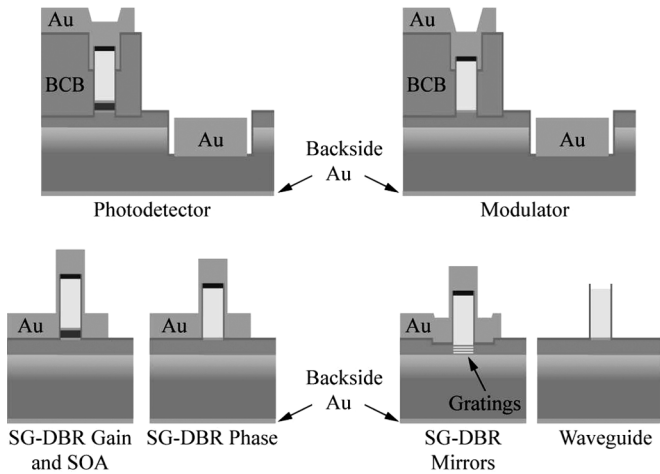


Fig. 6. Schematics showing cross sections of various components of the fully processed OPLL-PIC.

protect the thin InGaAs contact layer during the processing steps prior to metallization. The p-doping in the InP cladding layer is decreased closer to the waveguide core in order to reduce the free-carrier-induced optical loss.

Following the regrowth, surface-ridge waveguides are etched, as shown in Fig. 5(e). First, an MHA-based RIE using a 100 nm thick SiN_x hard mask is used to etch the waveguides to a depth of $\sim 1.5 \mu\text{m}$ below the regrown InGaAs layer. Following the dry etch, the surface ridge waveguide is further etched by a $\text{HCl}:\text{H}_3\text{PO}_4$ wet etch cleanup so that the rest of the p-doped InP cladding is removed. The 1.2Q layers directly above the MQW layer in the active regions and directly above the 1.4Q layer in the passive regions act as etch-stops for the selective wet-etch. All waveguides deviate less than 7° from the normal to the major plane, so that minimal undercutting of waveguide walls is observed. In one quarter of the fabricated PICs, including the PIC presented in this paper, waveguides widths are adiabatically tapered from $3 \mu\text{m}$, starting at the outputs of the 1×2 MMI splitters to $2.3 \mu\text{m}$ at the input of the feedback loop 2×2 MMI coupler. This is done over a distance longer than $300 \mu\text{m}$ in order to minimize the radiation losses. Similar tapering is done for the waveguide sections entering the output 2×2 MMI coupler. Since our passive waveguides are weakly multimoding when they are $3 \mu\text{m}$ wide, the tapering is used to diminish the negative effect that multimoding has on the extinction ratio of interference of the two lasers' outputs in the 2×2 MMI coupler. As the wider waveguide sections have lower loss, outputs of the 2×2 MMI couplers are tapered back to $3 \mu\text{m}$ in a similar manner. Passive waveguide widths in the rest three quarters of the PICs are maintained at $3 \mu\text{m}$. By comparing PICs with tapered waveguides to those with non-tapered waveguides, the effect of weak multimoding on the extinction ratio can be studied. Waveguide sections for input and output coupling of light are curved by 7° and their widths are tapered to $5.5 \mu\text{m}$ in order to minimize facet reflections. In addition, anti-reflection coatings are applied to the facets after the processing steps are completed. Together with the 7° waveguide curves and the $5.5\text{-}\mu\text{m}$ tapers, total facet

reflectivity of less than 10^{-4} is expected, which has been shown to be necessary for similar PICs [36], [37].

The processing steps that follow the ridge waveguide etching are fairly common and not necessarily characteristic of our integration platform. Here, we summarize the remaining steps. Fig. 6, shows various sections of the OPLL-PIC after these processing steps have been completed.

First, a thick photoresist is patterned so that it covers the entire sample except $\sim 12 \mu\text{m}$ on each side of the ridge waveguide sections that form the high-speed modulators and high-speed photodetectors. The waveguides are still protected by SiN_x hard mask that was used to etch the surface ridges in the previous step. MHA-based RIE is used to remove the top 20 nm thick 1.2Q SCH layer and approximately 80 nm of the underlying 1.4Q layer. Both of these layers contain Zn atoms that diffuse from the p-doped InP cladding during regrowth. These Zn atoms can considerably increase the capacitance for the detectors and modulators, necessitating the dry etching of the top 100 nm of the quaternary semiconductor.

An additional 100 nm thick SiN_x layer is deposited and patterned to provide a hard mask for MHA-based RIE that is used to etch windows for top N-contact metallization. The etch is performed until it penetrates $\sim 0.5 \mu\text{m}$ below the Si-graded-doped InP buffer into the heavily doped substrate. A thick photoresist covers the wafer everywhere except the N-contact metallization window regions. An electron-beam evaporator is used to deposit a Ni/AuGe/Ni/Au contact, which is patterned using the liftoff technique. The thickness of gold deposited during this step is only $\sim 0.5 \mu\text{m}$ as more gold is added during the P-contact metallization step. As illustrated in Fig. 6, the top N-contact is made only for fast devices, i.e., photodetectors and modulators. Top N-contacts are typically required for the PICs that are fabricated on semi-insulating substrates to provide low-loss connection to the ground plane [32], [36]. The main reason for having the top N-contacts in our proof-of-concept demonstration is the ease of direct RF probing, as discussed in Section II-B. N-contact for the remaining devices is achieved by backside metallization at the end of processing. The N-contacts are annealed at 430°C for 30 s. After the top N-contact metallization, a thin SiN_x layer is deposit and photo-sensitive BCB is spun, developed, and cured at 250°C . This leaves BCB in places that will be underneath the P-contact metal pads and traces running along the lengths of the high-speed photodetectors and modulators and covering the surface ridges in these regions. Along with the capacitance reduction etch, the BCB further reduces the capacitance of these devices to the extent that should enable their operation at frequencies far exceeding 10 GHz. The P-metal pads without BCB (1.2Q stop-etch layer) by sub-micron-thick SiN_x . BCB is used to elevate the P-metal pads farther from this surface, and thus farther from the N-doped substrate, so that this increased separation combined with the small dielectric constant of BCB (2.65), provide lower capacitance compared to the P-metal pads without BCB [36]. An additional thin SiN_x layer is deposit after BCB patterning. Thus, the BCB is sandwiched between thin layers of SiN_x , shown as thin lines in Fig. 6, for better adhesion to the

semiconductor surface below as well as the P-contact metal on top.

Three different types of P-contact metal vias need to be opened in the top SiN_x layer prior to the P-contact metallization. First, vias are formed by removing the SiN_x layer above N-contact metal. This is accomplished by patterning photoresist to cover the sample everywhere except over the N-contact metal and dry etching the SiN_x layer above the N-contact metal using CF_4/O_2 -based RIE. The next via is formed by removing the SiN_x layer on top of all the ridge waveguide sections except those covered with BCB. To open this via, photoresist is partly developed around the waveguides and partially etched back using O_2 -based RIE until the ridge tops are exposed. CF_4/O_2 -based RIE is then used to etch the SiN_x layer and expose the InP cap layer that is on top of the ridge waveguides. The remaining SiN_x over the rest of the wafer is protected by photoresist during this step. Finally, vias through the BCB layers are opened using a two-step process. A $5\text{-}\mu\text{m}$ -wide via is etched using CF_4/O_2 -based RIE to expose the ridge top buried underneath $3.7\text{-}\mu\text{m}$ -thick BCB and the SiN_x layers. This etch needs to be timed in order to minimize the difference in height between the ridge top and the BCB, and, consequently, minimize the P-contact capacitance. SiN_x is then re-deposited to fill in any openings that typically develop between the waveguide sidewalls and BCB, and a new via that is narrower than the waveguide is dry etched until the BCB and SiN_x layers are completely removed thereby exposing the InP on the top of the ridge.

At this point the sacrificial InP cap layer is removed using $\text{HCl}:\text{H}_3\text{PO}_4$ -based wet etch everywhere along the ridge waveguides, thus exposing the InGaAs contact layer.

Standard Ti/Pt/Au $8\text{-}\mu\text{m}$ -wide P-contact metal is deposited by electron-beam evaporation, where gold thickness is over $2\text{ }\mu\text{m}$. During the deposition, the sample is mounted on a rotation stage tilted at $\sim 30^\circ$ for maximum sidewall coverage. The P-contact metal is patterned using the liftoff technique. The thermal annealing is done at $400\text{ }^\circ\text{C}$ for 30 s.

After the P-contact metallization is completed, the passive waveguide sections that are not covered by metal are further processed. At this point, the SiN_x layers and the sacrificial InP cap layer are missing from the top surfaces of these waveguide sections, and the InGaAs contact layer is exposed. A thick photoresist is first patterned so that it covers the entire sample, including the metalized waveguide sections, except $\sim 12\text{ }\mu\text{m}$ on each side of the passive waveguide sections. The top InGaAs contact layer is then removed from the ridge tops in these sections using a $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ -based selective wet etch. SiN_x layers protect the top 1.4Q layer on each side of the ridge during this etch step. The same photoresist mask is subsequently re-patterned, and the wafer quarter is subjected to proton implantation. Proton implantation along with the removal of the InGaAs contact layer increase the electrical isolation between neighboring devices and reduces the free-carrier-induced optical loss. The use of proton implantation for neutralizing Zn acceptors, which dominate the carrier-induced loss, is described in [38].

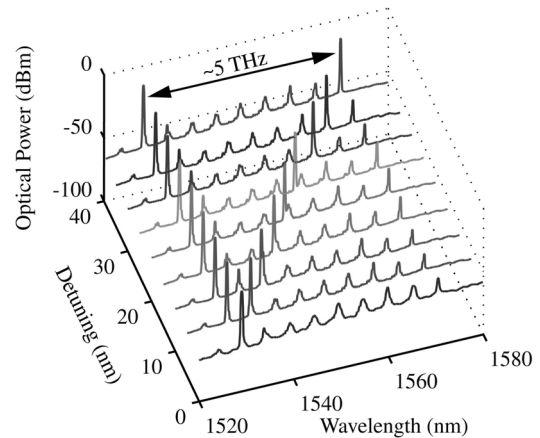


Fig. 7. Optical spectra obtained by heterodyning two integrated, unlocked widely tunable SG-DBR lasers.

Typical passive waveguide loss for this integration platform is $\sim 2.5\text{ dB/mm}$ [37].

The wafer quarter is then thinned to a thickness of $\sim 130\text{ }\mu\text{m}$, for the ease of cleaving. Back-side Ti/Pt/Au metallization is performed using electron-beam evaporation, where the thickness of gold is around $0.3\text{ }\mu\text{m}$. The thermal annealing is done at $380\text{ }^\circ\text{C}$ for 30 s. The sample is cleaved into bars along facets that have the waveguides for input or output coupling to an optical fiber. Anti-reflection coatings are applied to these facets to further reduce reflections. Individual devices are then cleaved and mounted on carriers and wire-bonded.

III. SG-DBR LASER PERFORMANCE

Besides the fact that it is a well established technology, there are at least four important characteristics of the SG-DBR laser that make it a very attractive choice for its use in an OPLL.

First, SG-DBR lasers have in excess of 40 nm of quasi-continuous wavelength tuning range, as shown in the optical spectrum analyzer spectra plotted in Fig. 7. In this figure, one of two on-chip SG-DBR lasers is tuned to a constant wavelength, while the wavelength of the other on-chip SG-DBR laser is detuned away from that wavelength in increments of $\sim 5\text{ nm}$. This wide wavelength tuning range enables the OPLL-PIC to generate a heterodyne beat frequency that spans from DC to over 5 THz .

Second, the FM tuning mechanism of the SG-DBR laser is very efficient. Unlike Distributed Feedback (DFB) lasers, which are tuned by current injection into the laser gain section, in SG-DBR lasers, the tuning is achieved by current injection into a small, separate, passive phase section. The DC FM sensitivity can be as high as 20 GHz/mA for this tuning mechanism, which is over an order of magnitude greater than the $1\text{--}3\text{ GHz/mA}$ DC FM sensitivity reported for a three-section laser optimized for use in OPLL applications [2]. The large FM sensitivity directly translates into a large feedback loop gain and thus helps improve OPLL stability.

Third, an important advantage of the SG-DBR laser is that, unlike in a typical DFB laser, there is no sign change in its FM

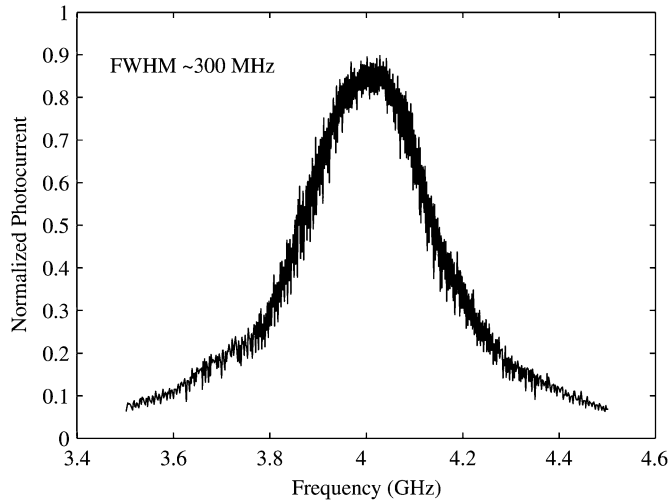


Fig. 8. Composite linewidth measured from the heterodyne beat of the two integrated, unlocked SG-DBR lasers. Resolution and video bandwidths are 2 MHz and 3 kHz, respectively.

phase response. The FM response has a 3 dB bandwidth of ~ 70 MHz, and no phase inversion is observed below this frequency. The phase inversion in a DFB laser occurs within its bandwidth at a frequency where the thermal effect becomes too slow to dominate frequency tuning with the corresponding red shift in the FM response so that frequency tuning becomes dominated by the carrier-injection effect and the corresponding blue shift in the FM response. It is very challenging to implement an OPLL feedback electronic circuit that can compensate for this phase inversion. The absence of phase inversion in the FM phase response of an SG-DBR laser is due to the fact that: 1) the small and efficient phase tuning pads require small currents for tuning, thereby reducing the thermal effects and 2) the phase section is composed of the passive material that has a band gap larger than that of the active material so that the accumulation of carriers is very efficient as they cannot be depleted by stimulated emission.

Fourth, the linewidth of an SG-DBR laser is dominated by low-frequency jitter [39], which is not very difficult to compensate with the large bandwidth of an integrated OPLL, which as we will show below is at least 300 MHz.

We note that the Shawlow–Townes linewidth limit for a typical SG-DBR laser is below 1 MHz [39]. However, the linewidth that we measure with a 30- μ s-delay self-homodyne technique is in the range between 10 and 50 MHz, varying with mirror setting, which is dominated by low-frequency jitter noise. This linewidth would be hard to compensate with an OPLL that is not integrated. Fig. 8 shows the linewidth from the heterodyne beat of two unlocked, integrated SG-DBR lasers obtained by combining their outputs at an offset frequency. The combined linewidth of ~ 300 MHz is measured using an external 20 GHz photodetector and a 20 GHz electrical spectrum analyzer. This wide linewidth is associated with low frequency current noise on the tuning port, and this is normally removed with a large capacitive load in cases where rapid tuning is not required.

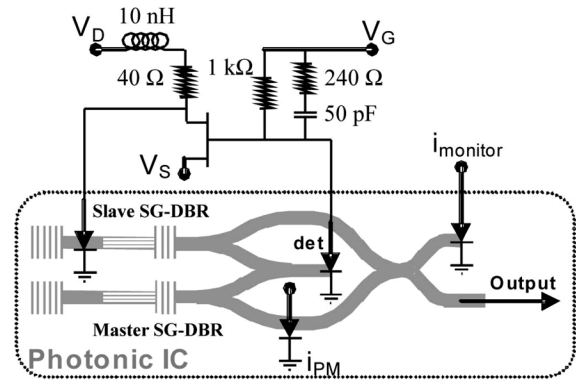


Fig. 9. Schematic of the homodyne locking experimental setup.

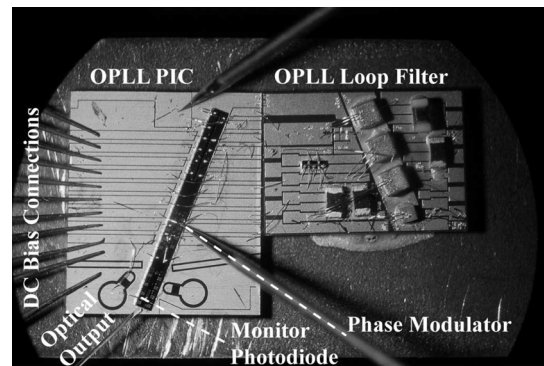


Fig. 10. Optical image of the homodyne locking experimental setup.

IV. PROOF-OF-CONCEPT EXPERIMENTAL RESULTS

We perform two experiments in order to demonstrate proof-of-concept operation of the OPLL: homodyne locking and offset locking of the two monolithically integrated SG-DBR-lasers, as presented in Sections IV-B and IV-C. Before presenting the details of these two experiments, we first present the basics of the electronics used in the feedback loop in Section IV-A.

A. Feedback Loop

Fig. 9 shows the schematic of OPLL-PIC including the feedback electronic circuit when used in the homodyne locking experiment, and Fig. 10 shows the corresponding optical image. The electronic circuit is built around a field effect transistor (FET). One of the two photodetectors in the Middle Section of the OPLL-PIC is used to detect a phase error signal between the two lasers, which is converted to an amplitude error signal in the 2×2 MMI. The reverse-biased current signal generated by this photodetector is amplified by the FET and converted into a forward-biased current signal needed to control the injection of carriers into the phase section of the slave SG-DBR laser.

We design the detector load to provide a second order loop transfer function with lag compensation. The FM response of the SG-DBR laser has a 3-dB point around 70 MHz. The LR circuit that loads the laser phase section is designed to have a zero close to the laser's pole, compensating its FM response and making it a more controllable device. The RC circuit that loads

the photodetector is designed to provide the following function. The larger of the two resistors dominates at frequencies closer to DC and ensures a large locking range. The other resistor dominates at frequencies closer to the 3-dB point and provides the desired zero needed to improve the stability of the loop for the higher frequencies where the gain becomes unity. The resulting loop bandwidth that we measure is ~ 300 MHz. Similar to a voltage-controlled oscillator in an RF PLL, the laser itself acts as an integrator, which means that the rest of the electronics is required to provide a single pole to realize a second-order loop. More details on the issues pertaining to the feedback loop design can be found in [40].

B. Homodyne Locking

As mentioned above, the schematic and optical image corresponding to the homodyne locking experiment are shown in Figs. 9 and 10, respectively. No current is applied to the back-side or the front-side mirror of the two SG-DBR lasers, so that they lase at their untuned wavelengths, which are close to 1542 nm. The random phase variation between the two lasers translates into an intensity modulated error signal at the output of the 2×2 MMI in the Middle Section of the OPLL-PIC and finally into a current error signal at the output of one of the photodetectors that is connected to the feedback loop. The error signal then passes through the electronic circuit and tunes the frequency of the slave laser so that it is matched to that of the master laser, where the slave laser effectively plays a role of a current-controlled oscillator.

In order to bring the OPLL from an unlocked state into a locked state, we inject appropriate bias currents into the phase section of the one of the SG-DBR laser until its frequency is within the feedback loop bandwidth, i.e., ~ 300 MHz, to that of the second SG-DBR laser. The bias current is adjusted until the noise spectrum measured at the optical output of the OPLL-PIC changes as shown in Fig. 11, which indicates that the OPLL-PIC has become locked. Fig. 11 also reveals the expected presence of the 300 MHz resonance frequency peak, above which the OPLL provides a positive rather than negative feedback and becomes unstable. The data is acquired using an external 20 GHz photodetector and a 20 GHz electrical spectrum analyzer. The uncompensated low-frequency noise below the resonance frequency peak is mainly due to OPLL-PIC's AM noise that can be effectively cancelled using feedback from a balanced photodetector pair (implemented on the PIC, but not used here) rather than a single photodetector.

To further confirm the homodyne locking, we inject current into one of the modulators and continuously adjust the phase of the light from one of the SG-DBR lasers. This modulator is part of the waveguide that directs light toward the 2×2 MMI in the Output Section of the OPLL-PIC and is not the feedback-loop. This phase modulator allows us to independently modulate the phase of one SG-DBR laser output while leaving the phase of the second SG-DBR laser unchanged. When the OPLL is in the locked state, the two lasers are coherent with respect to each

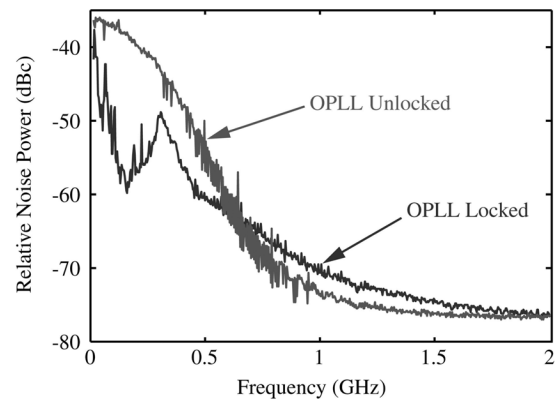


Fig. 11. Noise spectra measured at the optical output of the OPLL-PIC in the homodyne locking experiment. Resolution and video bandwidths are 2 MHz and 10 kHz, respectively.

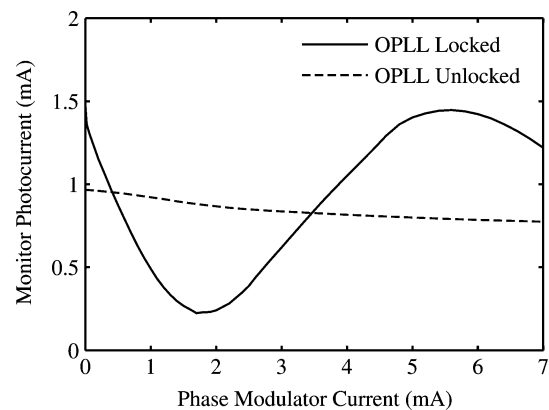


Fig. 12. Phase-to-amplitude modulation conversion observed for the locked and unlocked states of the OPLL for homodyne locking of the two SG-DBR lasers.

other. By changing the phase on one of the lasers, the interference between the two lasers in the 2×2 MMI in the Output Section of the OPLL-PIC shows the characteristic interference that is observed from a Mach-Zehnder Interferometer (MZI), which converts phase modulation to amplitude modulation. When the OPLL is not locked, the two lasers are not coherent with respect to each other and their interference in the 2×2 MMI does not exhibit the phase to amplitude modulation response that is characteristic of an MZI.

Fig. 12 illustrates this behavior for both locked and unlocked states of the OPLL. In both cases, we see a small intensity modulation characteristic for our modulators when operated in the forward bias. Also, the half-wave current (I_{π}) needed for switching the interference between “on” and “off” states is ~ 4 mA, which is consistent with other measurements performed on similar phase modulators. The extinction ratio (~ 8 dB) observed for the constructive versus destructive interference is limited by unequal optical powers reaching the 2×2 MMI, phase noise of the lasers, weak multimoding in the waveguides, and polarization mismatch. Because the SG-DBR lasers emit quasi-TE-polarized light and all of the integrated optical components are designed to be polarization maintaining, the

polarization mismatch is expected to have a small effect on the extinction ratio. Due to the present probing station limitations, i.e., limited number of bias controls, in this proof-of-concept study, we did not bias the SOAs independently nor did we tune the MMI splitters in order to overcome the possible optical power mismatch. This issue will be addressed more systematically in a future study.

C. Offset Locking

The same PIC and electronic circuit that were used in the homodyne experiment are also used in the offset locking experiment. To demonstrate offset-locking of the two monolithically integrated SG-DBR lasers, we apply a reverse bias phase modulation to one of the modulators that is connected to the output of the 2×2 MMI in the Middle Section of the OPLL-PIC and is a part of the feedback loop, as shown in Fig. 1. As this phase modulator output is only connected to the integrated detector pair used for the feedback circuit, the OPLL-PIC output signal does not contain any modulation sidebands. In this case, we use the reverse bias modulation based on the Franz-Keldysh effect because the gigahertz-range modulation frequency that we need far exceeds the bandwidth (~ 100 MHz) of the modulator in the forward-biased current-injection mode. In our offset-locking scheme, the carrier frequencies from both lasers are simultaneously modulated, which generates two modulation sidebands corresponding to either laser's carrier frequency. When the frequency separation between the two SG-DBR lasers equals the modulation frequency, the detected photocurrent will contain a phase-dependent DC component, and sideband locking of the two lasers becomes possible. Mixing of the two laser frequencies and their sidebands occurs in the photodetector, which generates a corresponding current error signal to the feedback electronics and the phase section of the slave laser whenever there is a random phase walk-off between a center frequency of one laser and a sideband of the other laser. The power in the sidebands is smaller in comparison to the power at the center frequencies of the laser. Consequently, the extinction ratio of the corresponding interference is smaller than for the homodyne OPLL, producing a weaker error signal. To compensate for this, to generate as strong modulation sidebands as possible, the power applied to the modulator used in offset locking is between 10 and 15 dBm.

Fig. 13(a) and (b) show an oscilloscope trace of the OPLL-PIC's optical output before and after 5 GHz offset locking of the two SG-DBR lasers, respectively. The oscilloscope is triggered by the 5 GHz modulating signal. Before locking, the phase of the beat varies randomly and only an envelope of the beat is observed in Fig. 13(a). After phase-locking, a coherent beat signal is generated, as observed by the oscilloscope trace in Fig. 13(b).

In addition to the time domain representation of the locked beat shown in Fig. 13(b), in Fig. 14, we plot the corresponding frequency spectrum obtained using an external 20 GHz photodetector and a 20 GHz electrical spectrum analyzer. As expected, the spectrum is centered at the 5 GHz modulation frequency, surrounded by two peaks that are offset by ~ 300 MHz, corresponding to the bandwidth of the feedback loop. From

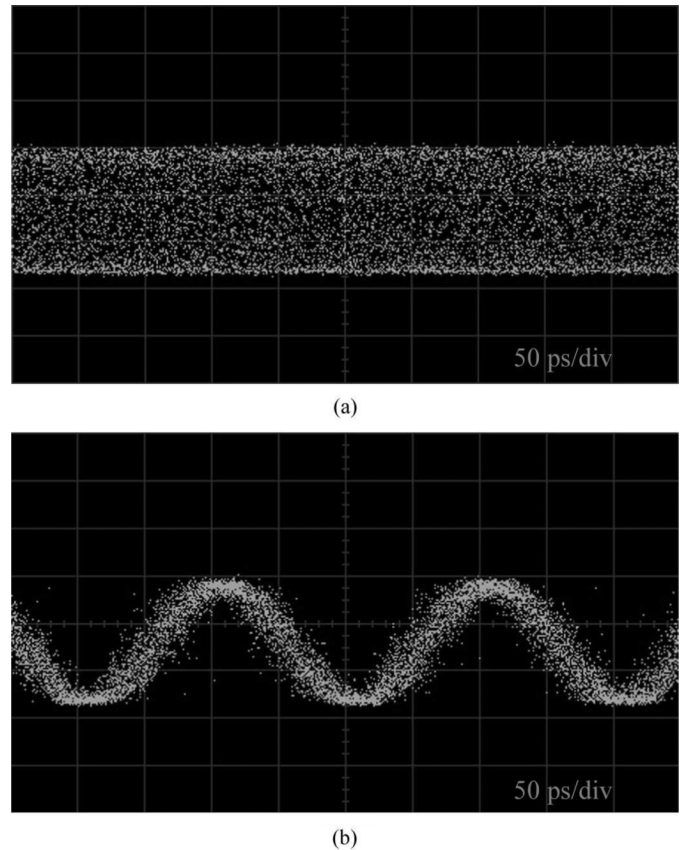


Fig. 13. Oscilloscope traces observed at the optical output of the OPLL-PIC in the heterodyne locking experiment when the OPLL is (a) unlocked and (b) locked.

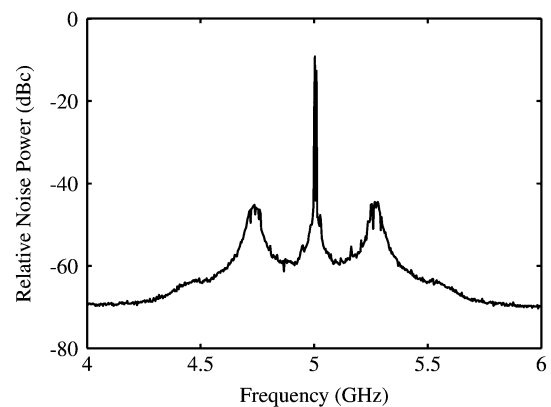


Fig. 14. Noise spectrum measured at the optical output of the OPLL-PIC in the heterodyne locking experiment. Resolution and video bandwidths are 2 MHz and 10 kHz, respectively.

the spectrum in Fig. 14, we calculated the phase error variance to be 0.03 rad^2 by dividing the noise power within the 2 GHz span by the signal power [3]. Our result is comparable to the state-of-the-art result in [2], where phase error radiance of 0.05 rad^2 in a 1 GHz bandwidth has been reported for an OPLL based on miniature bulk optics designed for use in a microwave photonic transmitter. We obtained similar results for different offset frequencies up to 15 GHz.

V. CONCLUSION

In this work, we have successfully demonstrated the first monolithically integrated optical phase-locked loop photonic integrated circuit in which all of the optical components are integrated on the same InP platform, including: master and slave SG-DBR lasers, high-speed modulators, high-speed photo detectors, multimode interference couples/splitters, as well as interconnecting optical waveguides. Compared to the alternatives, monolithic integration of an optical phase-locked loop is expected not only to provide a competitive performance, but also to make the technology more easily packaged and less expensive.

We have shown that, via monolithic integration, the phase-locked loop can be made sufficiently compact, and thus have a sufficiently wide bandwidth (300 MHz), to allow use of wide linewidth semiconductor lasers. We have further demonstrated suitability of SG-DBR lasers to be used as the master laser and the slave laser, i.e., current-controlled oscillator, in this application. Most importantly, unlike the DFB laser, the slave SG-DBR laser does not suffer from a phase inversion in the FM frequency response, which is not easily compensated by the loop filter electronics. In addition, the slave SG-DBR laser offers a large phase tuning sensitivity, improving the gain and stability of the phase-locked loop. We have also shown that the detuning range of the master and slave SG-DBR lasers exceeds 5 THz, which enables the phase-locked loop to generate phase-stable optical beats at very high frequencies. This beat can be modulated with on-chip high-speed modulators and also converted into an electrical signal with on-chip high-speed photodetectors.

We have performed two experiments to demonstrate the proof-of-concept operation of the monolithically integrated PLL: homodyne locking and offset (5 GHz offset) locking of the master and slave SG-DBR lasers. We have shown that a simple electronic filter is sufficient to enable locking. The future versions of optical phase-locked loop will utilize both feedback photodetectors as a balanced pair in order to reduce laser amplitude noise. In addition, integrated feedback electronics will be implemented to further increase the bandwidth of the loop. Both of the changes are expected to significantly reduce the phase noise of the PLL.

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