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THz Bipolar Transistors: Design and Process Technologies

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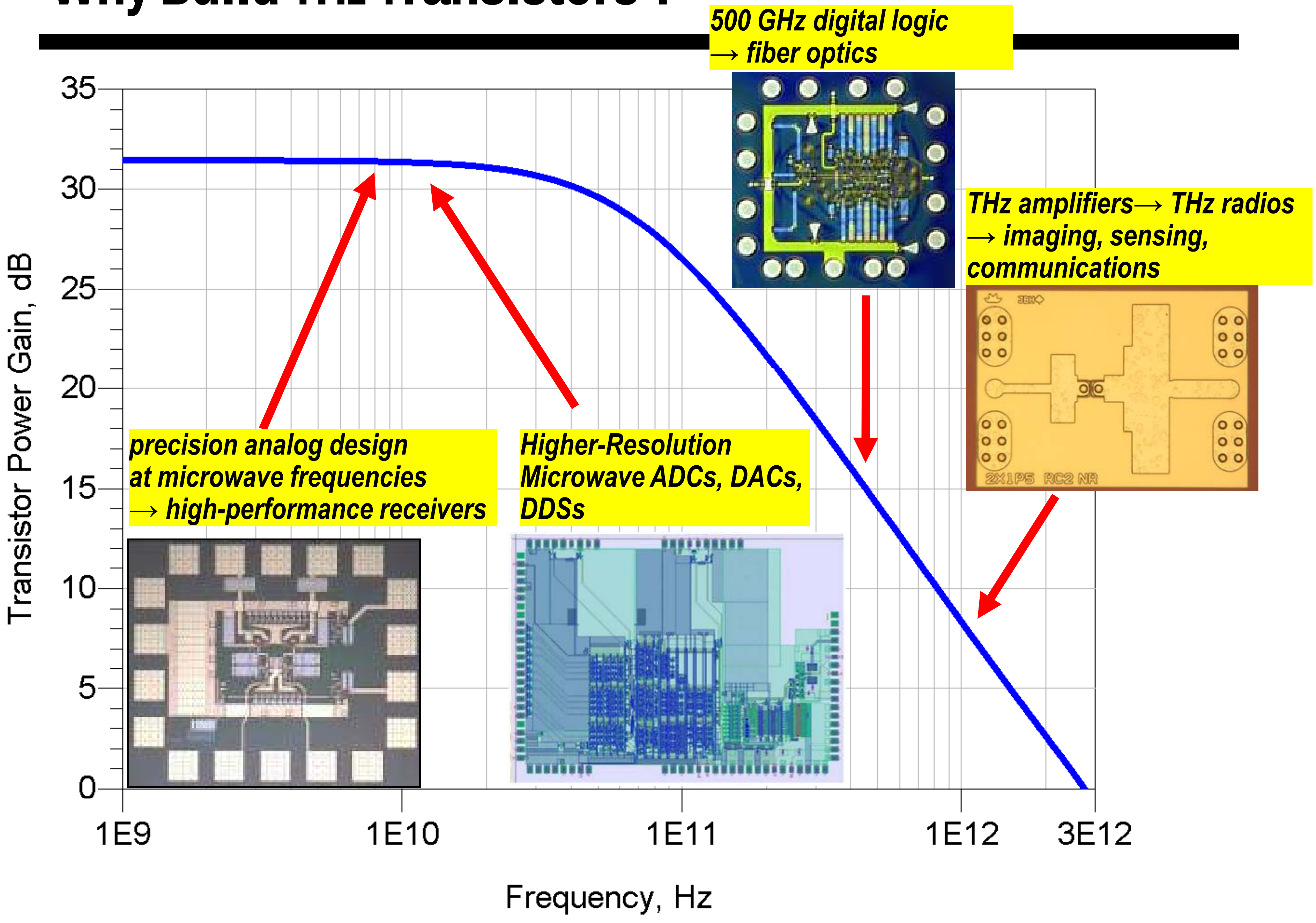
Why
THz Transistors ?

Why Build THz Transistors ?



500 GHz digital logic
→ fiber optics

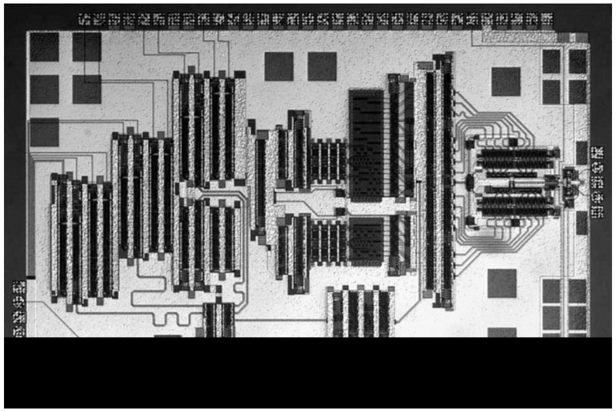
THz amplifiers→ THz radios
→ imaging, sensing,
communications

precision analog design
at microwave frequencies
→ high-performance receivers

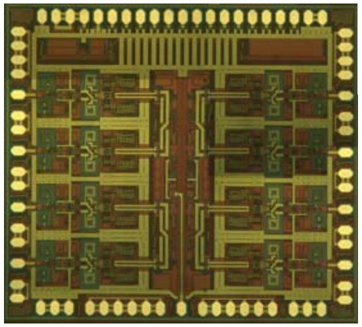
Higher-Resolution
Microwave ADCs, DACs,
DDSs

Why Bipolars for Fast Analog Applications ?

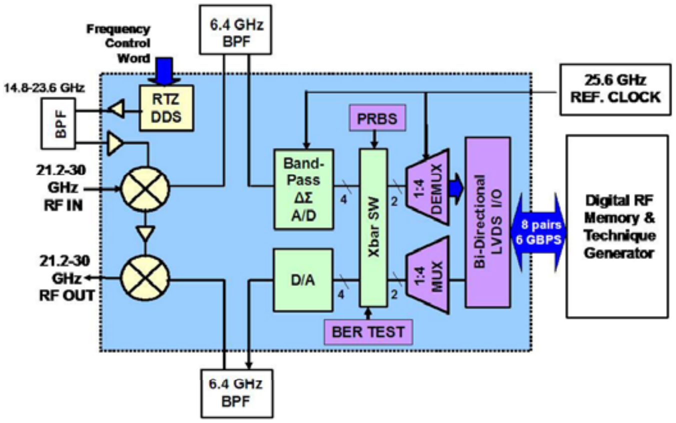
digital frequency synthesis



mm-wave
phased arrays



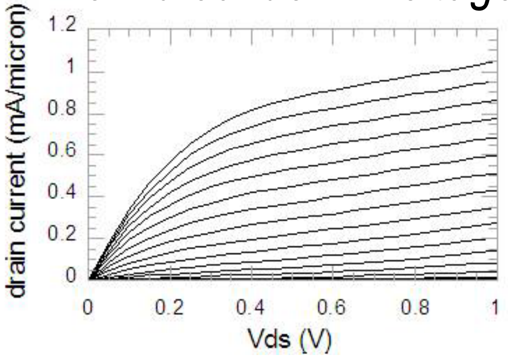
jammer on chip



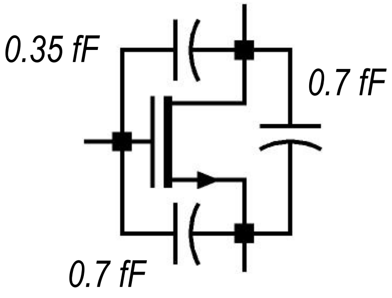
high resolution ADCs and DACs for 2-20, 38 GHz

CMOS does not serve all ICs

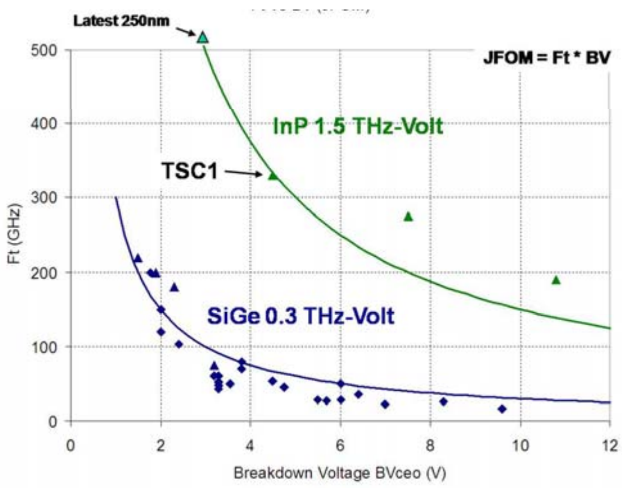
low analog gain
low analog precision
low breakdown voltage



high C_{ds}/C_{gs}, high C_{gd}/C_{gs}
→ less bandwidth
than f_τ suggests

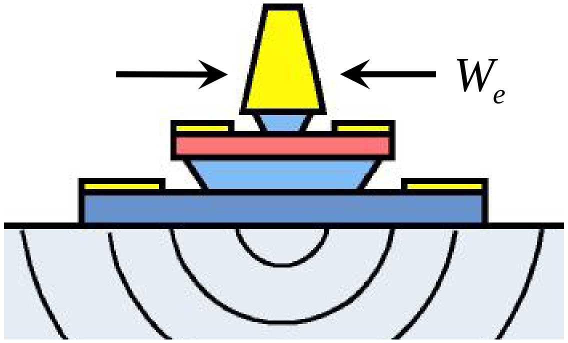


BJTs, particularly InP,
have high breakdown



How to Make
THz Transistors

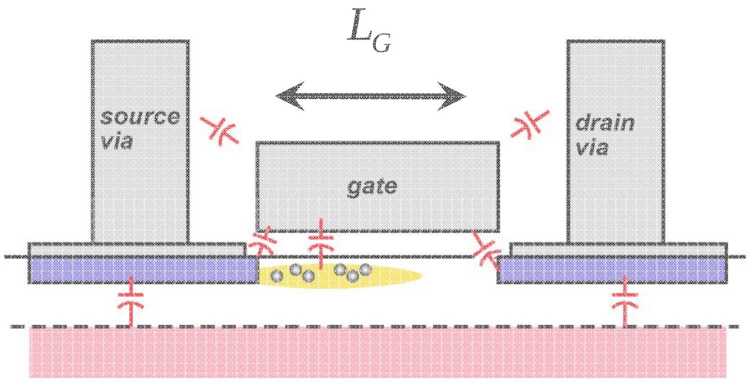
Changes required to double transistor bandwidth



(emitter length L_E)

HBT parameter	change
emitter & collector junction widths	decrease 4:1
current density (mA/μm^2)	increase 4:1
current density (mA/μm)	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1

nearly constant junction temperature → linewidths vary as (1 / bandwidth)^2



(gate width W_G)

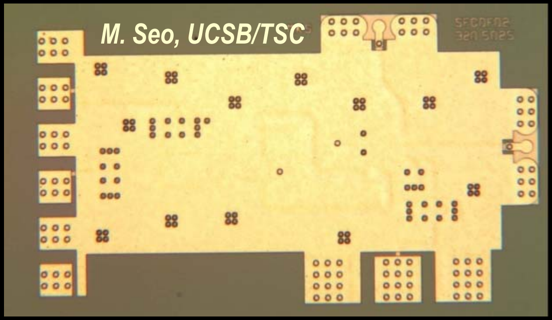
FET parameter	change
gate length	decrease 2:1
current density (mA/μm), g_m (mS/μm)	increase 2:1
channel 2DEG electron density	increase 2:1
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
channel thickness	decrease 2:1
channel density of states	increase 2:1
source & drain contact resistivities	decrease 4:1

constant voltage, constant velocity scaling

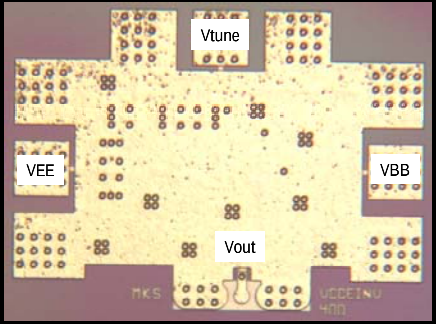
fringing capacitance does not scale → linewidths scale as (1 / bandwidth)

256 nm Generation
InP HBT

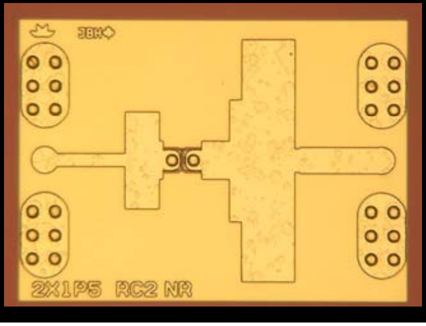
340 GHz dynamic frequency divider



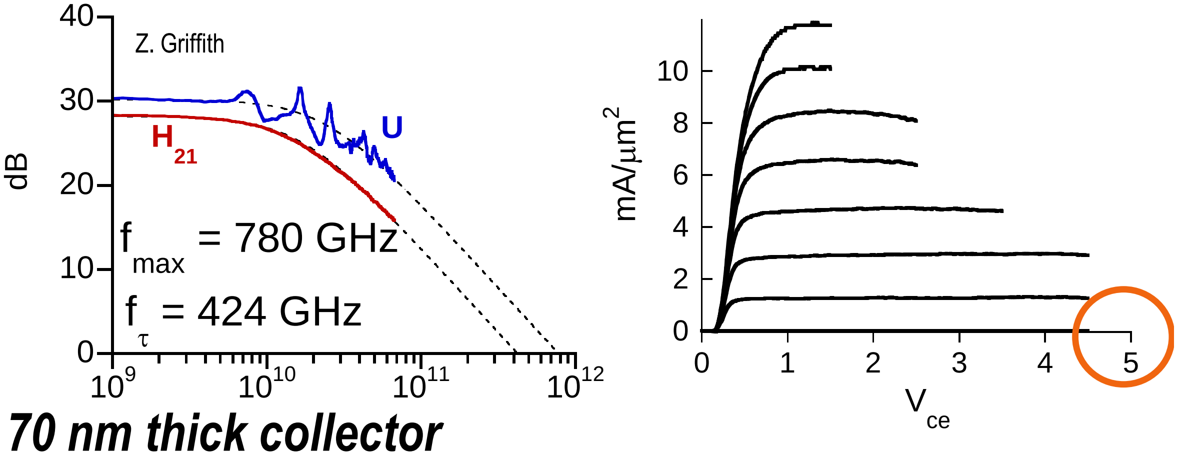
340 GHz VCO *M. Seo, UCSB/TSC*



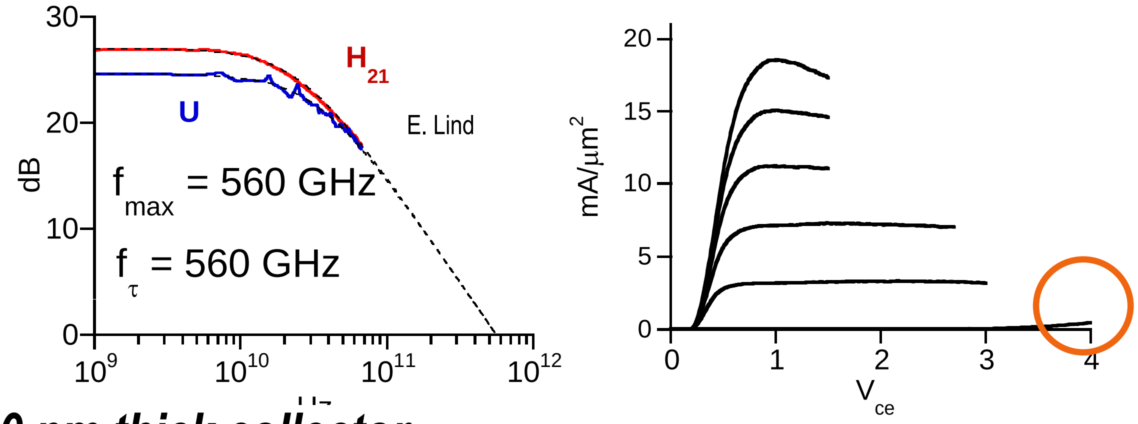
324 GHz amplifier *J. Hacker, TSC*



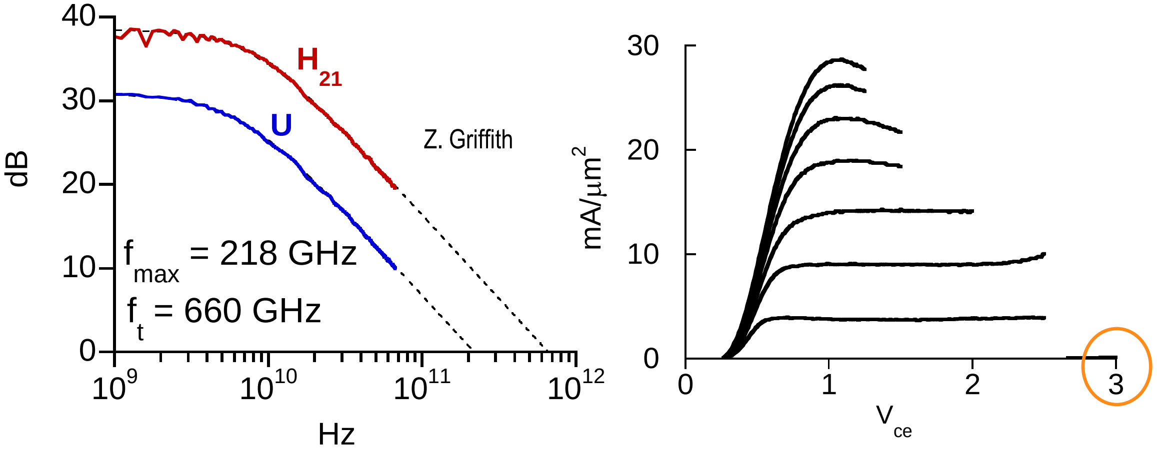
150 nm thick collector



70 nm thick collector

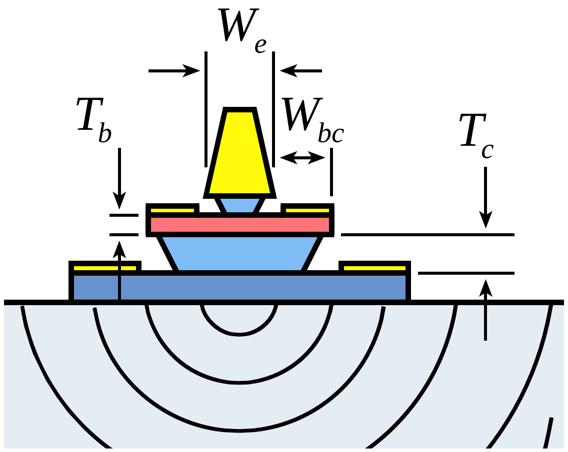


60 nm thick collector



InP Bipolar Transistor Scaling Roadmap

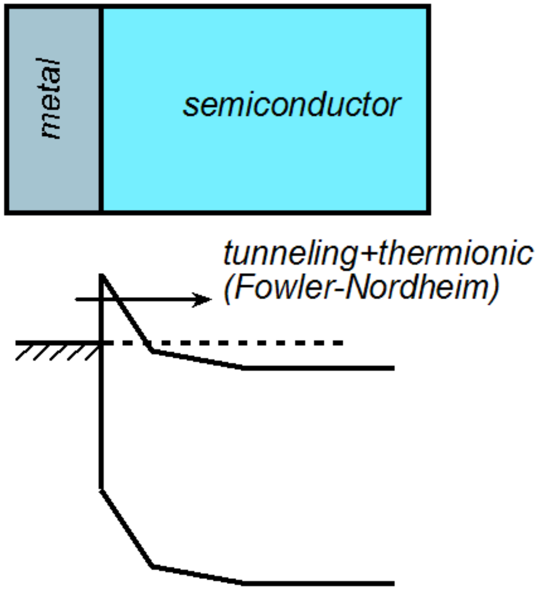
emitter	512	256	128	64	32 nm width
	16	8	4	2	1 $\Omega\cdot\mu m^2$ access ρ
base	300	175	120	60	30 nm contact width,
	20	10	5	2.5	1.25 $\Omega\cdot\mu m^2$ contact ρ
collector	150	106	75	53	37.5 nm thick,
	4.5	9	18	36	72 mA/μm^2 current density
	4.9	4	3.3	2.75	2-2.5 V, breakdown
f_τ	370	520	730	1000	1400 GHz
f_{max}	490	850	1300	2000	2800 GHz
power amplifiers	245	430	660	1000	1400 GHz
digital 2:1 divider	150	240	330	480	660 GHz



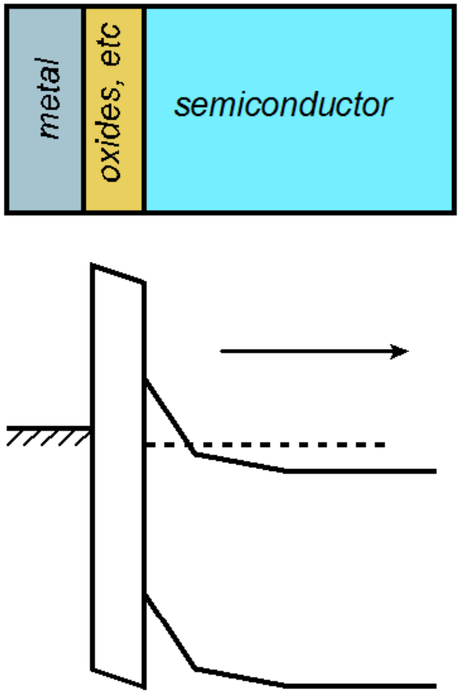
Conventional ex-situ contacts are a mess

THz transistor bandwidths: very low-resistivity contacts are required

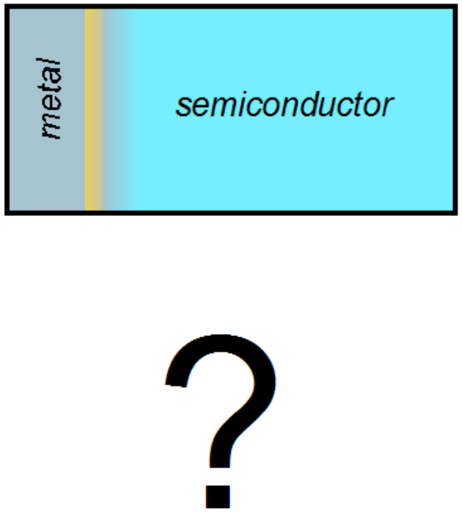
textbook contact



with surface oxide



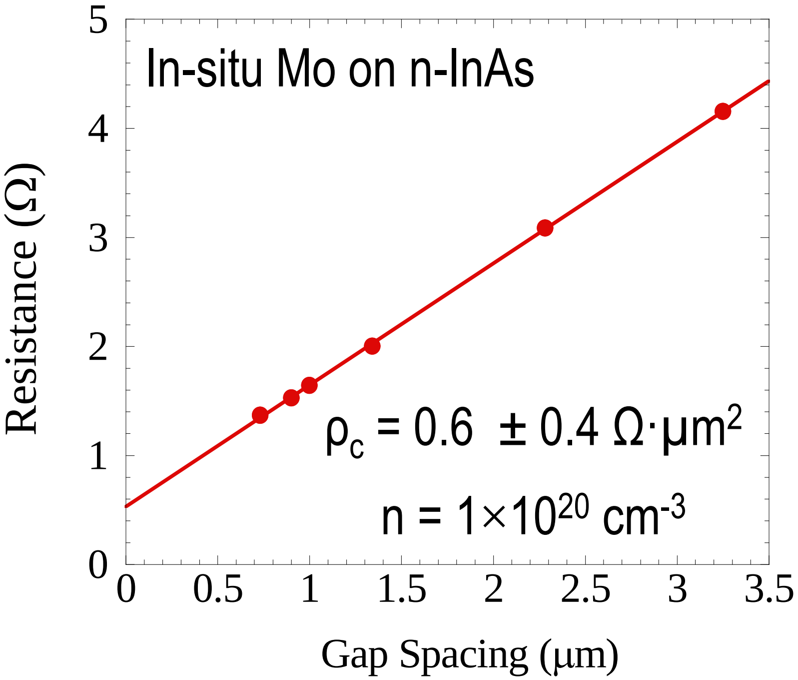
with metal penetration

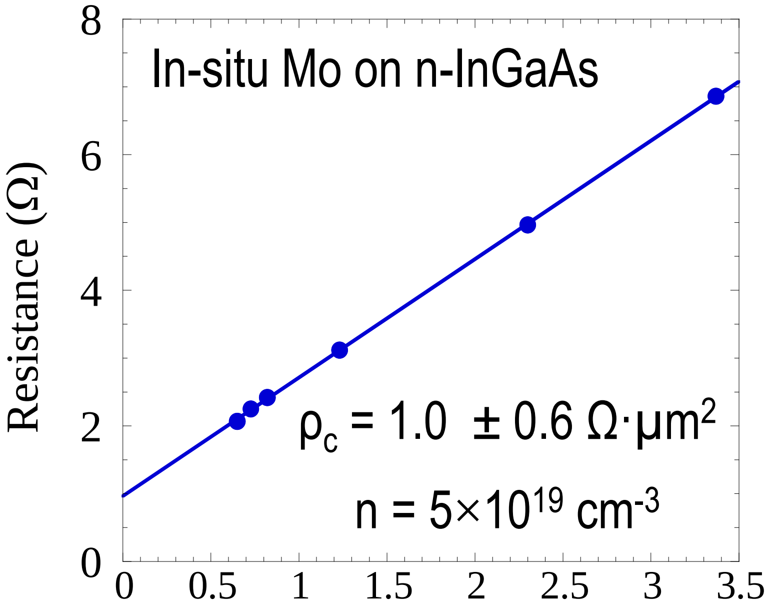


Interface barrier → resistance

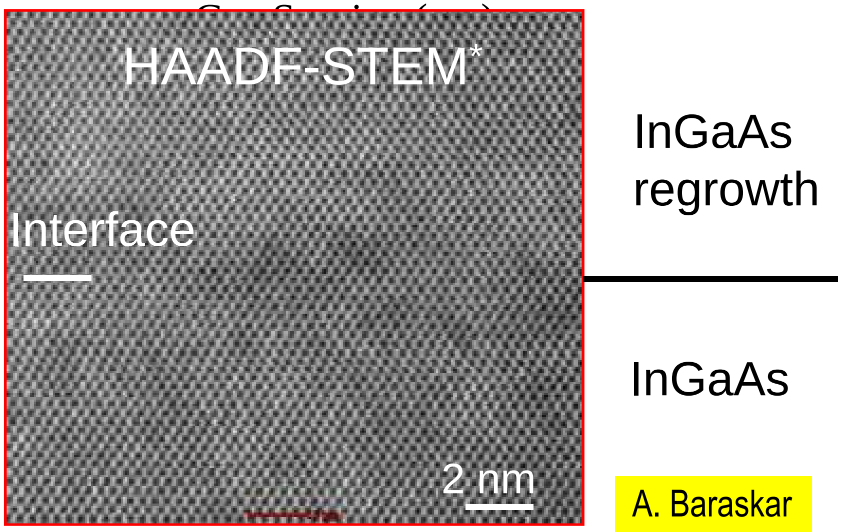
Further intermixing during high-current operation → degradation

In-Situ Refractory Ohmics on Regrown N-InGaAs





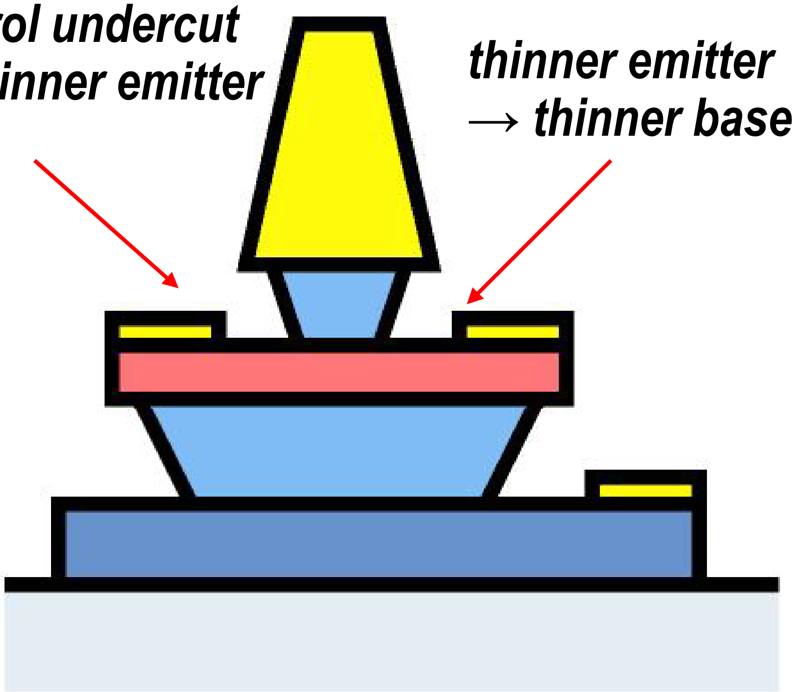
In-situ emitter contacts good enough for *64 nm* node



A. Baraskar

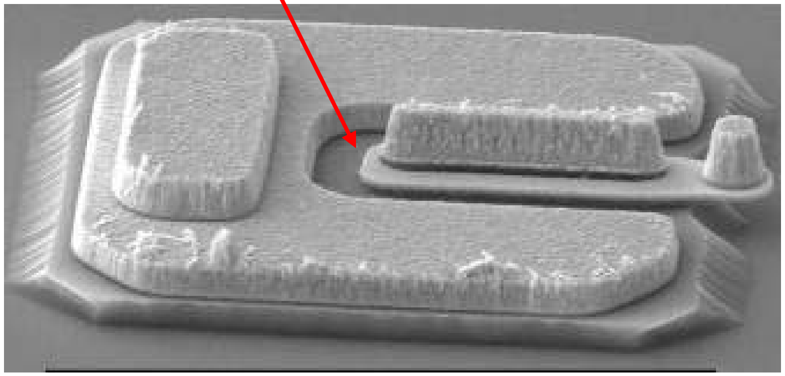
TEM by Dr. J. Cagnon, Stemmer Group, UCSB

Process Must Change Greatly for 128 / 64 / 32 nm Nodes



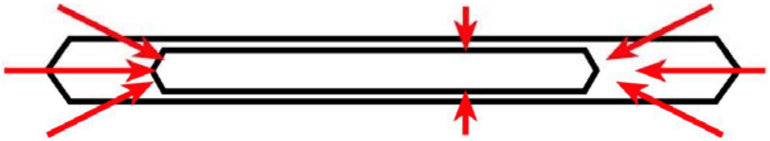
control undercut
→ thinner emitter

thinner emitter
→ thinner base metal



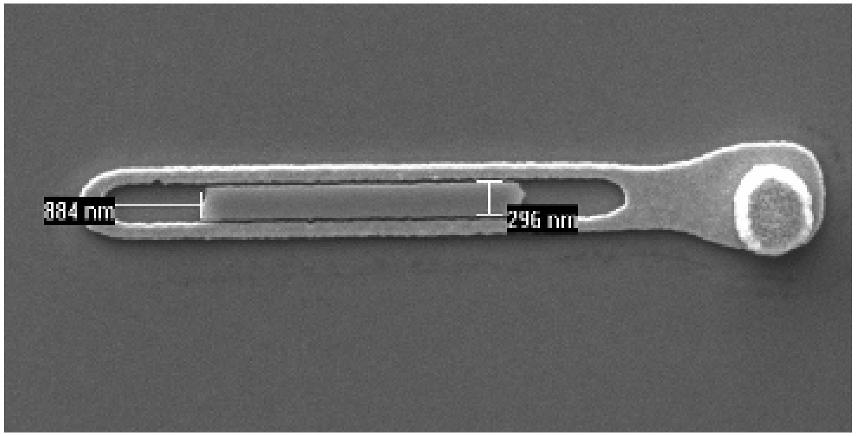
thinner base metal
→ excess base metal resistance

Undercutting of emitter ends



{101}A planes: fast

{111}A planes: slow



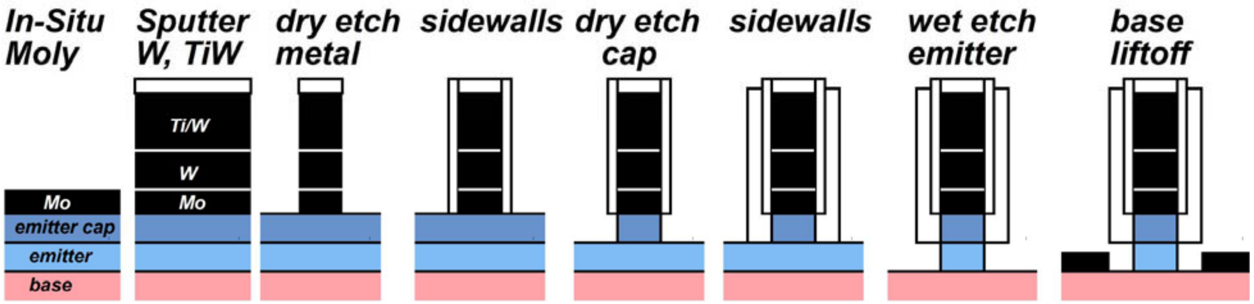
128 / 64 nm process: Dry-Etched Emitter Metal

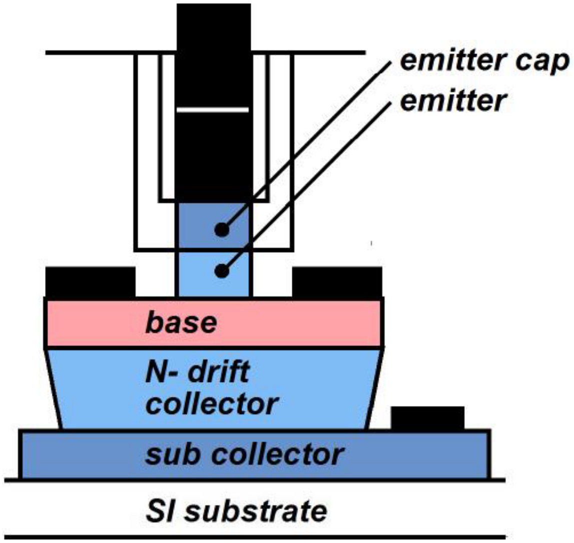
In-situ MBE emitter contacts:
refractory→ high J
low contact ρ: ~0.7 Ω-μm^2

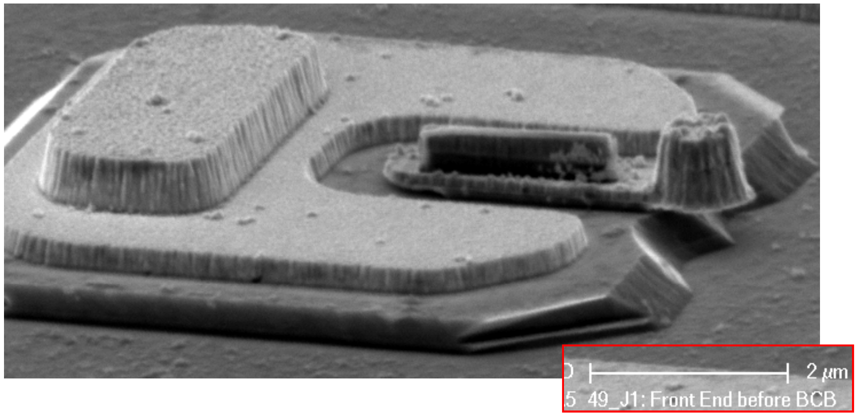
Refractory emitter contact
dry-etched→ nm resolution
refractory→ high current

Wet/dry etched emitter
dry-etched→ nm resolution

conventional base liftoff
high penetration→ thick bases
moderate contact ρ ~4Ω-μm^2
yield issues ?

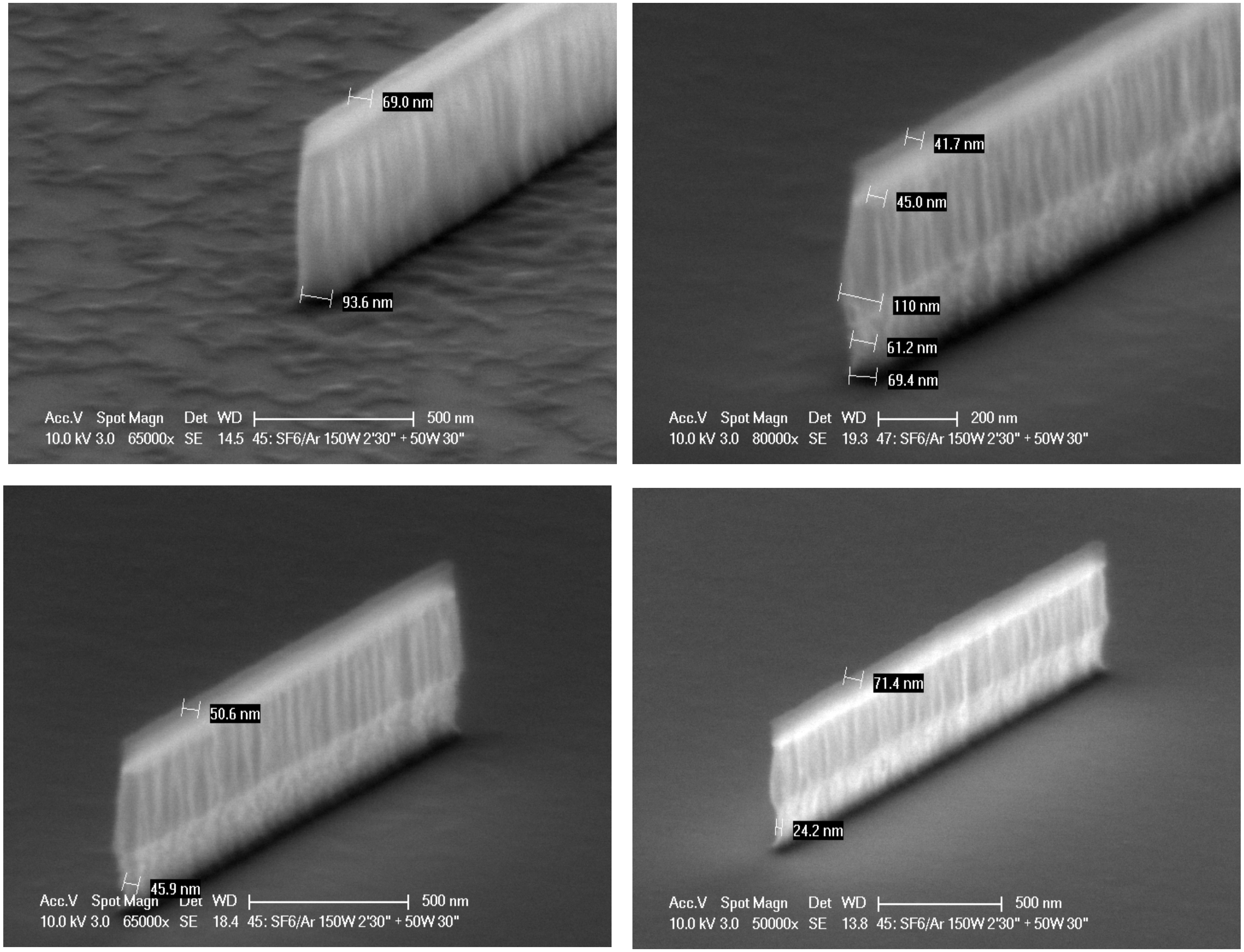






V. Jain
E. Lobisser

Dry-Etched W/TiW Emitter Contact Process



Sputtered W/ $Ti_{0.1}W_{0.9}$ process

Vertical ICP etch profile

Low-stress film

Good adhesion between layers

Refractory Metals

W/TiW bilayer: stress and etch bias compensation

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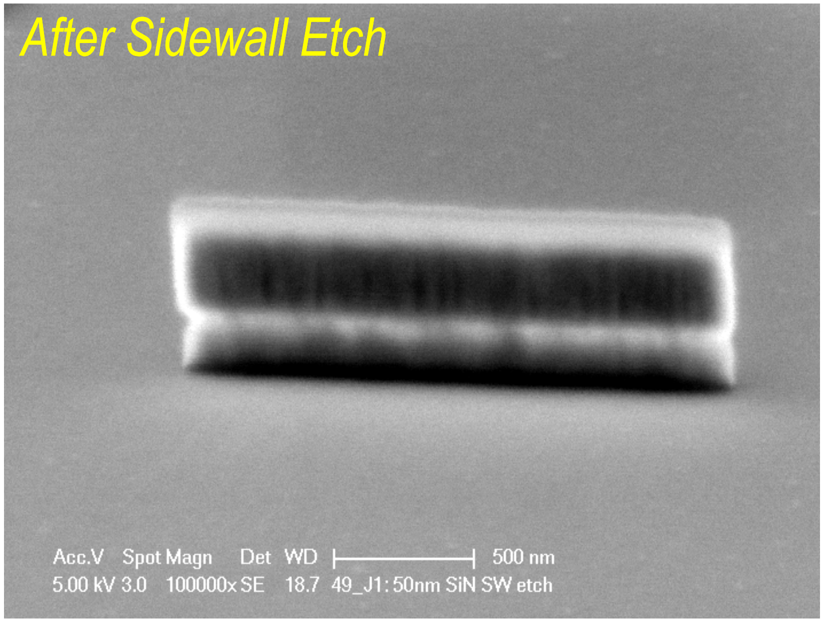
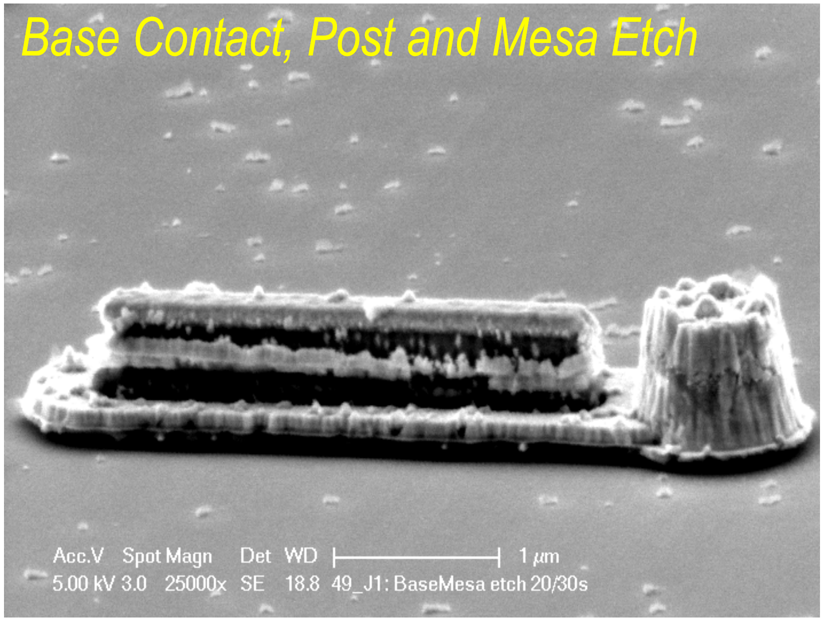
E. Lobisser

Sub-100 nm devices: lifted-off base metal

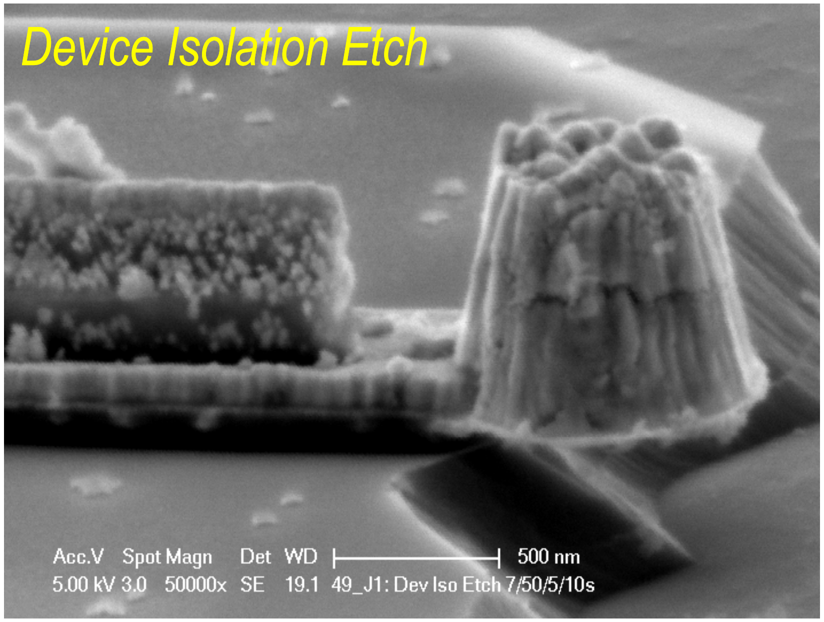
V. Jain
E. Lobisser



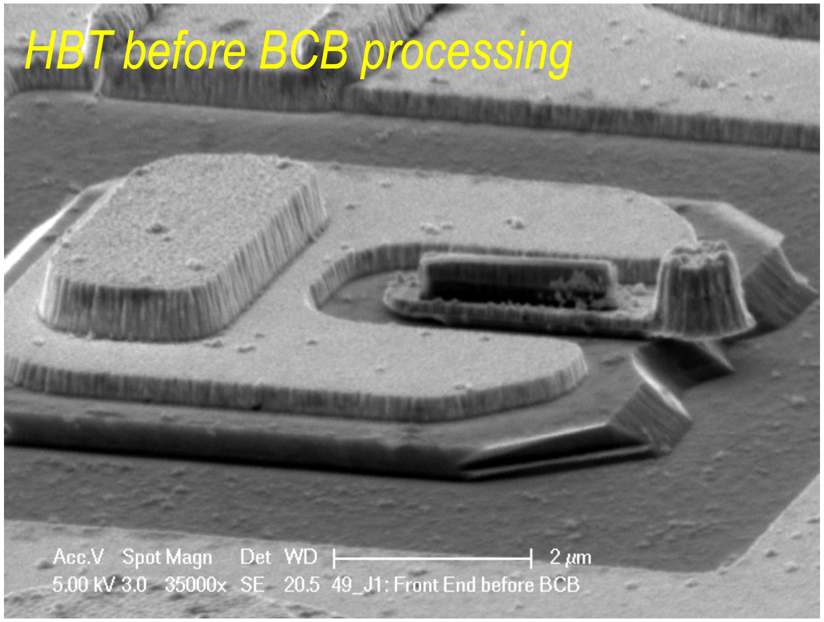
After Sidewall Etch



Base Contact, Post and Mesa Etch



Device Isolation Etch



HBT before BCB processing

Sub-100 nm devices: lifted-off base metal

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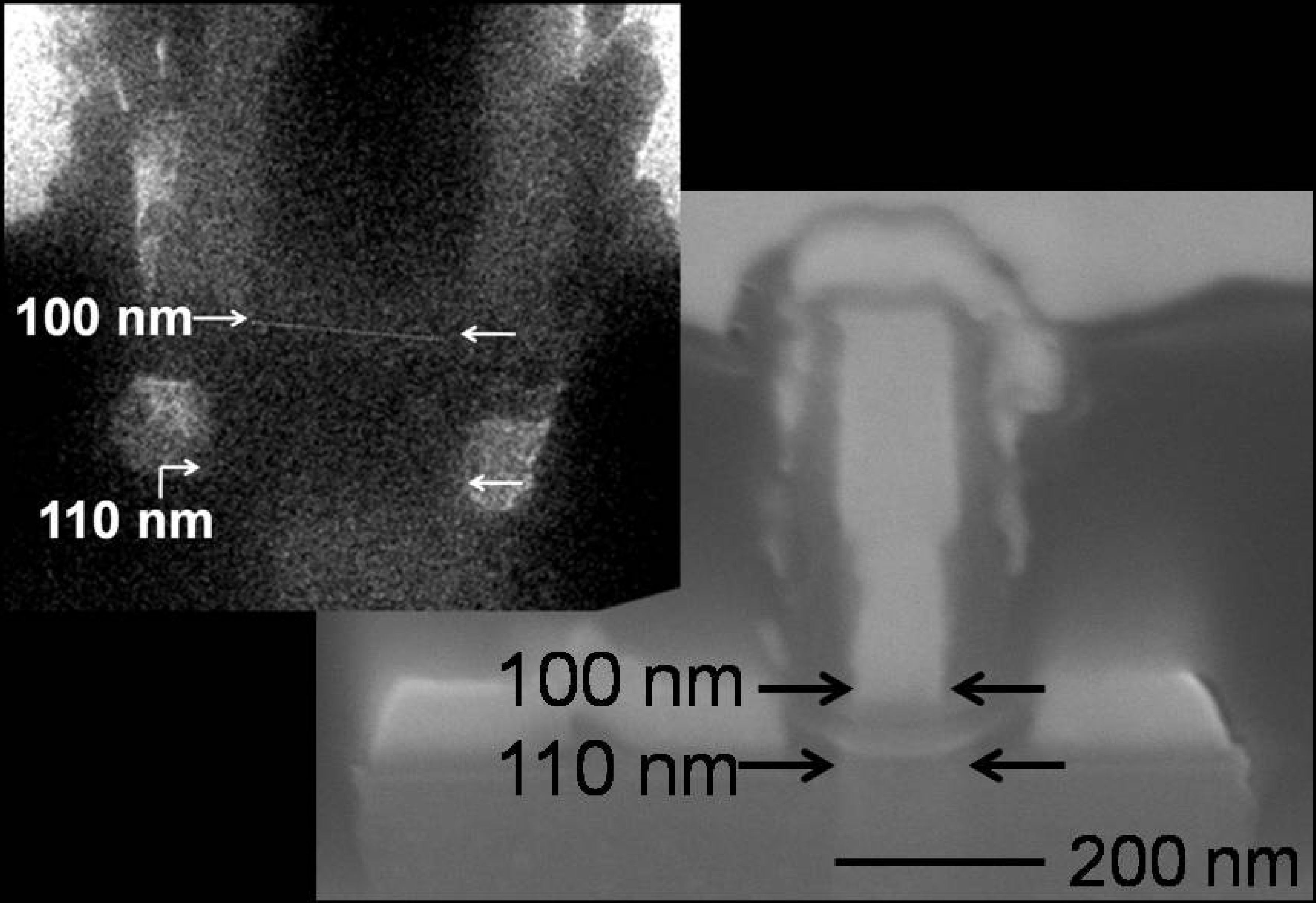

Sub-100 nm devices: lifted-off base metal

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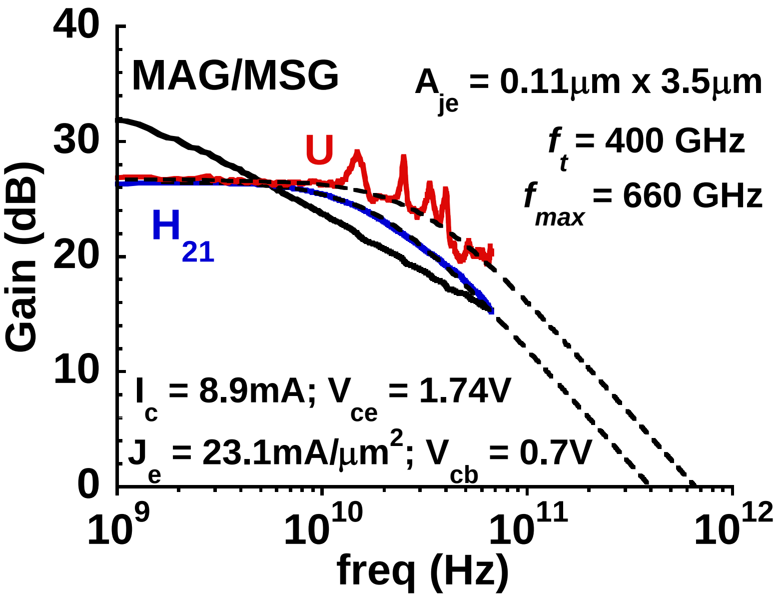
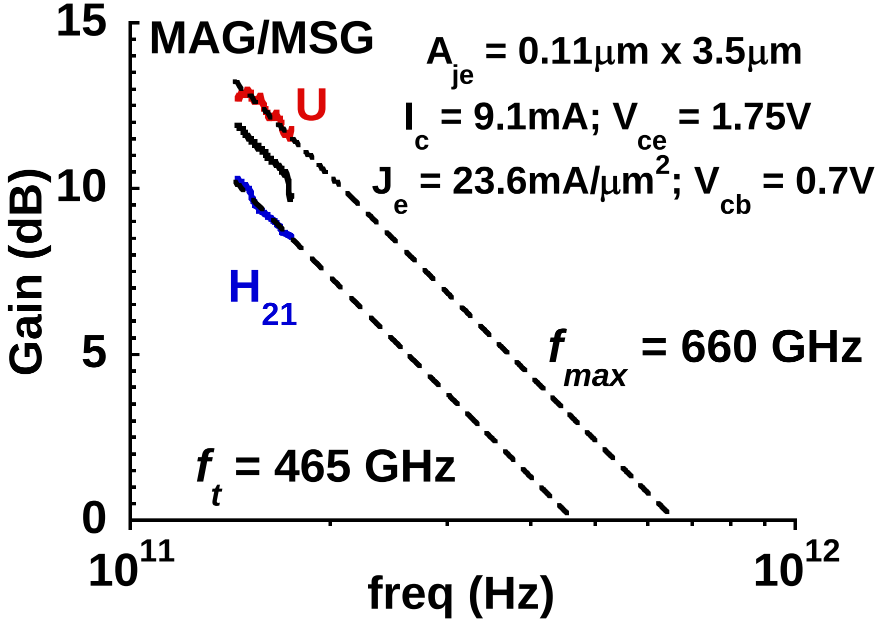
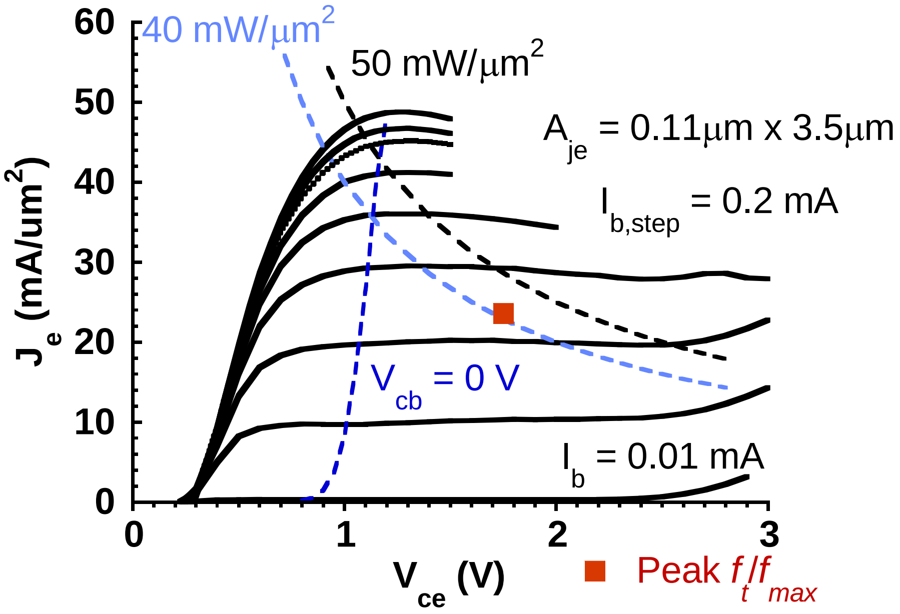
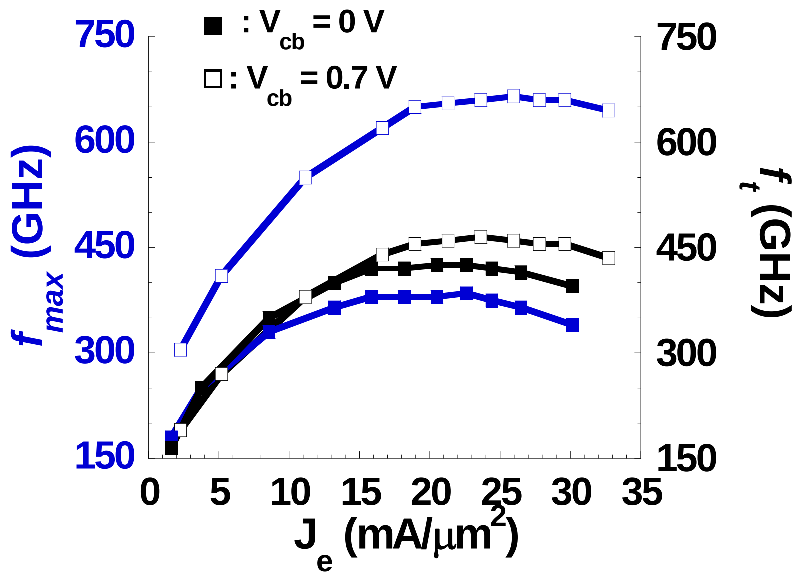








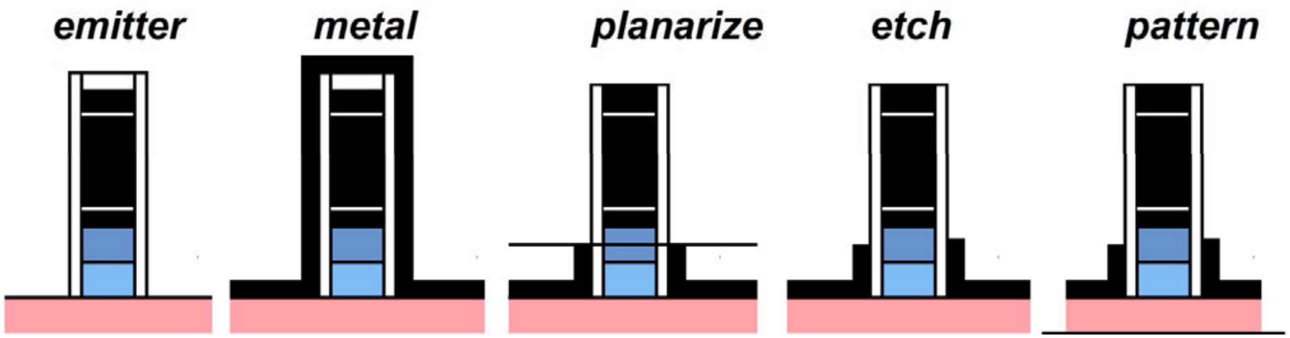
128 / 64 nm process: Sputtered Refractory Base

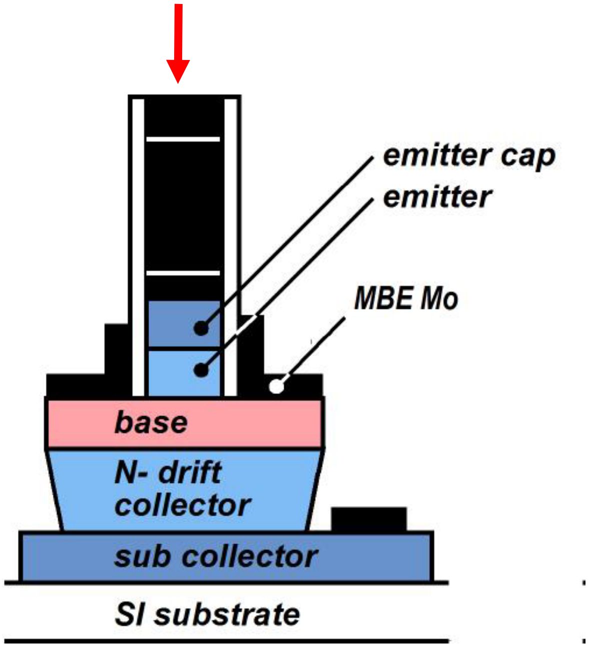
In-situ MBE emitter contacts:
refractory→ high J
low contact ρ: ~0.7 Ω-μm^2

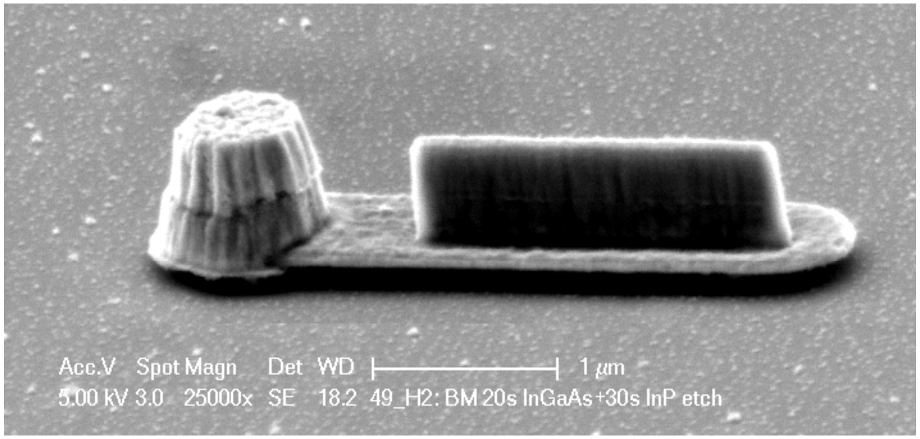
Refractory emitter contact
dry-etched→ nm resolution
refractory→ high current

Wet/dry etched emitter
dry-etched→ nm resolution

Refractory base contacts
low penetration→ thin bases
low contact ρ ~2.5 Ω-μm^2
self-aligned/ liftoff-free







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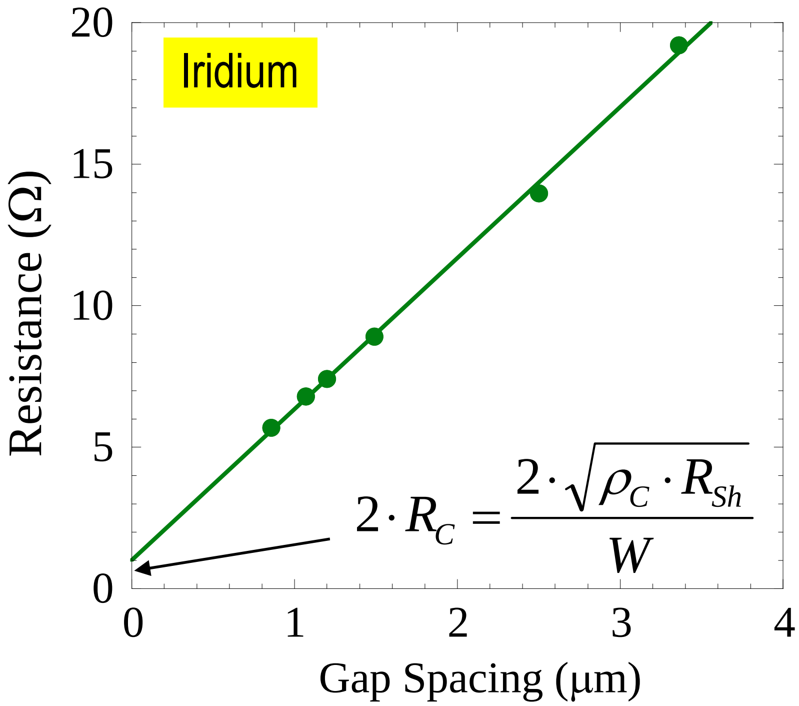
E. Lobisser

In-Situ Refractory Ohmics on P-InGaAs

Metal Contact	ρ_c (Ω-μm^2)	ρ_h (Ω-μm)
In-situ Ir	**1.0 ± 0.7**	**11.5 ± 3.3**

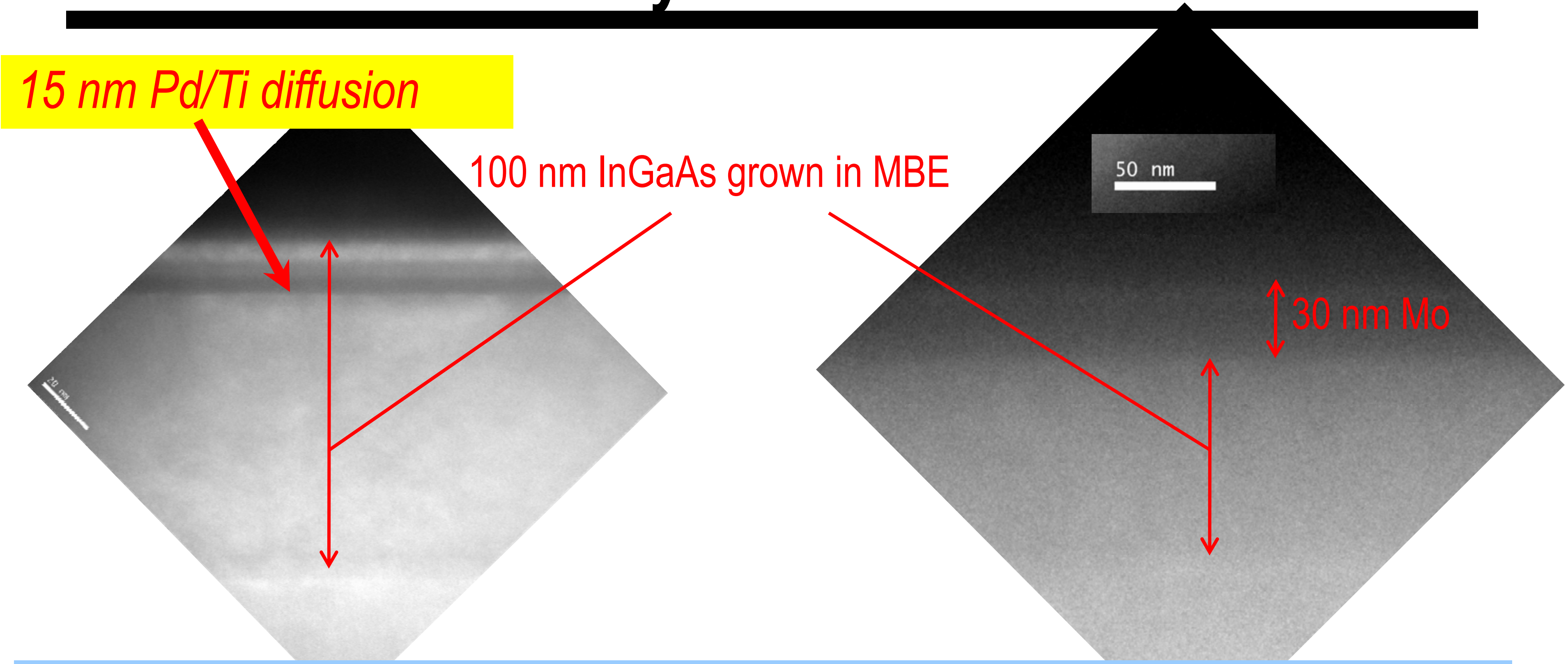


$$2 \cdot R_C = \frac{2 \cdot \sqrt{\rho_C \cdot R_{Sh}}}{W}$$

In-situ base contacts good enough for *32 nm* node
Remaining work: contacts on *processed* surfaces
contact thermal stability & reliability

A. Baraskar

Benefits of refractory base contacts



After 250°C anneal, Pd/Ti/Pd/Au *diffuses* 15nm into semiconductor

deposited Pd thickness: 2.5nm

base now 30 nm thick: observed to degrade with thinner bases

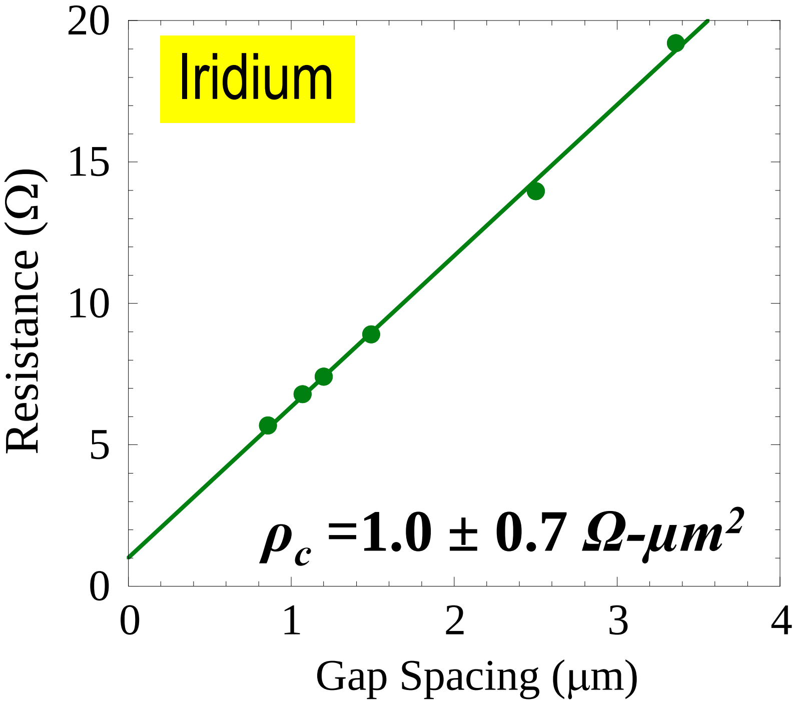
Refractory Mo contacts *do not diffuse measurably*

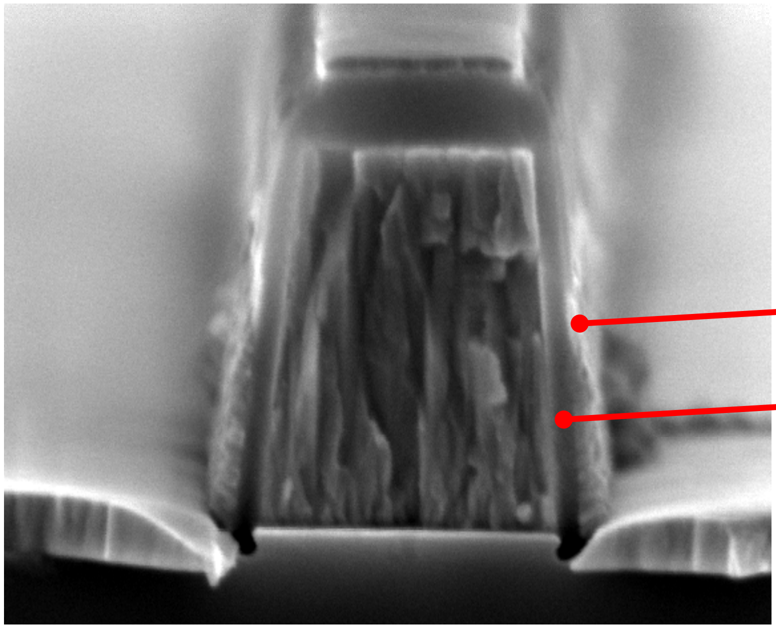
Refractory, non-diffusive metal contacts for thin base semiconductor

A.. Baraskar

Sputtered Process for in-situ base contacts

- Blanket ex-situ *Pd/W* contacts
- Planarization and etch back
- Low contact resistivity
- Lift-off free and Au free base process
- Self-aligned process for thin emitters
- Enables *refractory, in-situ* base contacts



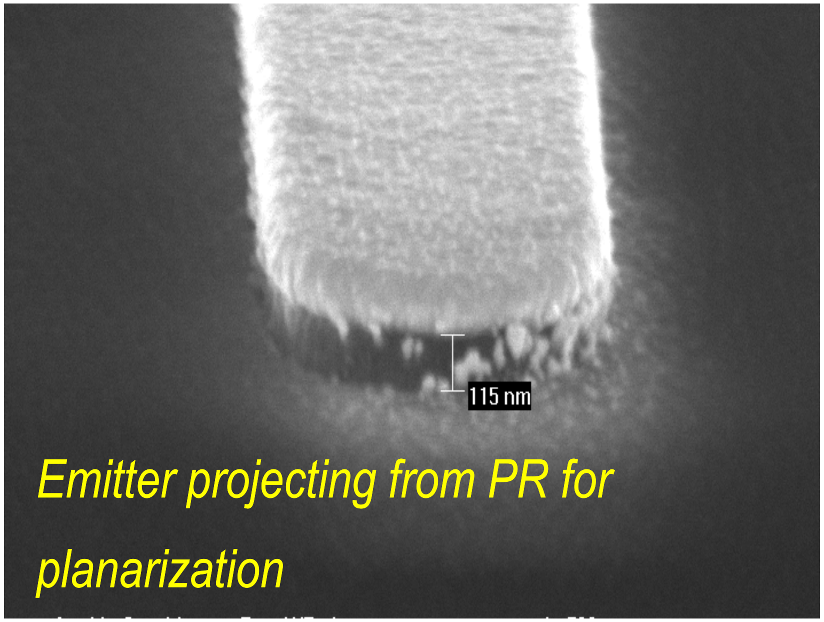


Planarization boundary

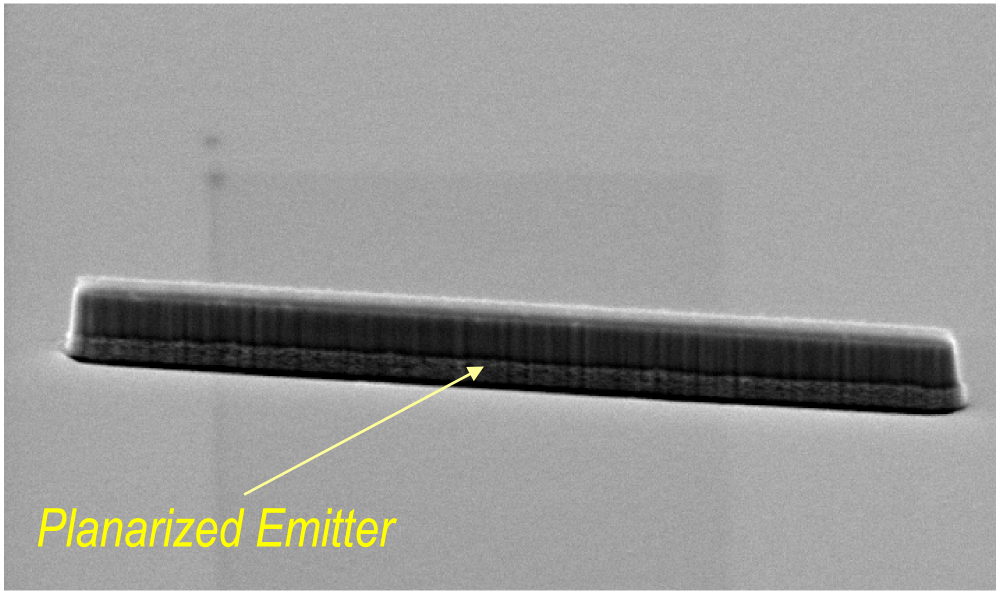
SiN$_x$ Sidewall

V. Jain
E. Lobisser

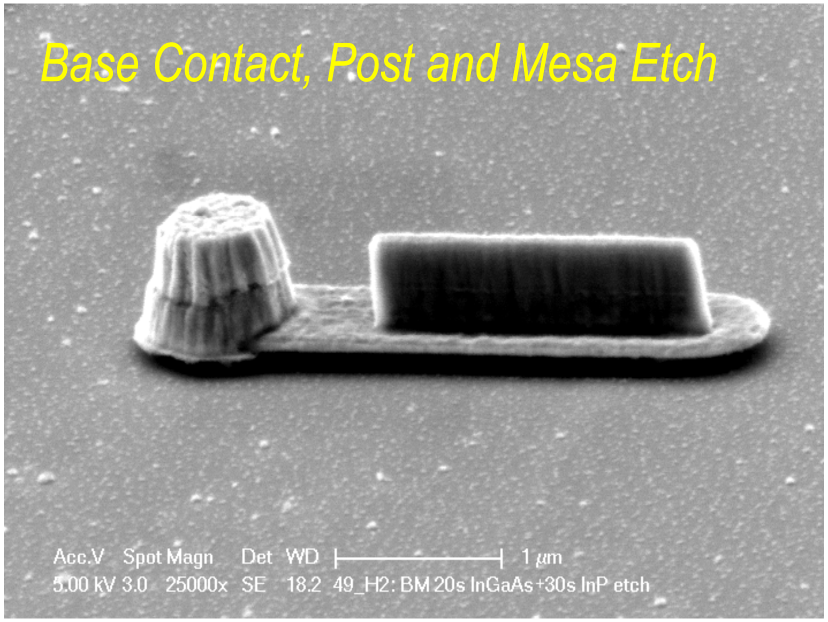
Sub-100 nm HBTs : planarized base contact



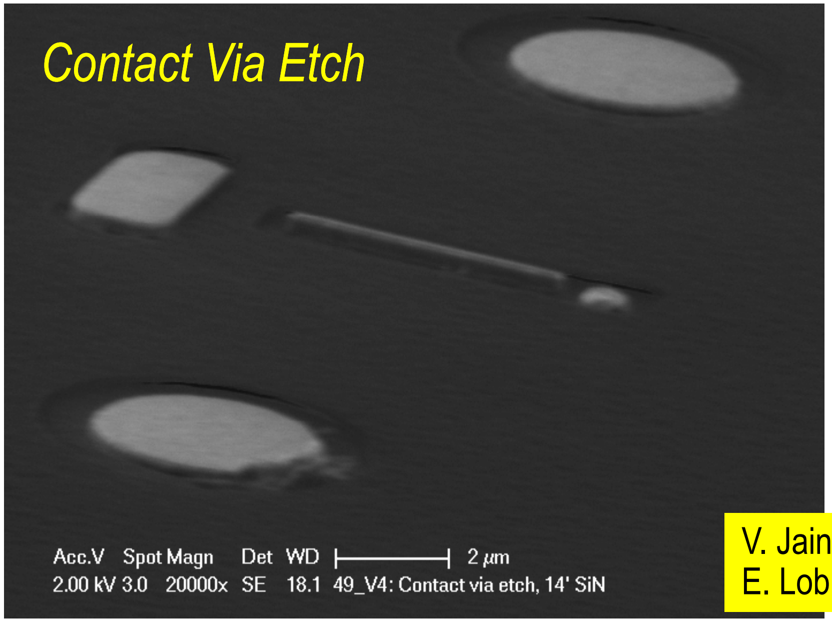
Emitter projecting from PR for planarization



Planarized Emitter



Base Contact, Post and Mesa Etch

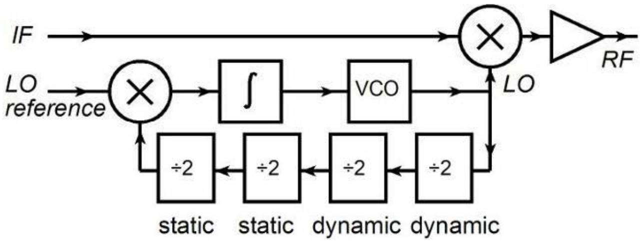


Contact Via Etch

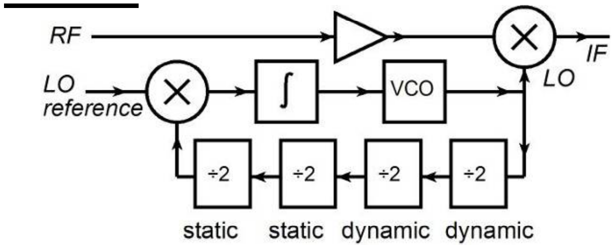
V. Jain
E. Lobisser

670 GHz Transceiver Simulations in 128 nm InP HBT

transmitter exciter



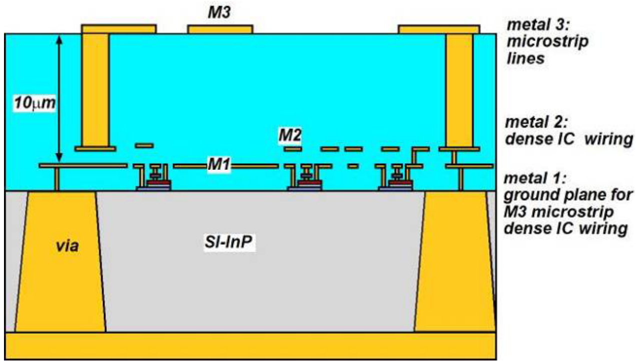
receiver



3-layer thin-film THz interconnects

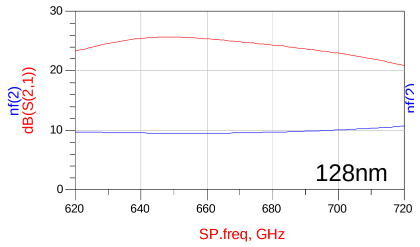
thick-substrate--> high-Q TMIC

thin -> high-density digital

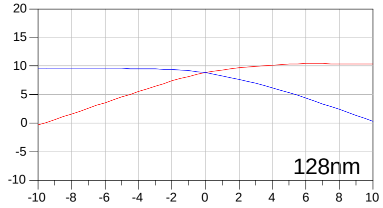


Simulations @ 670 GHz (128 nm HBT)

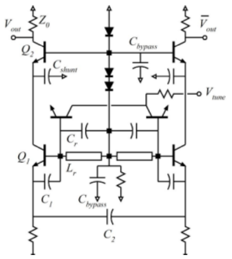
LNA: 9.5 dB Fmin at 670 GHz

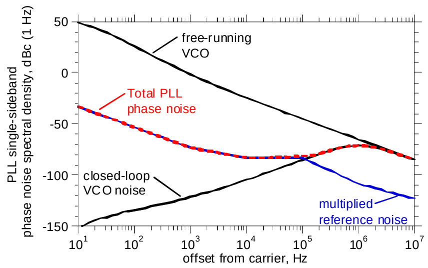


PA: 9.1 dBm Pout at 670 GHz

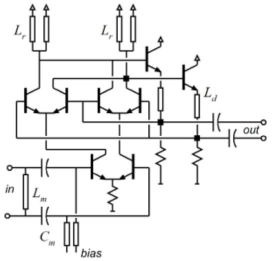


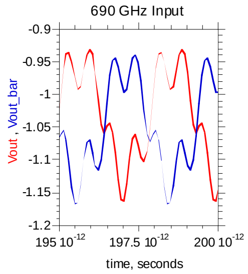
VCO:
-50 dBc (1 Hz)
@ 100 Hz offset
at 620 GHz (phase 1)

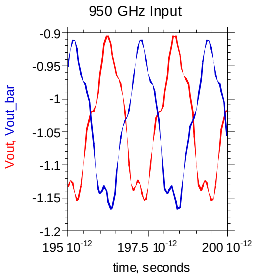




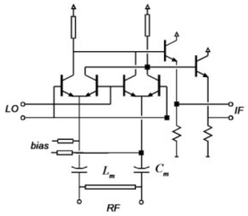
Dynamic divider:
novel design,
simulates to 950 GHz

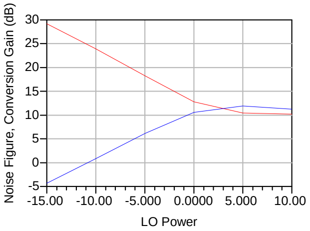






Mixer:
10.4 dB noise figure
11.9 dB gain



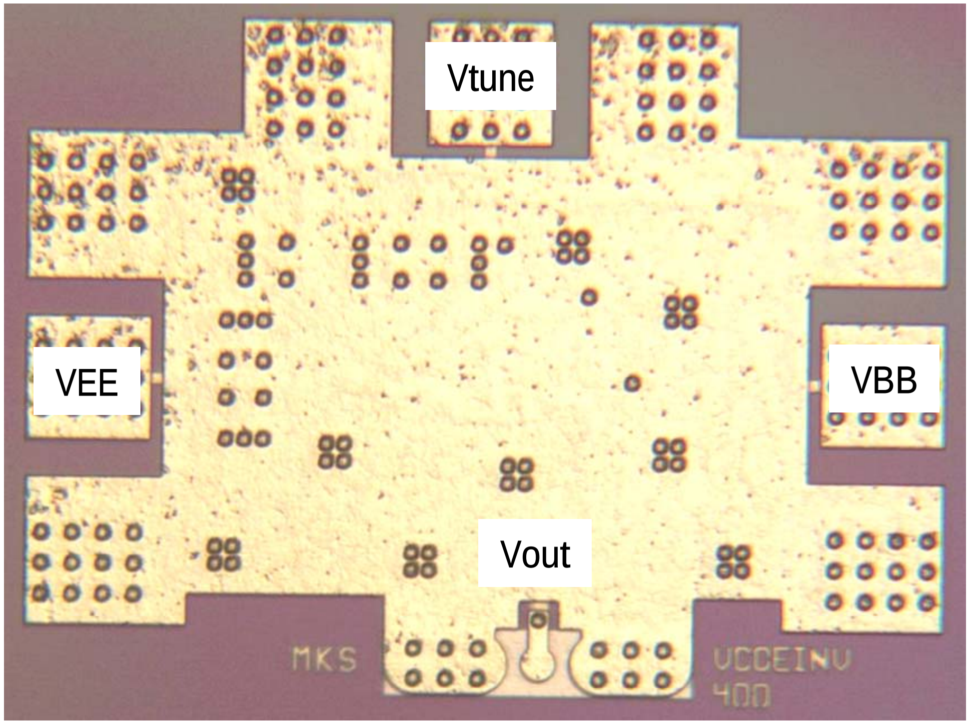


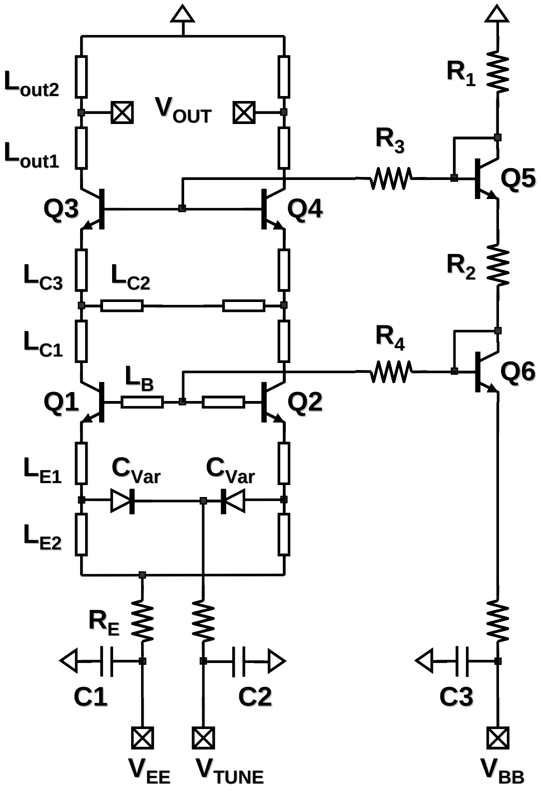
InP HBT Fundamental Oscillators to > 340 GHz

M. Seo UCSB
M. Rodwell UCSB
M. Urteaga TSC
TSC HBT Technology

Differential Topology, Cascode output buffer, ECL outputs

Fixed frequency and voltage controlled designs





InP HBT 331 GHz Dynamic Frequency Dividers

M. Seo UCSB
M. Rodwell UCSB
M. Urteaga TSC
Z. Griffith TSC
TSC HBT Technology

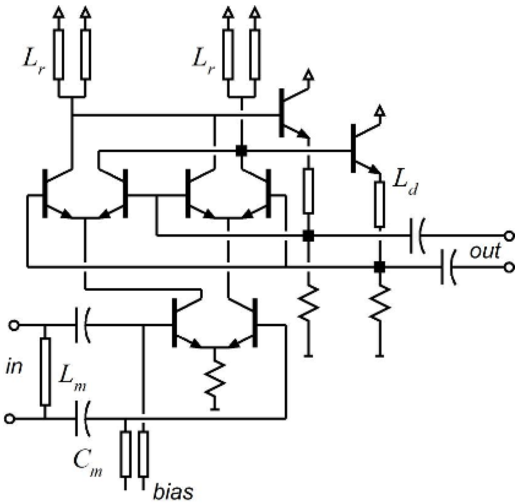
Topology: Double-balanced mixer with emitter follower feedback and resonant loading

Modified version of modern dynamic divider (H.M. Rein)

Inverted microstrip wiring

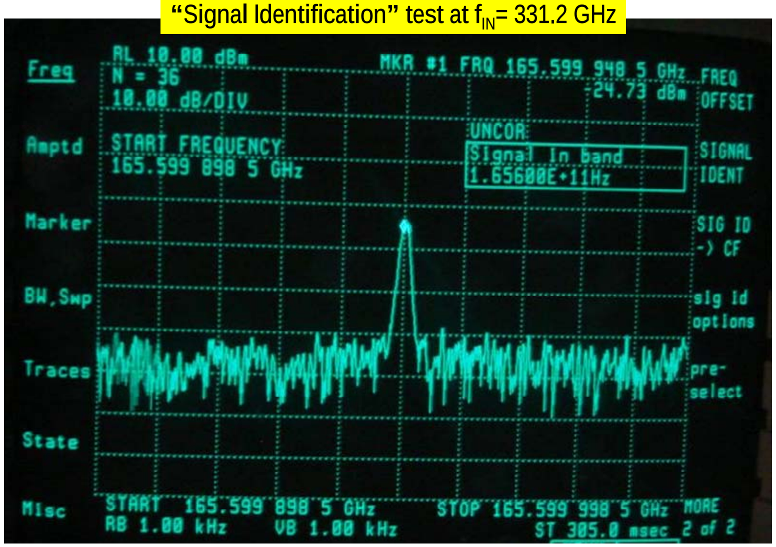
Design variations with input for external clock source and with integrated fixed frequency and voltage controlled oscillators for testing.

Circuit Schematic

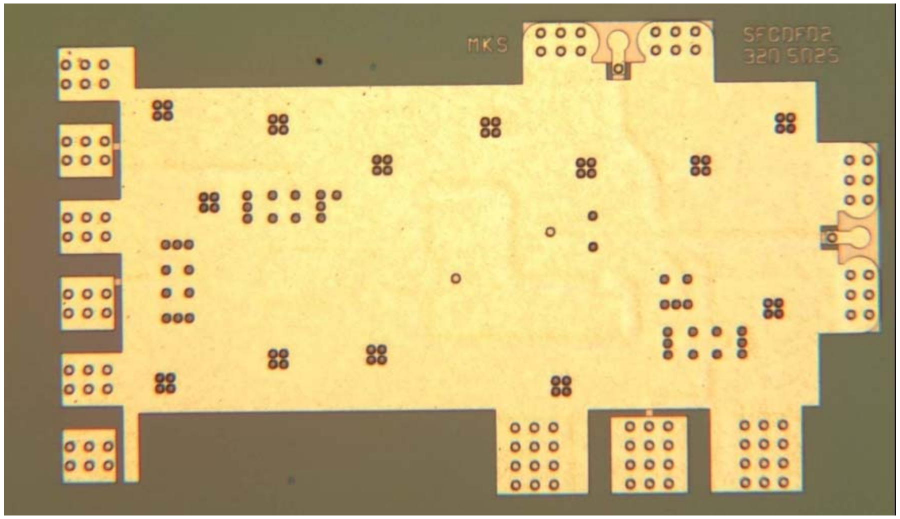


Output spectrum with 331.2 GHz clock input

“Signal Identification” test at f_{IN}= 331.2 GHz



Chip photograph

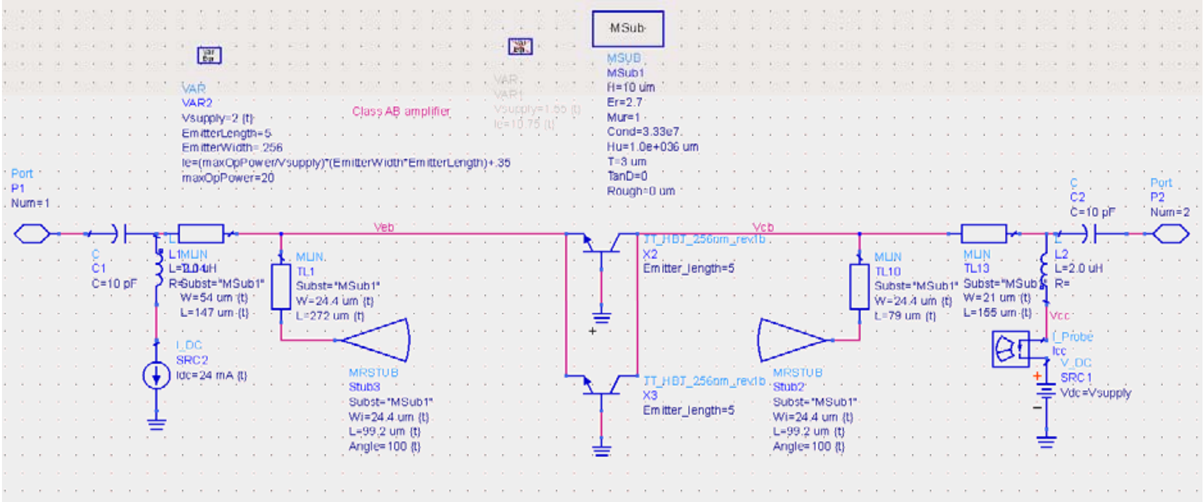


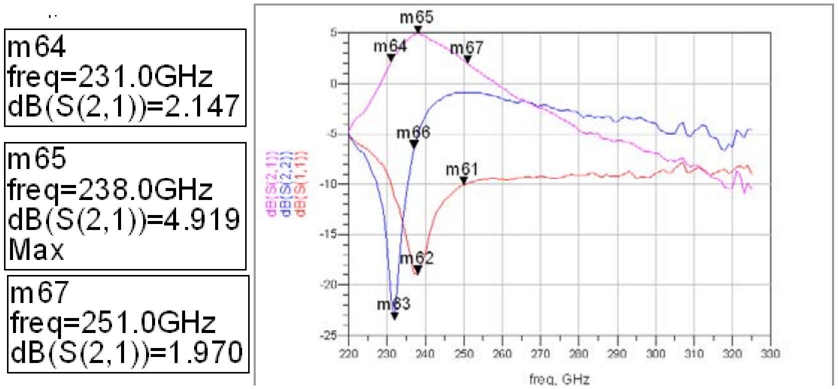
THz 240 GHz PA Design

T. Reed UCSB
M. Urteaga TSC
Z. Griffith TSC
TSC HBT Technology

Teledyne InP HBTs We=256nm, Tc=150nm

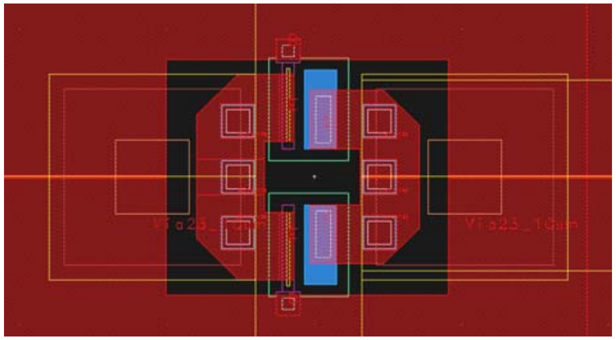
Two-finger design achieves S21 = 4.9dB @ 238GHz

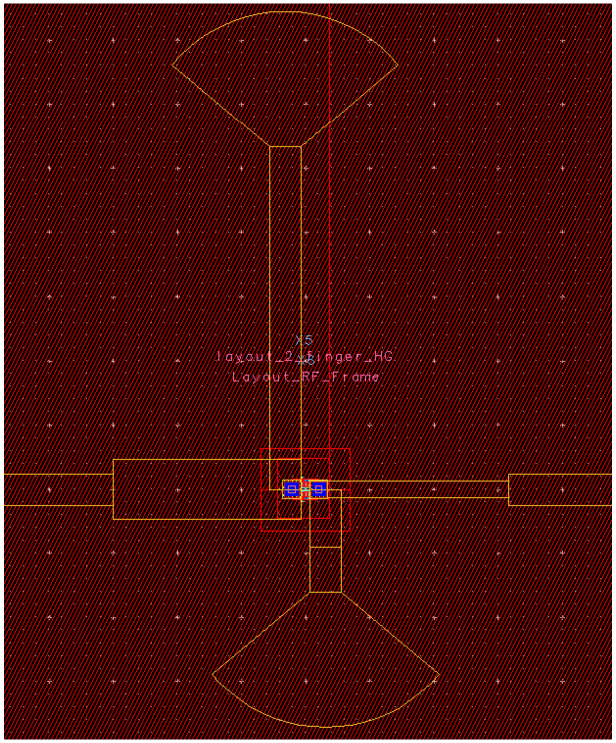



m64
freq=231.0GHz
dB(S(2,1))=2.147

m65
freq=238.0GHz
dB(S(2,1))=4.919
Max

m67
freq=251.0GHz
dB(S(2,1))=1.970





THz Transistors

THz Integrated Circuits

Device scaling (Moore's Law) is not yet over.

Scaling→ multi-THz transistors.

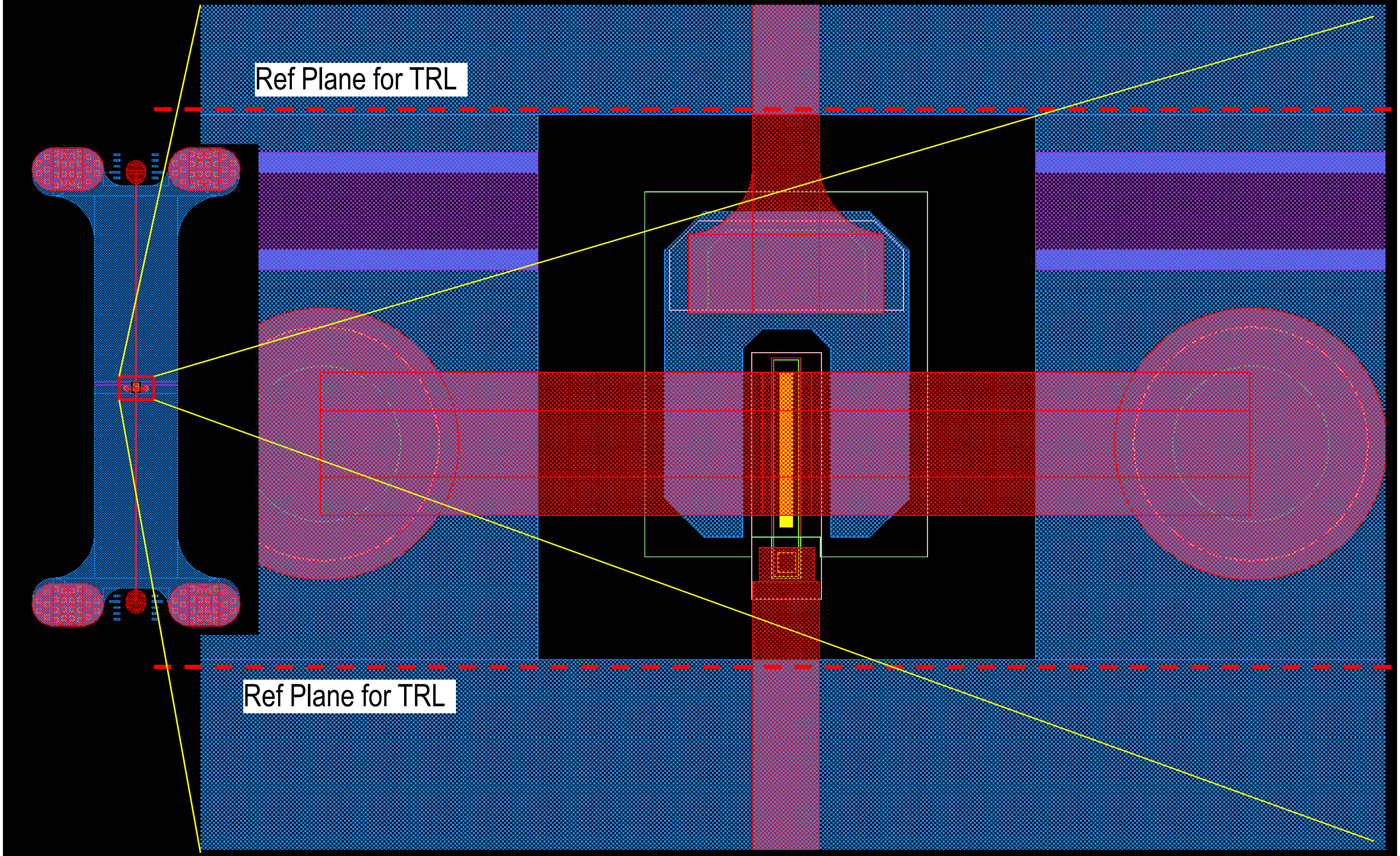
Challenges in scaling:
contacts, dielectrics, heat

Multi-THz transistors:
for systems at very high frequencies
for better performance at moderate frequencies

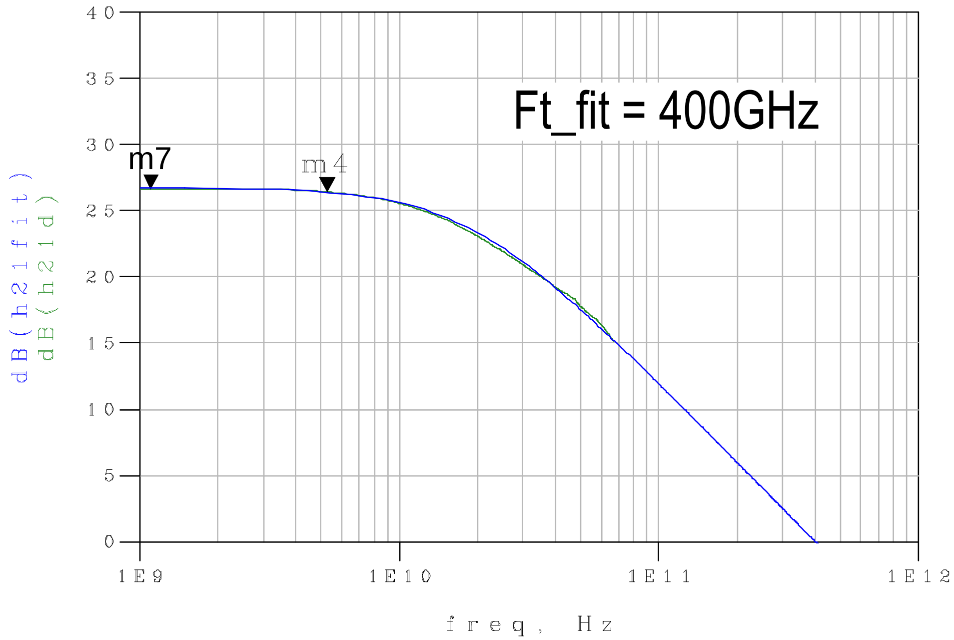
Vast #s of THz transistors
complex systems
new applications.... imaging, radio, and more

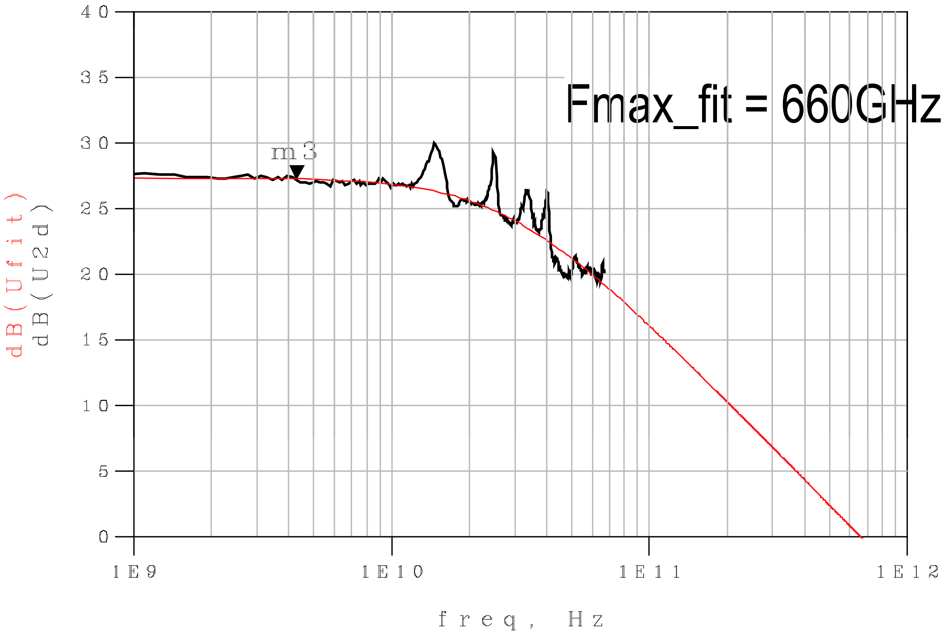
end

On-Wafer TRL Calibration Envirnoment

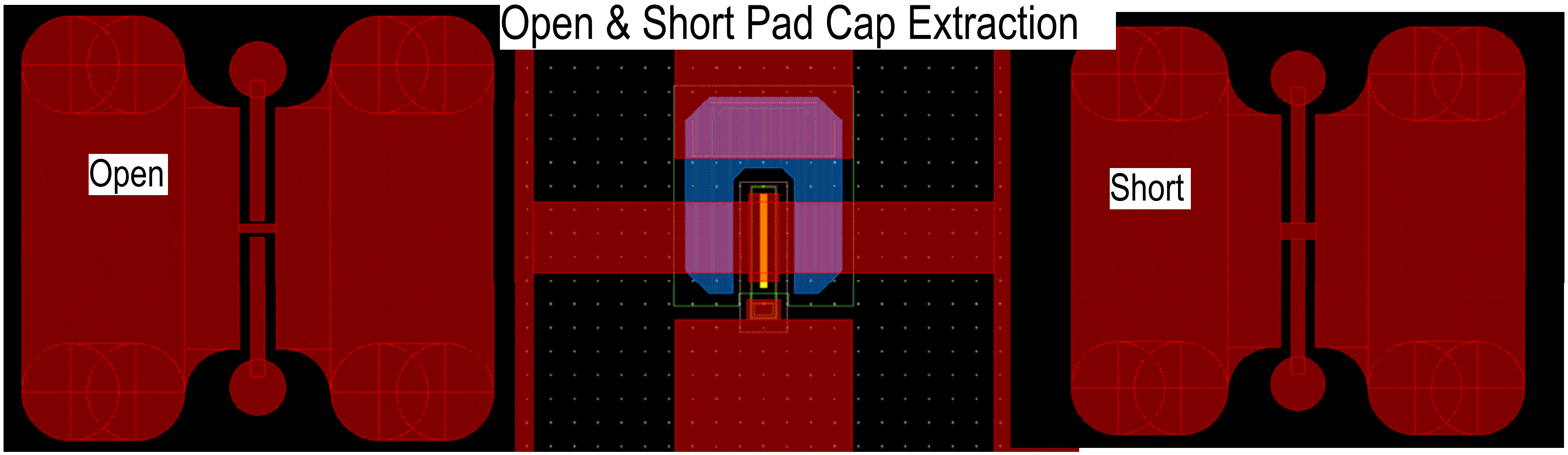


0.5-67GHz Data: Lumped Pads, Off Wafer LRRM Cal.





Standard Off Wafer OSLT

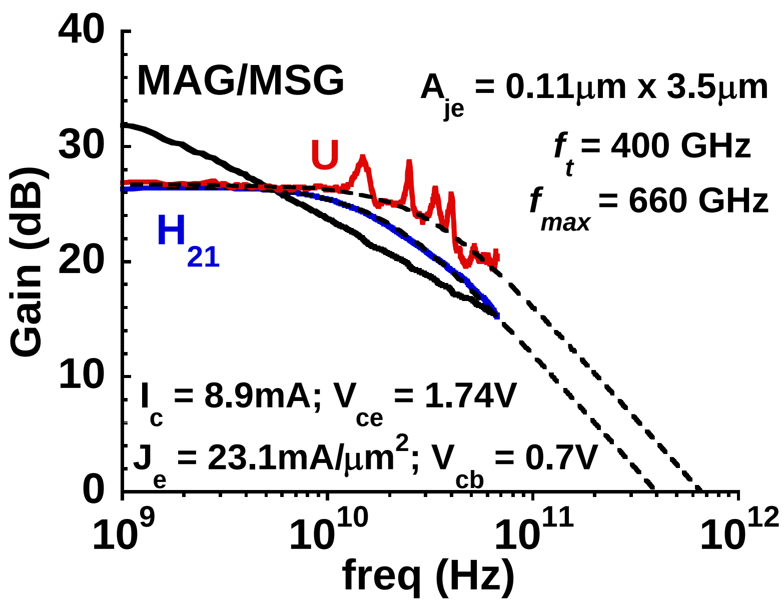


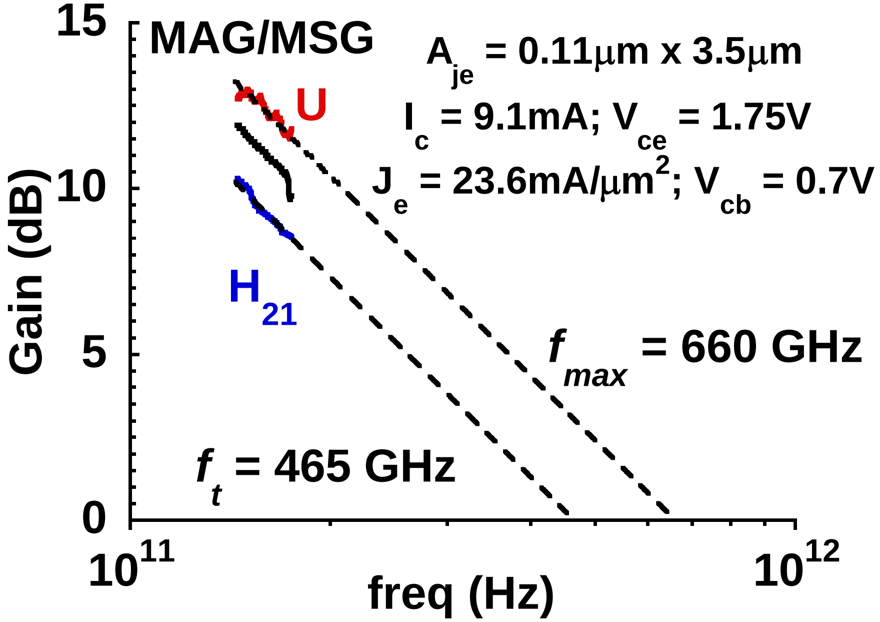
Open & Short Pad Cap Extraction

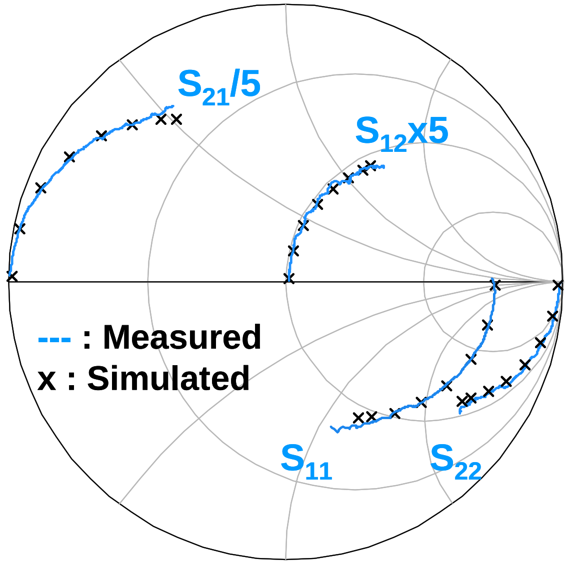
THz
Bipolar Transistors

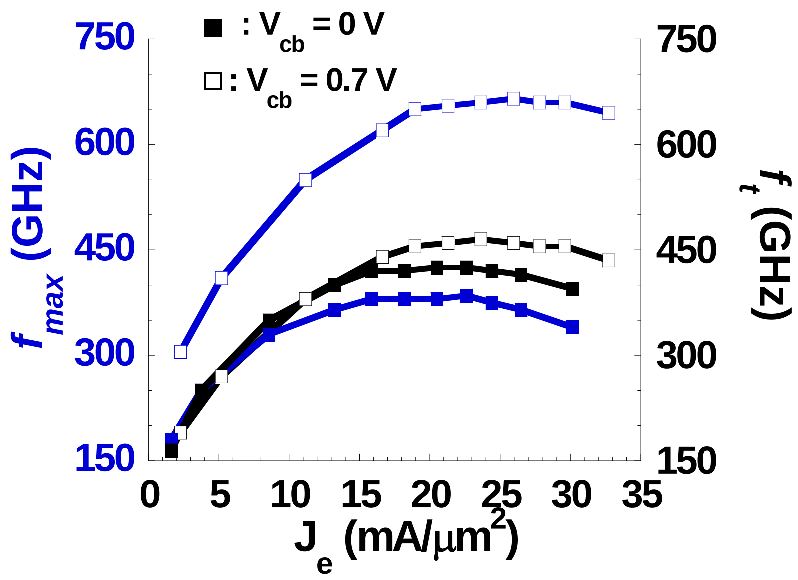
Sub-100 nm devices: lifted-off base metal

V. Jain
E. Lobisser



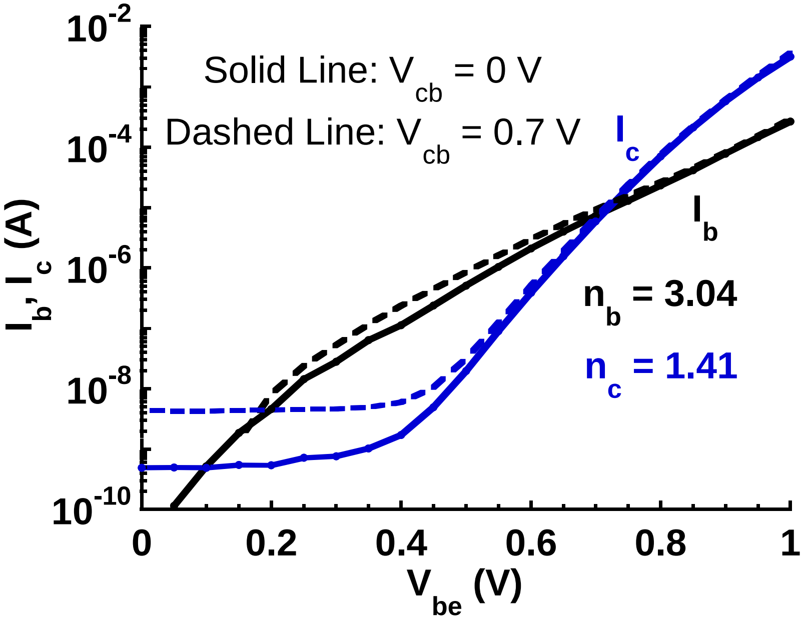


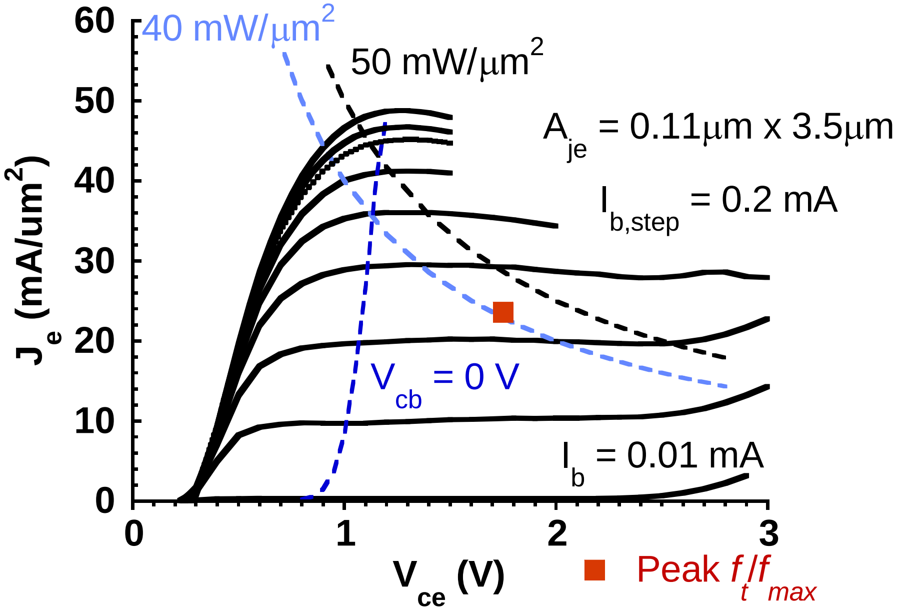


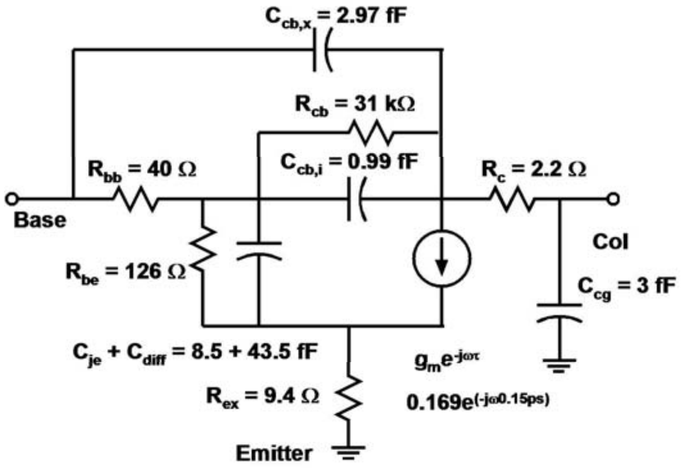


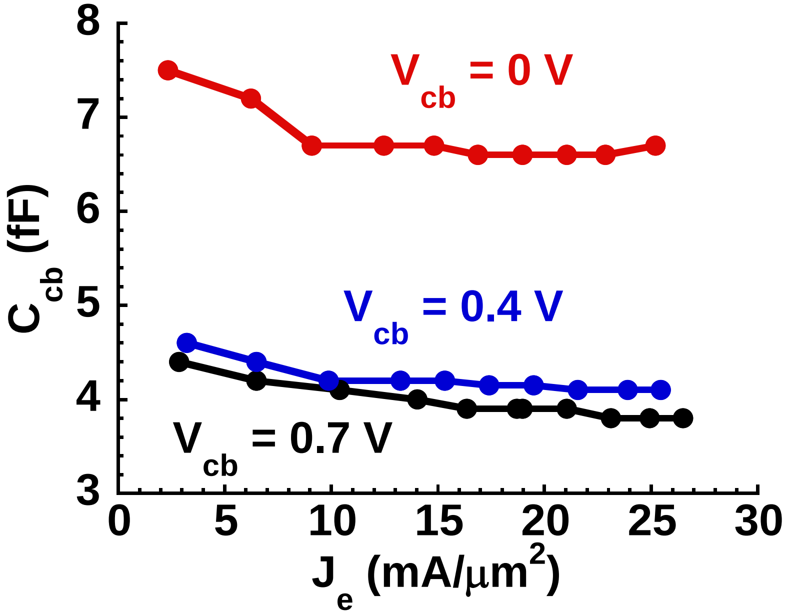
Sub-100 nm devices: lifted-off base metal

V. Jain
E. Lobisser

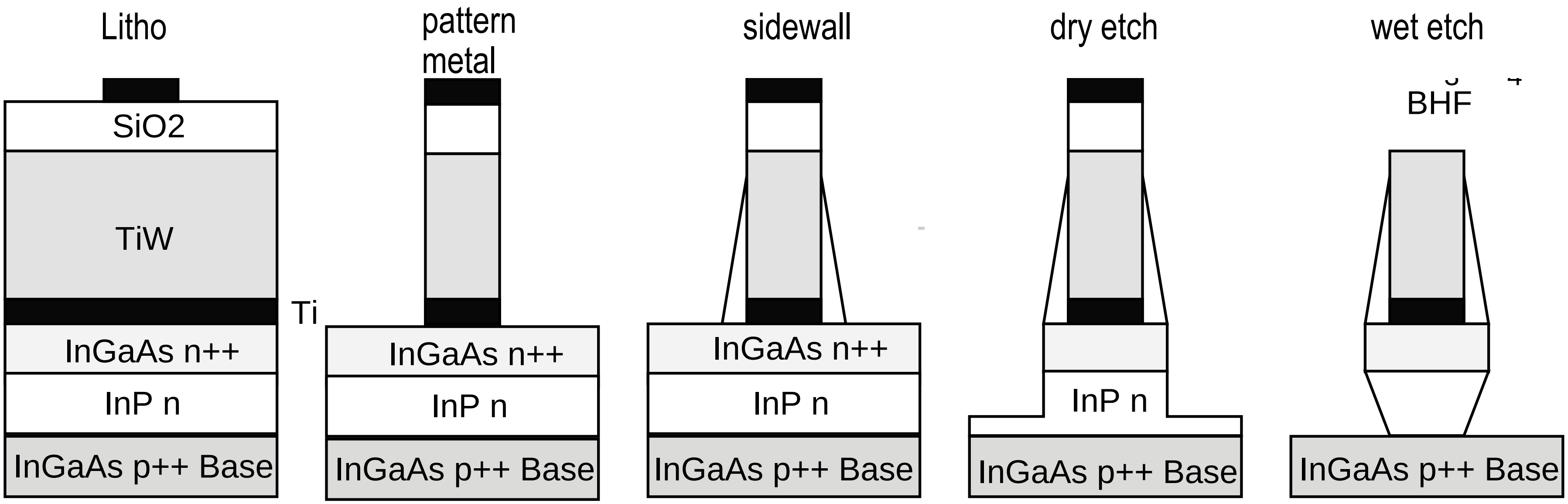


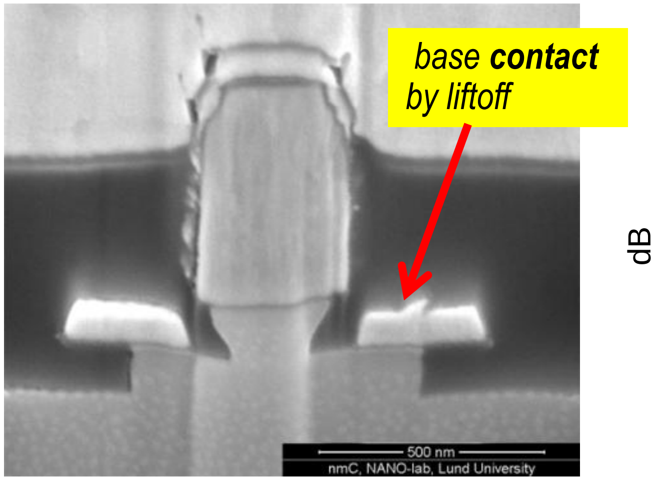


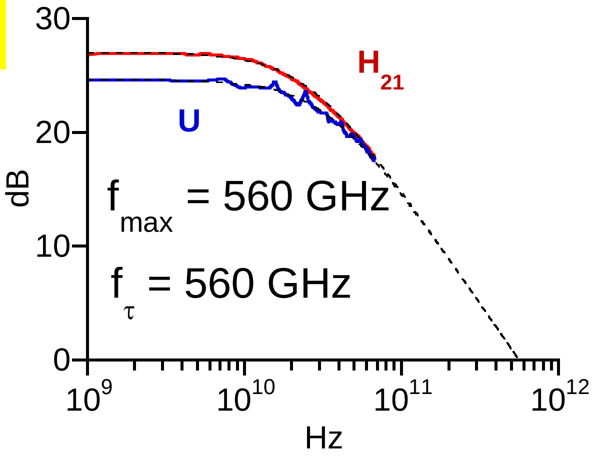




2008 UCSB Dry-Etched Ti/TiW Emitter Process




*base **contact** by liftoff*



Worked well @ 200 nm

Low yield @ 128 nm: stress⟶ poor adhesion

Substantial revision required