

# THz Transistors: Design and Process Technologies

Mark J.W. Rodwell<sup>a</sup>, Vibhor Jain<sup>a</sup>, Evan Lobisser<sup>a</sup>, Ashish Baraskar<sup>a</sup>, Mark A. Wistey<sup>a,b</sup>, Uttam Singiseti<sup>a</sup>, Greg J. Burek<sup>a</sup>, Brian J. Thibeault<sup>a</sup>, Arthur C. Gossard<sup>a</sup>, Eun Ji Kim<sup>c</sup>, Paul C. McIntyre<sup>c</sup>, Bo Yu<sup>e</sup>, Peter Asbeck<sup>e</sup>, Yuan Taur<sup>e</sup>

<sup>a</sup>Departments of ECE and Materials, University of California, Santa Barbara

<sup>b</sup>Now at the University of Notre Dame

<sup>c</sup>Materials Science and Engineering Department, Stanford University,

<sup>d</sup>Intel Corporation

<sup>e</sup>Departments of ECE and Materials, University of California, San Diego

**Abstract:** To obtain THz bandwidths in either bipolar or field-effect transistors, lithographic junction dimensions and epitaxial layer thicknesses must be reduced, device contact resistivities reduced, gate capacitance densities increased, and operating current densities increased. Fabrication process flows must be extensively revised to fabricate devices having 10-50 nm junction dimensions and 1-3 THz cutoff frequencies...

**Keywords:** Heterojunction bipolar transistors, MOSFETs, THz electronics.

## Introduction

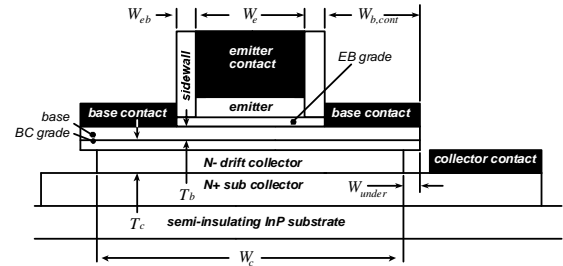
III-V transistors of ~10 to 100 nm lithographic dimensions are being developed both for THz applications and for use in large-scale digital integrated circuits. Reducing dimensions increases both IC packing density and transistor bandwidth. Increasing bandwidth of an arbitrary circuit by  $\gamma:1$  requires a  $\gamma:1$  reduction of transistor capacitances and transit delays while maintaining constant resistances and bias and signal voltages and currents.

For bipolar transistors [1], this requires a  $\sim\gamma^1:1$  reduction in epitaxial dimensions, a  $\gamma^2:1$  reduction in contact resistivities, and a  $\gamma^2:1$  reduction in lithographic dimensions. For field-effect transistors [2], such scaling requires again a  $\gamma:1$  reduction in epitaxial dimensions (dielectric equivalent thickness, wavefunction depth) and a  $\gamma^2:1$  reduction in contact resistivities, but only requires a  $\gamma^1:1$  reduction in lithographic dimensions (gate length). Required current densities scale with both transistor types; for HBTs, emitter current density ( $\text{mA}/\mu\text{m}^2$ ) varies as  $\gamma^2$ , though current per unit emitter stripe length remains fixed, while for FETs, current per unit gate width ( $\text{mA}/\mu\text{m}$ ) varies as  $\gamma^1$ , but current per unit source and drain Ohmic contact area ( $\text{mA}/\mu\text{m}^2$ ) varies as  $\gamma^2$ .

To build multi-THz HBTs and HEMTs, and to build sub-22-nm InGaAs MOSFETs, we must fabricate *self-aligned* contacts and junctions of 10-100 nm dimensions. We must develop Ohmic contacts of  $\sim 1\ \Omega - \mu\text{m}^2$  contact resistivity; this resistivity must not increase when operating  $\sim 25\text{-}250\ \text{mA}/\mu\text{m}^2$  current density, nor can the contact metals diffuse under such high current and thermal stress through device junctions only  $\sim 5\text{-}10\ \text{nm}$  below the surface. We here describe our efforts to

Table 1: HBT scaling laws: changes required for  $\gamma:1$  increased bandwidth in an arbitrary circuit

parameter	law
emitter junction length, $L_e$ (nm)	$\gamma^0$
emitter junction width, $W_e$ (nm)	$\gamma^{-2}$
collector junction width (nm)	$\gamma^{-2}$
collector depletion thickness (nm)	$\gamma^{-1}$
base thickness (nm)	$\sim \gamma^{-1/2}$
contact resistivities $\rho_c$ ( $\Omega - \mu\text{m}^2$ )	$\gamma^{-2}$
emitter current density ( $\text{mA}/\mu\text{m}^2$ )	$\gamma^2$
emitter current density ( $\text{mA}/\mu\text{m}$ )	$\gamma^0$
temperature rise (one device, K)	$\sim \ln(L_e/W_e)$



develop such fabrication processes for both InP-based FETs and HBTs.

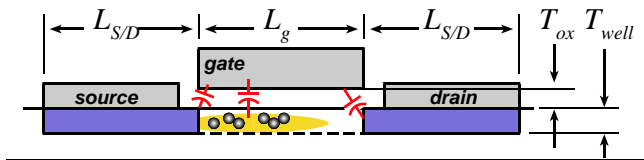
## THz and nm FET Scaling

First consider in more detail FET scaling in the constant-voltage, constant-velocity limit. Vertical dimensions ( $T_{well}$ ,  $T_{eq}$ ) must be reduced in proportion to gate length to maintain a constant  $g_m/G_{ds}$  ratio and to maintain a constant ratio of the parallel-plate ( $C_{g-ch}$ ) to the fringing ( $C_{gs,f}$ ,  $C_{gd}$ ) components of the device input capacitance; in the absence of vertical scaling, drain-induced barrier lowering increases, output conductance degrades, and the input capacitance becomes dominated by gate fringing fields.

As a consequence of vertical scaling, on-state current density  $I_d/W_g$  increases as  $\gamma^1$ . It is well understood that difficulties in reducing  $T_{eq}$  (gate leakage by tunneling) and in increasing  $C_{DOS}$  [3] will impede constant-voltage FET

Table 2: Constant-voltage / constant-velocity FET scaling laws: changes required for  $\gamma : 1$  increased bandwidth in an arbitrary circuit

parameter	law
gate length $L_g$ , source-drain contact lengths $L_{S/D}$ (nm)	$\gamma^{-1}$
gate width $W_g$ (nm)	$\gamma^{-1}$
equivalent oxide thickness $T_{eq} = T_{ox} \epsilon_{SiO_2} / \epsilon_{oxide}$ (nm)	$\gamma^{-1}$
dielectric capacitance $C_{ox} = \epsilon_{SiO_2} L_g W_g / T_{eq}$ (fF)	$\gamma^{-1}$
inversion thickness $T_{inv} \sim T_{well} / 2$ (nm)	$\gamma^{-1}$
semiconductor capacitance $C_{semi} = \epsilon_{semi} L_g W_g / T_{inv}$ (fF)	$\gamma^{-1}$
DOS capacitance $C_{DOS} = q^2 n m^* L_g W_g / 2\pi\hbar^2$ (fF)	$\gamma^{-1}$
electron density $n_s$ ( $\text{cm}^{-2}$ )	$\gamma^1$
gate-channel capacitance $C_{g-ch} = [1/C_{ox} + 1/C_{semi} + 1/C_{DOS}]^{-1}$ (fF)	$\gamma^{-1}$
transconductance $g_m \sim C_{g-ch} v_{injection} / L_g$ (mS)	$\gamma^0$
gate-source, gate-drain fringing capacitances $C_{gs,f} \propto \epsilon W_g$ , $C_{gd} \propto \epsilon W_g$ (fF)	$\gamma^{-1}$
S/D access resistances $R_s, R_d$ ( $\Omega$ )	$\gamma^0$
S/D contact resistivity $R_s / W_g, R_d / W_g$ ( $\Omega - \mu\text{m}$ )	$\gamma^{-1}$
S/D contact resistivity $\rho_c$ ( $\Omega - \mu\text{m}^2$ )	$\gamma^{-2}$
drain current $I_d \sim g_m (V_{gs} - V_{th})$ (mA)	$\gamma^0$
drain current density (mA/ $\mu\text{m}$ )	$\gamma^1$
temperature rise (one device, K)	$\sim W_g^{-1}$



scaling; note also that  $T_{inv}$  must scale as  $\gamma^{-1}$ , requiring thinner wells or stronger vertical fields,  $(R_s + R_d) / W_g$  must scale as  $\gamma^{-1}$ , requiring both lower  $\rho_c$  and increased carrier concentrations in access regions, and on-state inversion charge density  $n_s$  must scale as  $\gamma^1$ , requiring increased gate barrier height. Further, device self-heating scales as  $\gamma^1$ , a serious concern for normally-on circuits such as sub-mm-wave amplifiers.

These scaling considerations apply to equally to InGaAs FETs in development for VLSI and for sub-mm-wave/THz applications; device design goals include low access resistance, high drive current density, thin wells, high sheet carrier density, and gate barriers that are both

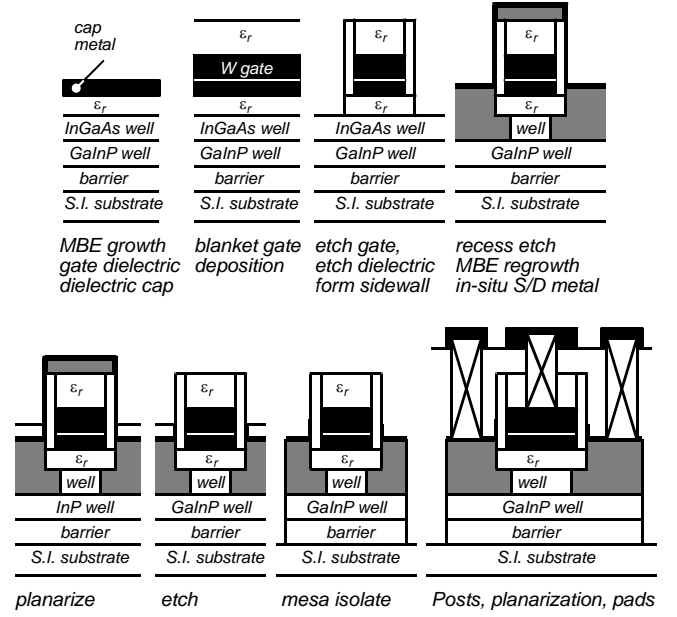


Figure 1: Process flow for III-V FETs with source/drain regrowth by MEE.

thin and high in energy. Future sub-mm-wave FETs may well use high-K gate dielectrics to permit small  $T_{eq}$  and large  $n_s$ ; note that moderately high interface charge density  $D_{it}$  will not impair device gain at frequencies well above the inverse of the interface trap lifetimes.

### III. Fabrication Processes For nm III-V MOSFETs

Established III-V HEMT structures do not well address these scaling requirements. We have therefore developed a fully self-aligned InGaAs MOSFET process flow [4,5,6,7] (fig. 1). In this flow, 4.7 nm  $\text{Al}_2\text{O}_3$  gate dielectric is deposited by ALD on a 5 nm  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  channel, the gate is formed by blanket  $W/\text{Cr}/\text{SiO}_2$  deposition and RIE etching, and thin  $\sim 25$  nm  $\text{Si}_3\text{N}_4$  gate sidewalls formed. After etching the  $\text{Al}_2\text{O}_3$ , self-aligned S/D InAs N+ regions (50 nm thick,  $8 \times 10^{19} \text{cm}^{-3}$ , 23  $\Omega$  sheet resistance) are formed by migration enhanced epitaxy, and self-aligned S/D contacts formed by in-situ blanket evaporation of Mo (3.5  $\Omega - \mu\text{m}^2$  contact resistance) and a subsequent height-selective etch [8]. Mesa isolation and back-end metal completes the process. Unlike HEMTs, no gate barrier is present in the S/D regions, the source and drain are fully self-aligned to the gate, and carrier densities in the S/D access regions are high ( $\sim 1.5 \times 10^{13} \text{cm}^{-2}$ ). Figure 3 shows measured  $I_D$  for a 200-nm- $L_g$  device.



Figure 3: Cross-section of regrown S/D InGaAs FET with a 27 nm gate.

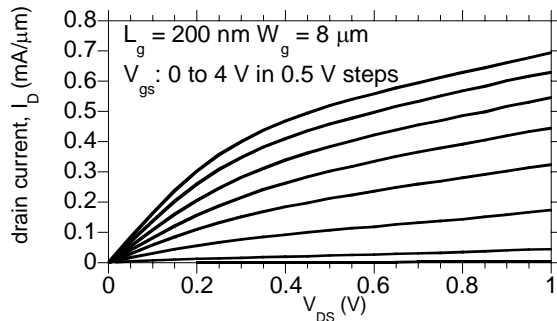


Figure 4: Common-source characteristics of 200 nm device

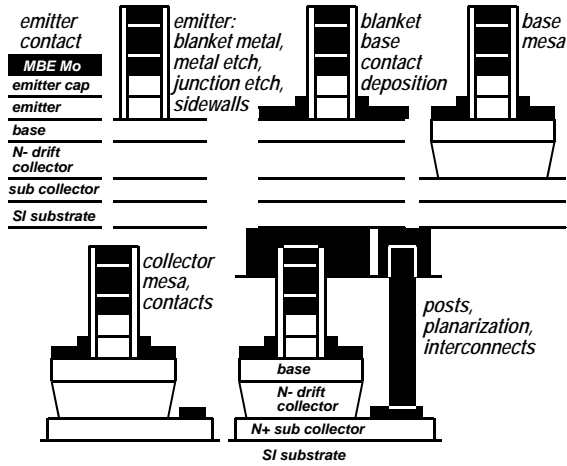


Figure 5: Refractory-contact /dry-etched process flow for 128 nm /64 nm InP HBTs

### THz Bipolar Transistor Scaling

We now review bipolar transistor scaling. Unlike FETs, the diffusion capacitances and the parallel-plate component of junction depletion capacitances dominate over edge (fringing) capacitances, hence HBTs need not be scaled to progressively increase the device operating

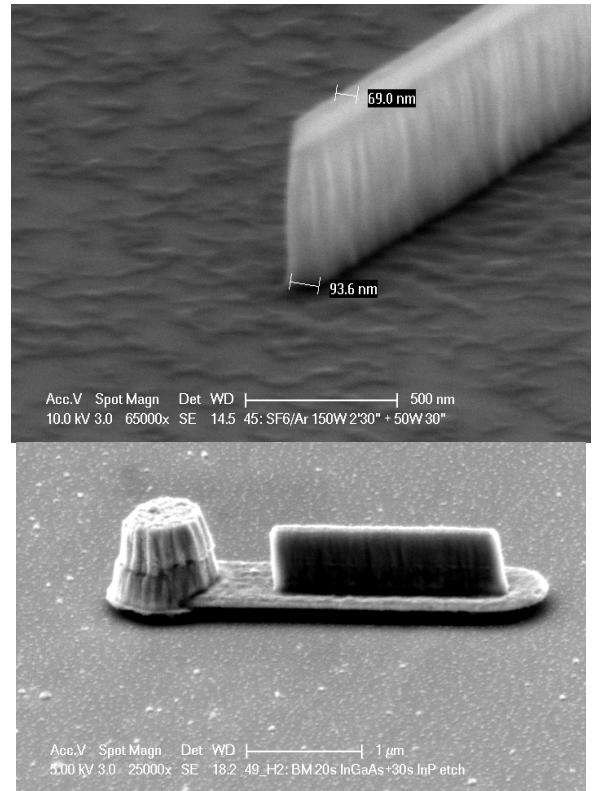


Figure 2: Images of sub-100-nm HBTs with refractory W emitter and base contacts. Top: 94 nm emitter contact. Bottom: HBT after emitter and base definition

current and transconductance per unit junction length. Unlike MOSFETs (but like THz HEMTs), the HBT is biased normally-on, and the device operating power density and the consequent junction temperature rise is a dominant consideration controlling the geometric scaling laws [9]. As noted above, each  $\gamma$ :1 increase in bandwidth requires a  $\sim \gamma^1$ :1 reduction in epitaxial dimensions, a  $\gamma^2$ :1 reduction in contact resistivities, and a  $\gamma^2$ :1 reduction in lithographic dimensions. These scaling laws arise simply because the collector thickness must be reduced  $\gamma^1$ :1 to reduce collector transit time, and the collector area reduced  $\gamma^2$ :1 to obtain the desired  $\gamma^1$ :1 reduction in collector capacitance. With all junction areas reduced  $\gamma^2$ :1, contact resistivities must be reduced in the same proportion to maintain constant access resistance, and current densities increased in the same proportion to maintain constant operating current. Because junction temperature rise varies as  $\Delta T \propto (P/K_{thermal}) \cdot \ln(L_e/W_e)$ , the required  $\gamma^2$ :1 reduction in junction area *cannot* be obtained by reducing the device junction length; instead, the emitter (and collector) junction widths are both reduced  $\gamma^2$ :1. The scaling laws of table 1 are thereby obtained.

### V. Fabrication Processes For nm III-V HBTs

For HBTs, a 1.0 THz  $f_r$  and 2.0 THz  $f_{max}$  should be obtained with  $\sim 64$  nm contact width and  $\sim 2$

$\Omega - \mu\text{m}^2$  resistivity for both the emitter and base contacts. The emitter current density must be  $\sim 30\text{-}40 \text{ mA}/\mu\text{m}^2$ , and the base must be  $\sim 20 \text{ nm}$  thick.

There are serious challenges in building such a device. It is difficult to form tall yet narrow emitter contacts by liftoff, and target emitter current densities are close to the electromigration limits of a gold emitter electrode. We are therefore forming the emitter contact by blanket sputter deposition and subsequent dry-etching of a refractory (W or Mo) metal. To control the emitter etc undercut during emitter junction definition, the emitter semiconductor must either be very thin, or the emitter must be dry-etched. Base-emitter contact separation by liftoff is not straightforward at these junction dimensions. Figure 4 shows a simplified version of our present 128nm/64 nm process flow. n-situ Mo emitter contacts [10] provide  $1.1 \pm 0.4 \Omega - \mu\text{m}^2$  contact resistivity. The emitter metal is dry-etched Mo or W to withstand high target current densities. Emitter and base contacts are separated by thin  $\text{Si}_x\text{N}_y$  sidewalls, and base contacts are sputter-deposited refractory metals.

## References

- [1] Mark Rodwell, Minh Le, Berinder Brar, "InP Bipolar ICs: Scaling Roadmaps, Frequency Limits, Manufacturable Technologies" IEEE Proceedings, Volume 96, Issue 2, Feb. 2008 Page(s):271 - 286
- [2] M.A. Wistey, U. Singiseti, G. Burek, A. Baraskar, V. Jain, B. Thibault, A. Nelson, E. Arkun, C. Palmstrøm, J. Cagnon, S. Stemmer, A. Gossard, M. Rodwell, P. McIntyre, B. Shin, E. Kim, S. Bank, Y.-J. Lee, "III-V/Ge Channel Engineering for Future CMOS", *Proceedings*, Electrochemical Society Annual Meeting, May 2009.
- [3] P. M. Solomon, S. E. Laux, 2001 IEEE IEDM
- [4] U. Singiseti, M.A. Wistey, G.J. Burek, E. Arkun, Y. Sun, E.J. Kiwera, B. J. Thibeault, A.C. Gossard, C. Palmstrøm, and M.J.W. Rodwell, "InGaAs channel MOSFET with novel self-aligned source/drain MBE regrowth technology", *Physica Status Solidi (c)*, Volume 6 Issue 6.
- [5] M. J. W. Rodwell, U. Singiseti, M. Wistey, G. Burek, A. Gossard, C. Palmstrøm, E. Arkun, P. Simmonds, S. Stemmer, R. Engel-Herbert, Y. Hwang, Y. Zheng, P. Asbeck, Y. Taur, M. V. Fischetti, B. Yu, D. Wang, Y. Yuan, C. Sachs, A. Kummel, P. McIntyre, C. Van de Walle, and J. Harris, "Technology Development & Design for 22 nm InGaAs/InP-channel MOSFETs" 2008 IEEE Indium Phosphide and Related Materials Conference, May, Versailles, France
- [6] U. Singiseti, M. A. Wistey, G. J. Burek, A. K. Baraskar, B. J. Thibeault, A. C. Gossard, M. J. W. Rodwell, B. Shin, E. J. Kim, P. C. McIntyre, B. Yu, Y. Yuan, D. Wang, Y. Taur, P. Asbeck, Y. -J. Lee, "In<sub>0.53</sub>Ga<sub>0.47</sub>As Channel MOSFETs With Self-Aligned InAs Source/Drain Formed by MEE Regrowth" . IEEE Electron Device Letters, Volume 30, Issue 1, Nov. 2009, pp. 1128-1130.
- [7] M.A. Wistey, U. Singiseti, G. Burek, A. Baraskar, V. Jain, B. Thibault, A. Nelson, E. Arkun, C. Palmstrøm, J. Cagnon, S. Stemmer, A. Gossard, M. Rodwell, P. McIntyre, B. Shin, E. Kim, S. Bank, Y.-J. Lee, "Improved Migration-Enhanced Epitaxy for Self-Aligned InGaAs Devices" Electronic Materials Conference (EMC), June 25, 2009, University Park, PA
- [8] G.J. Burek, M.A. Wistey, U. Singiseti, A. Nelson, B.J. Thibeault, S.R. Bank, M.J.W. Rodwell, A.C. Gossard, "Height-selective etching for regrowth of self-aligned contacts using MBE" *Journal of Crystal Growth*, Volume 311, Issue 7, 15 March 2009, Pages 1984-1987
- [9] Mark Rodwell, E. Lobisser, M. Wistey, V. Jain, A. Baraskar, E. Lind, J. Koo, Z. Griffith, J. Hacker, M. Urteaga, D. Mensa, Richard Pierson, B. Brar, " THz Bipolar Transistor Circuits: Technical Feasibility, Technology Development, Integrated Circuit Results", 2008 IEEE Compound Semiconductor IC symposium, October 12-14, Monterey, CA.
- [10] Ashish K. Baraskar, Mark A. Wistey, Vibhor Jain, Uttam Singiseti, Greg Burek, Brian J. Thibeault, Yong Ju Lee, Arthur C. Gossard and Mark J. W. Rodwell, "Ultra low resistance, non-alloyed ohmic contacts to n-InGaAs" *Journal of Vacuum Science and Technology B* 27, 4, Jul/Aug 2009