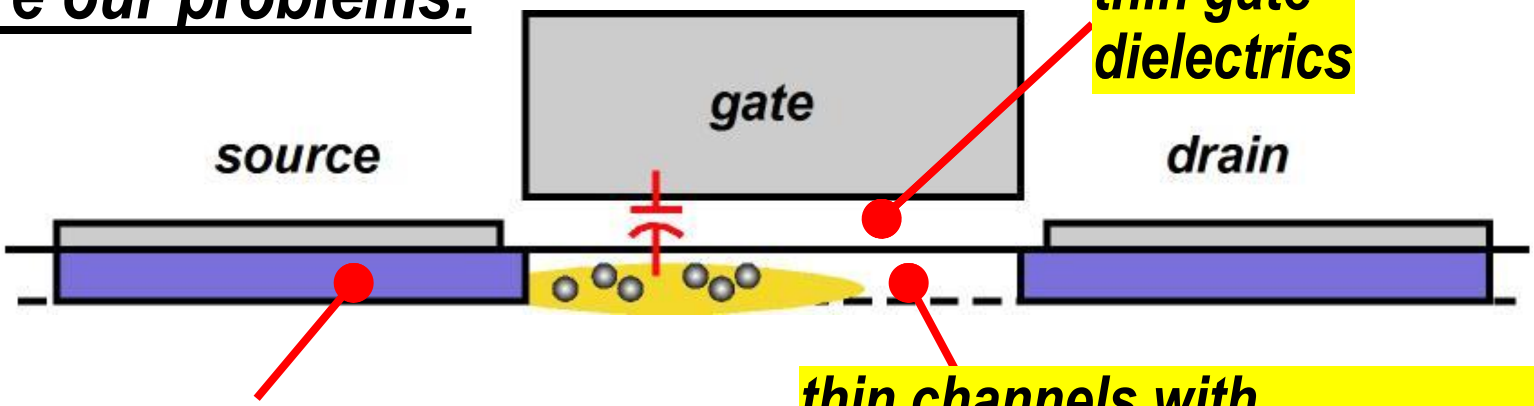
We want the best transistor we can get!

We'd like 3 THz cutoff frequencies.   We'd like 5 nm gate lengths
We'd like 3 mA/μm & a 1/2-Volt supply

Making short gates is easy----it's not the problem we face.

These are our problems:



thin gate dielectrics

low resistivity access regions:

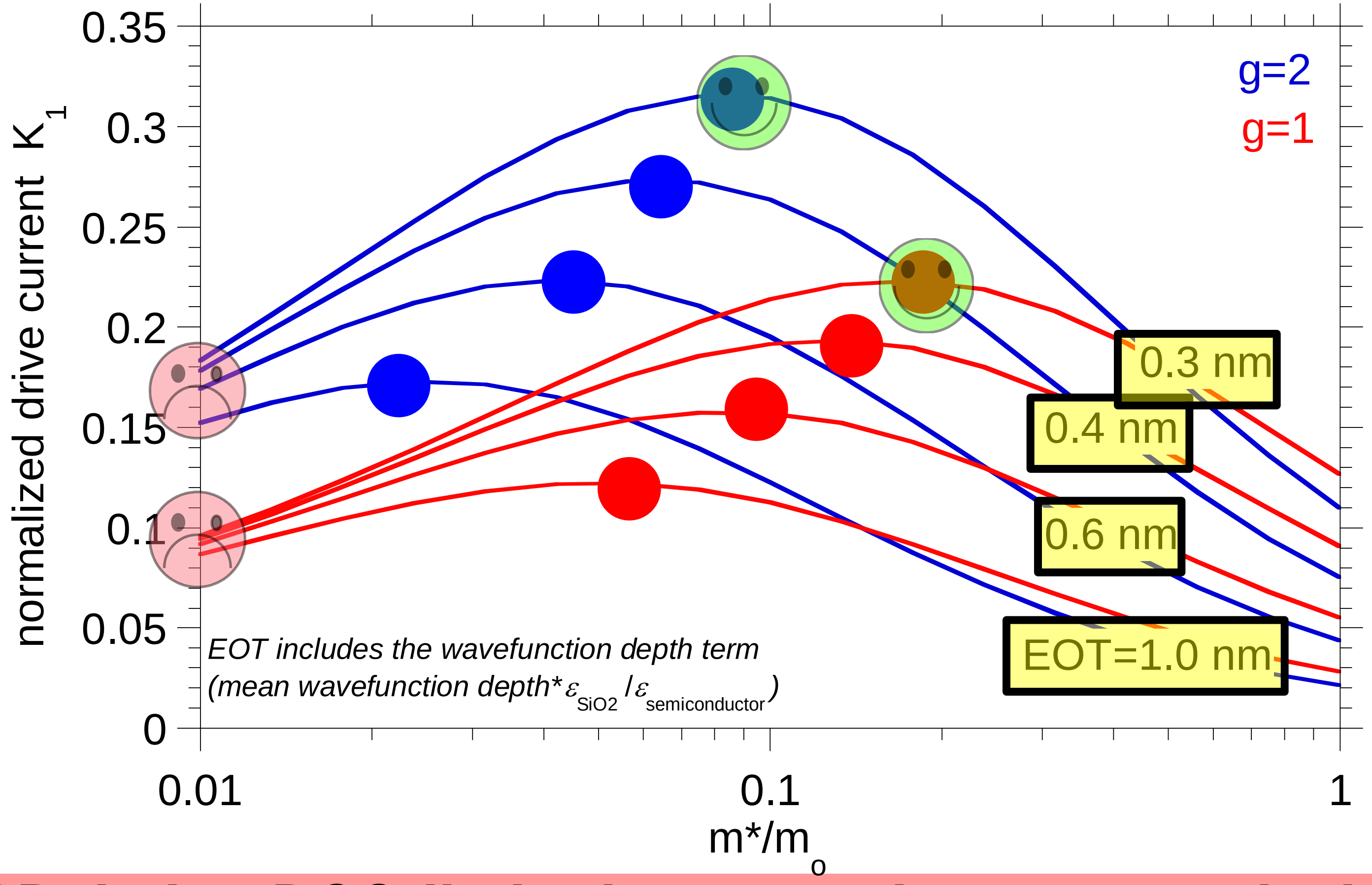
thin channels with high velocity, high DOS

Fundamental limits ...or things to be fixed ?

A good 0.1 nm gate dielectric is very hard to find

Make the best dielectric you can...

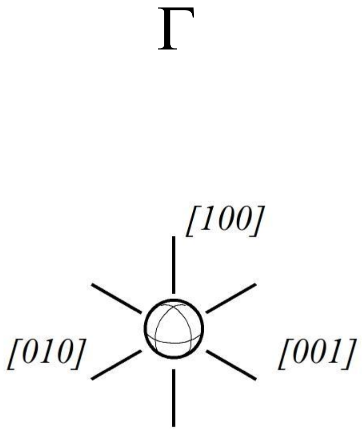
...then pick the channel for the most current you can get !

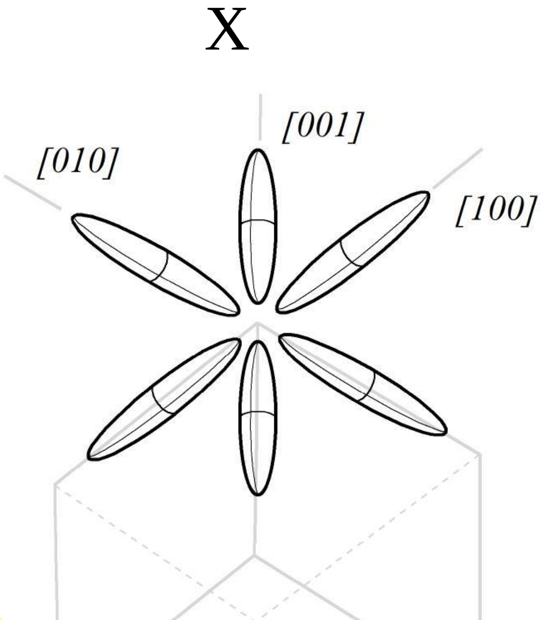


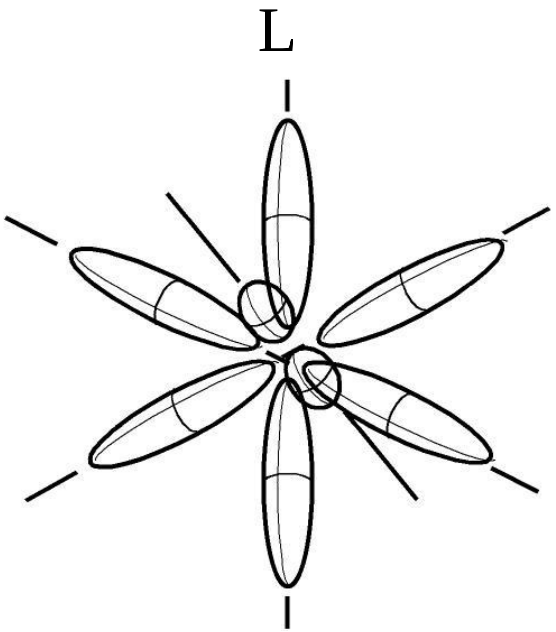
EOT includes the wavefunction depth term (mean wavefunction depth$\varepsilon_{SiO2}/\varepsilon_{semiconductor}$)*

For 2D, being DOS-limited means a low-current design...

L Valleys let us greatly increase the state density

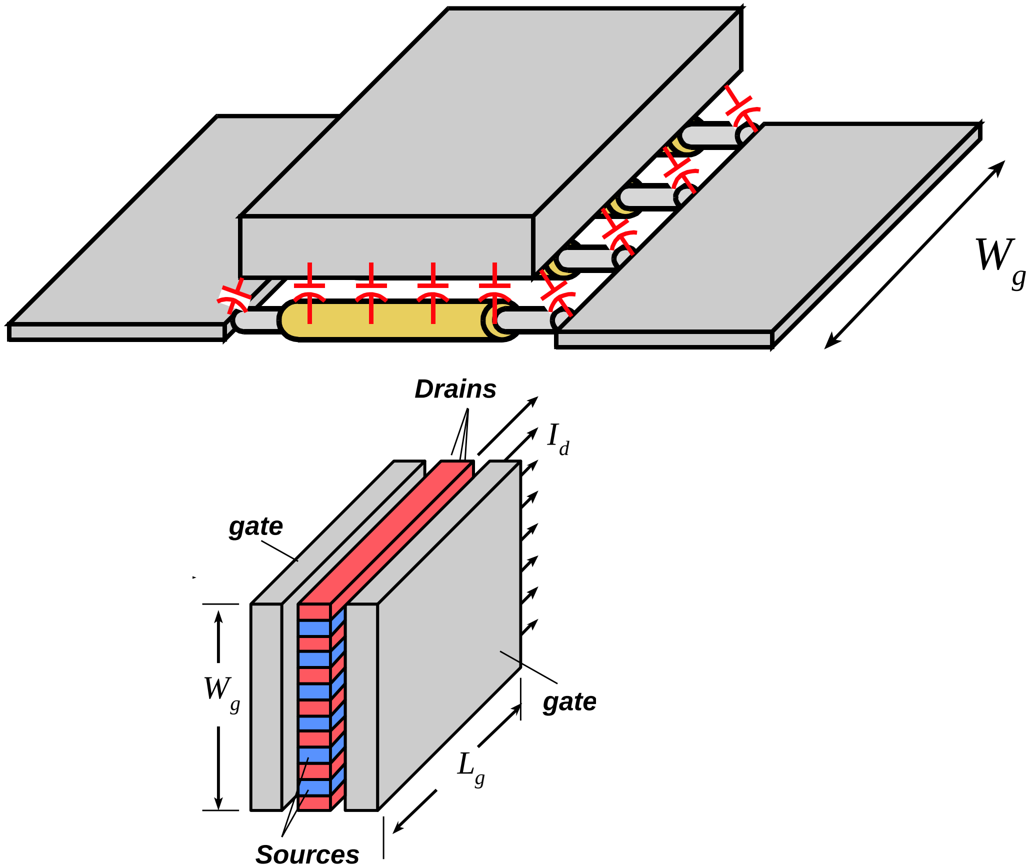




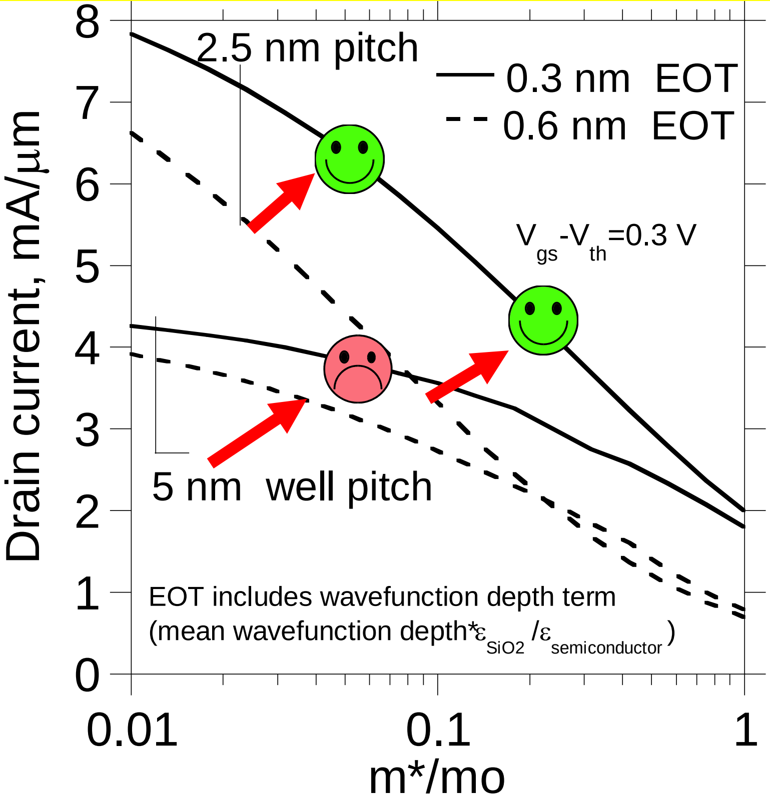


		Γ valley	X valley			L valley		
material	substrate	m^* / m_o	m_l / m_o	m_t / m_o	$E_x - E_\Gamma$	m_l / m_o	m_t / m_o	$E_L - E_\Gamma$
$In_{0.5}Ga_{0.5}As$	InP	0.045	1.29	0.19	0.83 eV	1.23	0.062	0.47 eV
InAs	InP	0.026	1.13	0.16	0.87 eV	0.65	0.050	0.57 eV
GaAs	GaAs	0.067	1.30	0.22	0.47 eV	1.90	0.075	0.28 eV
Si	Si	---	0.92	0.19	(negative)			

Pack 1-D FETs closely, or external parasitics will dominate



for 1-D, low m* seems good...

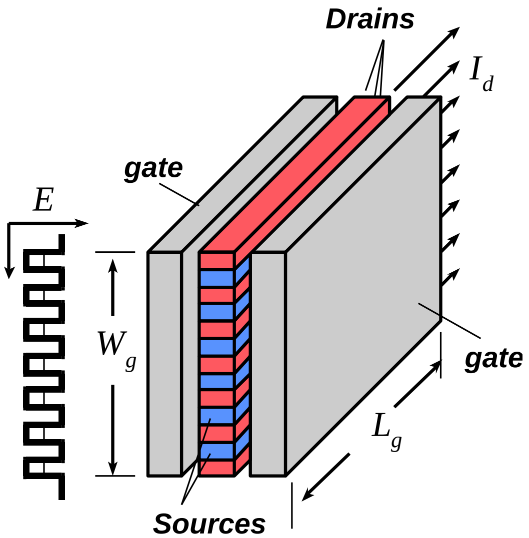


... but low transverse mass prevents close conductor spacing !

....so pick a <u>moderate</u> effective mass

Better still: use an anisotropic band.

Do CNTs beat an L-valley array ???

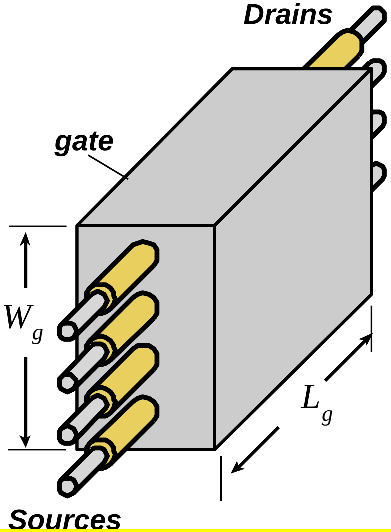


Array of 1D L-valley wells @ 2.5 nm pitch

$$E_{well} = \frac{\hbar^2\pi^2}{2m^* T_{well}^2} = 0.37\text{ eV}, \quad g_{m,well} = 2q^2/h = 78\mu\text{S}$$

$$J = \left(\frac{78\ \mu\text{A}}{2.5\text{ nm}}\right)\left(\frac{E_f - E_c}{1\text{ eV}}\right) = \left(31.2\frac{\text{mA}}{\mu\text{m}}\right)\left(\frac{E_f - E_c}{1\text{ eV}}\right) = 6.4\frac{\text{mA}}{\mu\text{m}}\cdot i$$

for 0.2 eV Fermi level shift in semiconductor



Array of carbon nanotubes, 2.5 nm pitch

$$g_{m,tube} = 4q^2/h = 156\mu\text{S}$$

$$J = \left(\frac{156\ \mu\text{A}}{2.5\text{ nm}}\right)\left(\frac{E_f - E_c}{1\text{ eV}}\right) = \left(62\frac{\text{mA}}{\mu\text{m}}\right)\left(\frac{E_f - E_c}{1\text{ eV}}\right) = 12.5\frac{\text{mA}}{\mu\text{m}}\cdot i$$

for 0.2 eV Fermi level shift in semiconductor

If we are going to talk about devices which we can't build anyway...

then CNTs are not the only imaginary device to pick from

It's silly to fix one problem at a time. . .

$$(1/2\pi f_\tau) = \tau_1 + \tau_2 + \tau_3 + \tau_4 = 50 + 50 + 50 + 50 = 200\ \text{fs}$$

$$(1/2\pi f_\tau) = \tau_1/10 + \tau_2 + \tau_3 + \tau_4 = 5 + 50 + 50 + 50 = 155\ \text{fs}$$ ☹

So we make scaling roadmaps:

Gate length	nm	50	35	25	18	13	9	
Gate EOT	nm	1.17	0.83	0.58	0.41	0.29	0.21	
well thickness	nm	8.0	5.7	4.0	2.8	2.0	1.4	
S/D resistance	Ω–μm	210	148	105	74	53	37	
# bands	––	1	1	1	2	3	3	
effective mass	$*m_0$	0.05	0.05	0.05	0.08	0.08	0.08	
f_τ	GHz	490	700	773	1144	1608	2330	
f_{max}	GHz	552	814	930	1391	1963	2883	
$f_{divider}$	GHz	109	151	219	303	431	576	
I_d/W_g	mA/μm	0.42	0.54	0.69	0.95	1.4	1.8	@ 200 mV overdrive

→ *contacts & dielectrics are as important as the channel*

1-D DOS-limited FETs sure ain't linear

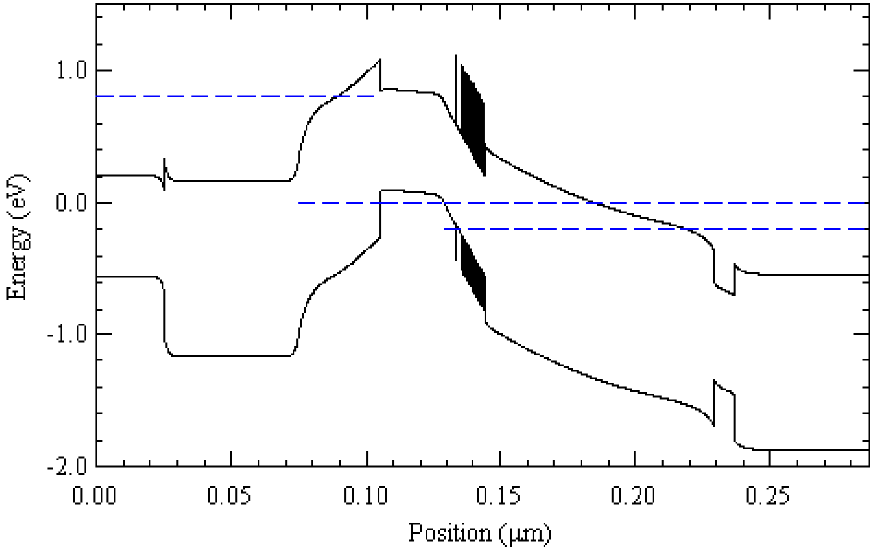
pick your poison....or pick your nonlinearity...

2-D FET: in ballistic limit
- *input capacitance is linear*
- *transconductance is nonlinear*

1-D semiconductor FET: in ballistic limit
- *transconductance is linear...*
- *input capacitance is nonlinear !!!!!!!!!!!!*

When we want linearity, we use bipolars
- *high gm→ linearize by external resistance*
- *fully depleted collectors for low capacitance variation*
- *but then velocity modulation gets us.*

by the way...THz HBTs also see DOS limits

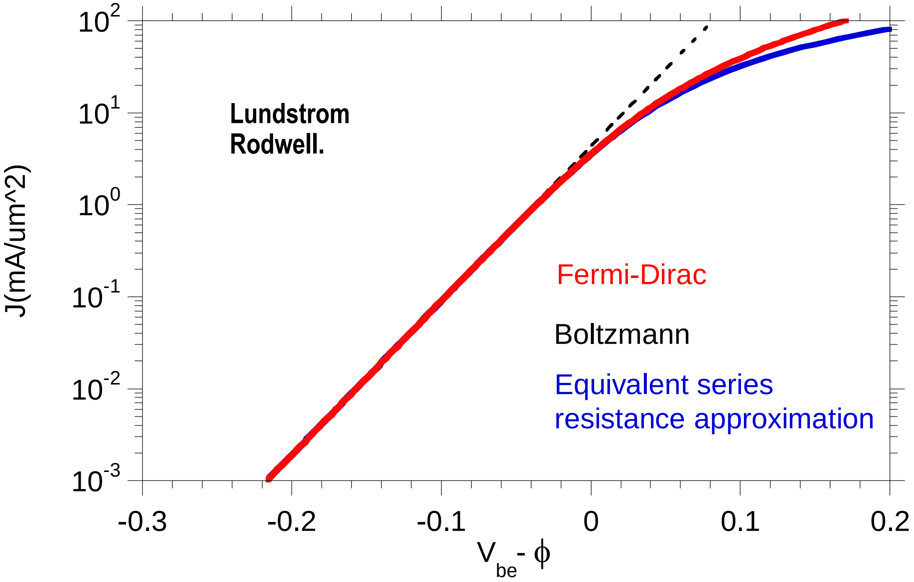


Highly degenerate limit

$$J = \frac{qm^*(E_f - E_c)^2}{2\pi^2\hbar^3}$$

$$= \left(130\,\frac{\text{mA}}{\mu\text{m}^2}\right)\left(\frac{E_f - E_c}{0.1\,\text{eV}}\right)^2$$

for InP emitter ($m^*/m_0 = 0.08$).



Electron degeneracy contributes 1 Ω - μm² equivalent series resistance for InP emitter