High performance 110 nm InGaAs/InP DHBTs in dry-etched *in-situ* refractory emitter contact technology

Vibhor Jain, Evan Lobisser, Ashish Baraskar, Brian J Thibeault, Mark Rodwell
ECE Department, University of California, Santa Barbara, CA 93106-9560

Zach Griffith, Miguel Urteaga
Teledyne Scientific & Imaging, Thousand Oaks, CA 91360

Sebastian T Bartsch
Nanoelectronics Device Laboratory, EPFL, Switzerland

D Loubychev, A Snyder, Y Wu, J M Fastenau, W K Liu
IQE Inc., 119 Technology Drive, Bethlehem, PA 18015

vibhor@ece.ucsb.edu, 805-893-3273

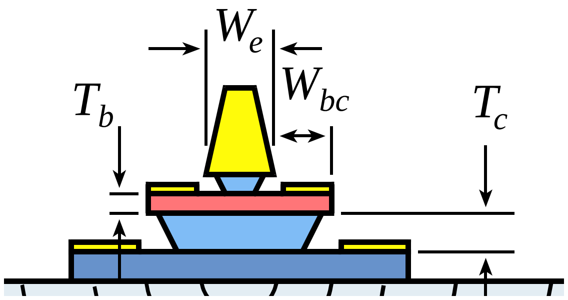
Outline

- HBT Scaling Laws
- Fabrication
  - Challenges
  - Process Development
- DHBT Epitaxial Design
- Results
  - DC & RF Measurements
- Summary

Bipolar transistor scaling laws

$$\frac{1}{2\pi f_\tau} = \tau_{tr} + RC$$

$$f_{\max} = \sqrt{\frac{f_\tau}{8\pi R_{bb,eff} C_{cb,eff}}}$$



(emitter length L_e)

To ***double cutoff frequencies*** of a mesa HBT, must:

Keep ***constant*** all ***resistances*** and ***currents***
Reduce all ***capacitances*** and ***transit delays by 2***

$$\tau_b \approx T_b^2/2D_n + T_b/v_{exit}$$
$$\tau_c = T_c/2v_{sat}$$

Epitaxial scaling

$$C_{cb} = \varepsilon A_c/T_c$$
$$I_{c,\max} \propto v_{eff} A_e (V_{\mathrm{cb}} + \phi_{bi})/T_c^2$$

Lateral scaling

$$R_{ex} = \rho_{\mathrm{contact}}/A_e$$
$$R_{bb} = \rho_{\mathrm{sheet}}\left(\frac{W_e}{12L_e} + \frac{W_{bc}}{6L_e}\right) + \frac{\rho_{\mathrm{contact}}}{A_{\mathrm{contacts}}}$$

Ohmic contacts

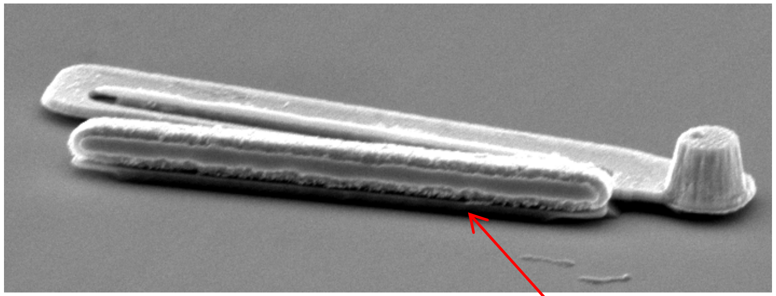
InP Bipolar transistor scaling roadmap

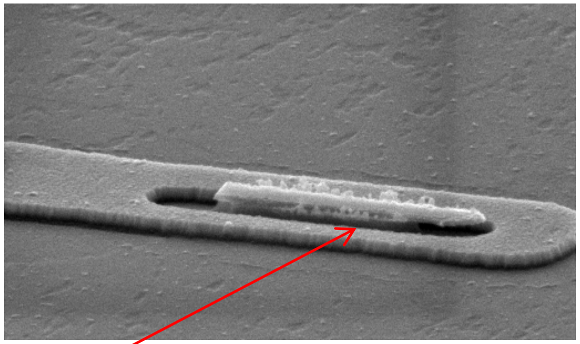
Design	Emitter	*256*	*128*	*64*	*32*	Width (nm)
		8	4	2	1	Access ρ ($\Omega\cdot\mu m^2$)
	Base	175	120	60	30	Contact width (nm)
		10	5	2.5	1.25	Contact ρ ($\Omega\cdot\mu m^2$)
	Collector	106	75	53	37.5	Thickness (nm)
Performance	Current density	9	18	36	72	mA/μm^2
	Breakdown voltage	4	3.3	2.75	2-2.5	V
	f_τ	*520*	*730*	*1000*	*1400*	GHz
	f_{max}	*850*	*1300*	*2000*	*2800*	GHz

Evan Lobisser *et al*, IPRM 2009

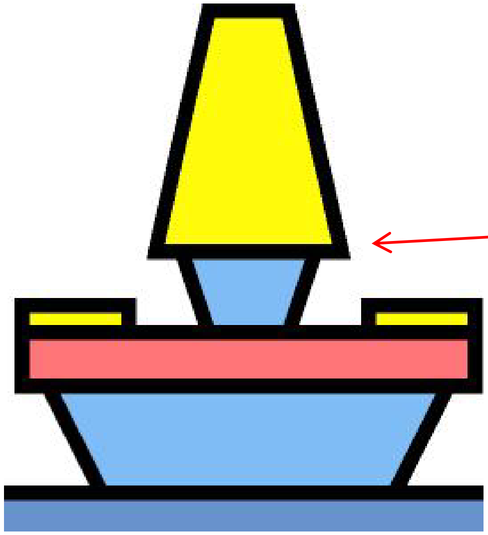
Sub-200 nm HBT node: Fabrication Challenges - I

Emitter yield drops during base contact, subsequent lift-off steps





Fallen emitters



High stress in emitter metal stack

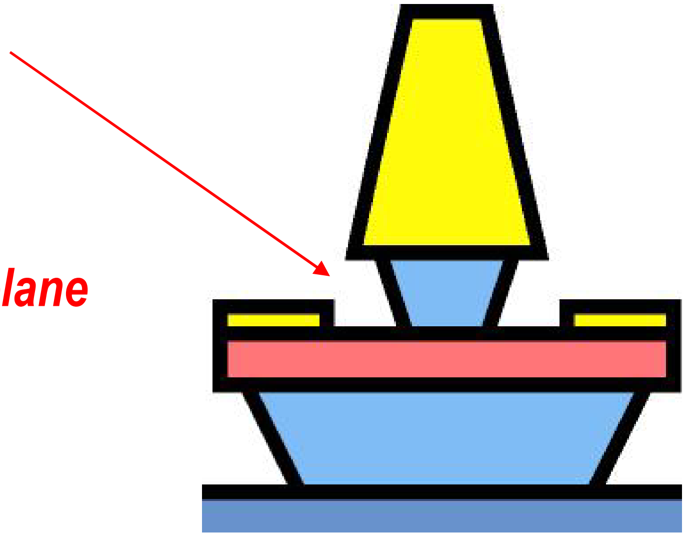
Poor metal adhesion to InGaAs

Need for low stress, high yield emitters

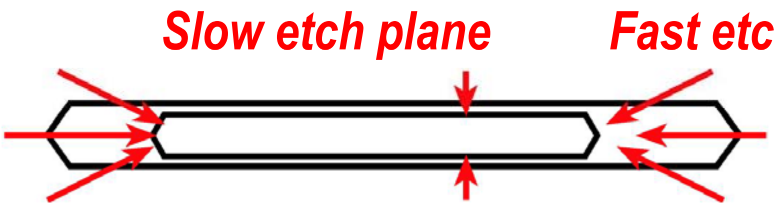
Sub-200 nm HBT node: Fabrication Challenges - II

Undercut in emitter semiconductor

Helps in Self Aligned Base Liftoff



InP Wet Etch



Narrow emitters need controlled semiconductor undercut

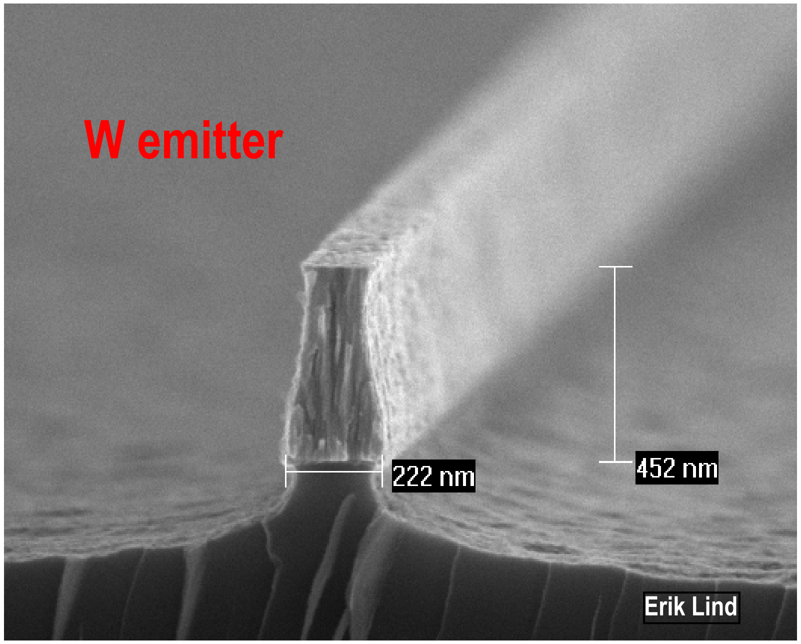
- →**Thin semiconductor**

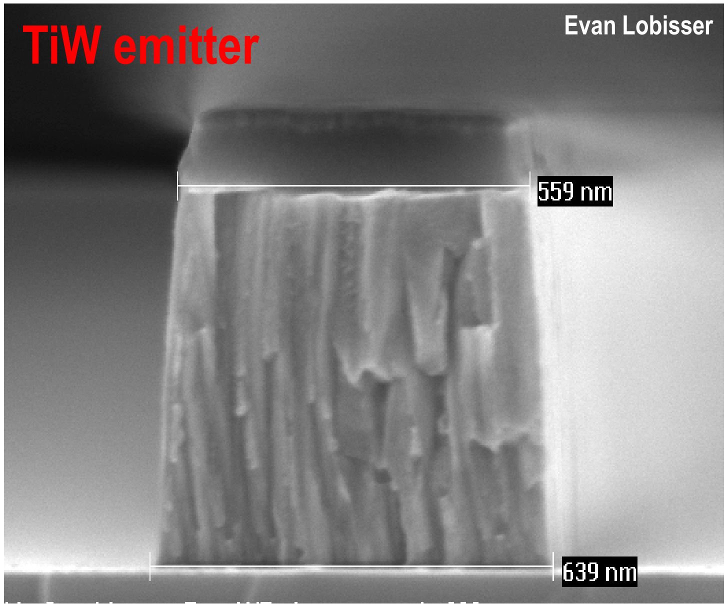
To prevent short, base metal needs to be thinned

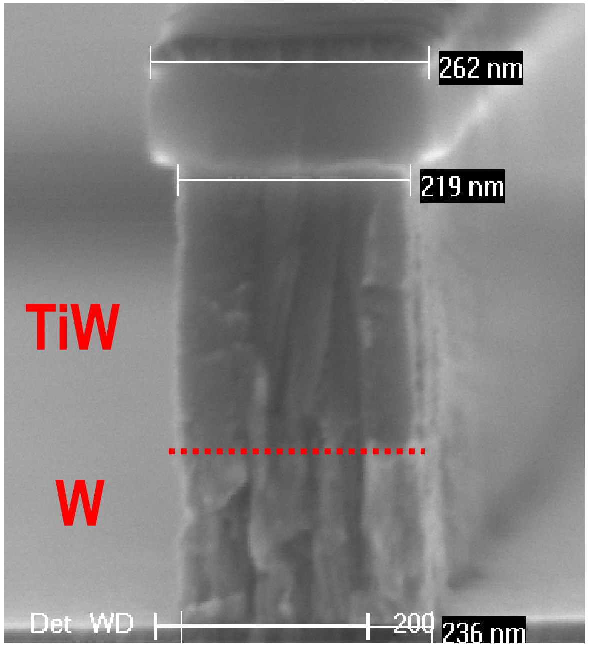
- →**Higher base metal resistance**

Solution: Undercut in the emitter metal to act as a shadow mask

Composite Emitter Metal Stack

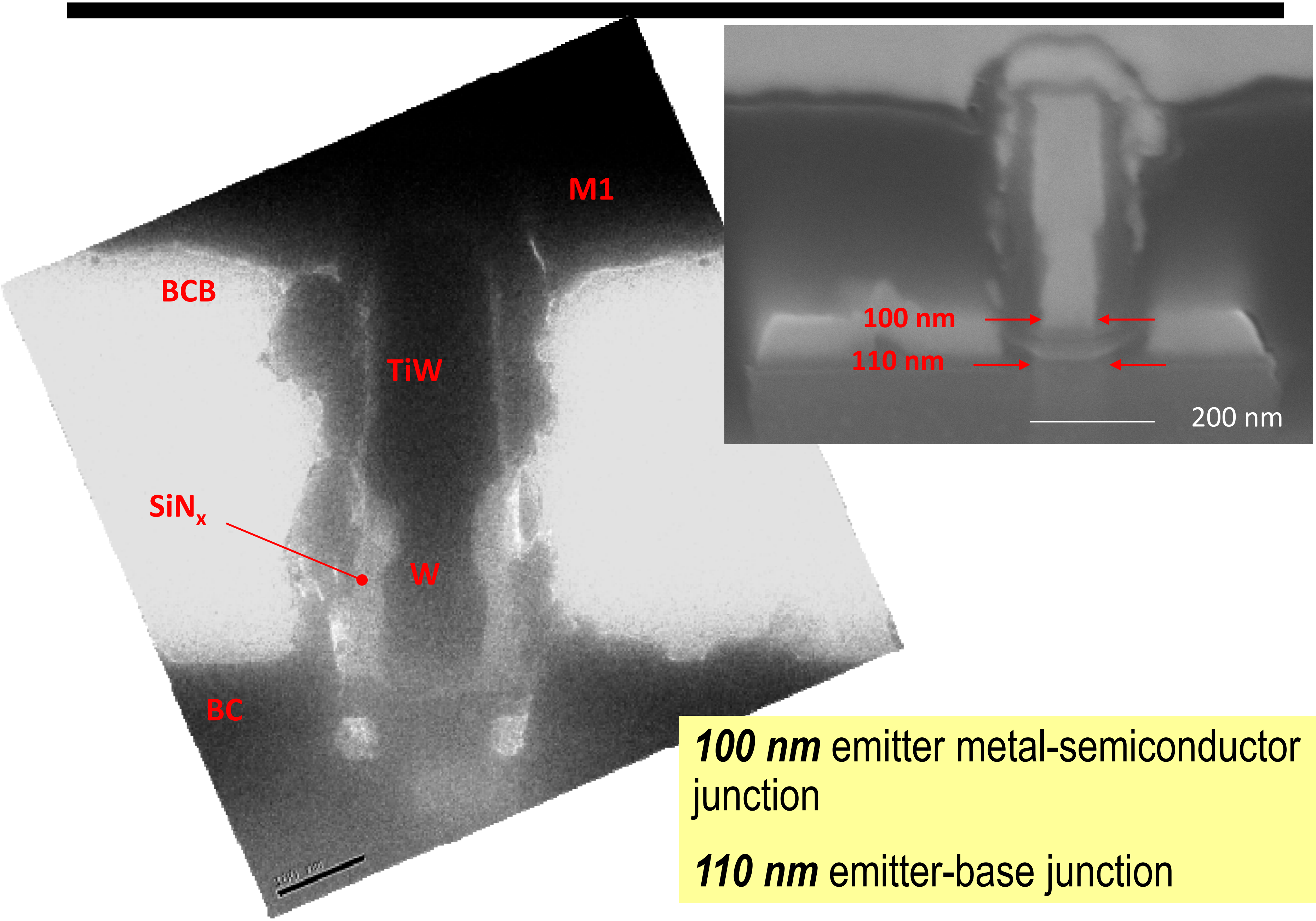






- W/$Ti_{0.1}W_{0.9}$ metal stack
- Low stress
- Refractory metal emitters
- Vertical dry etch profile

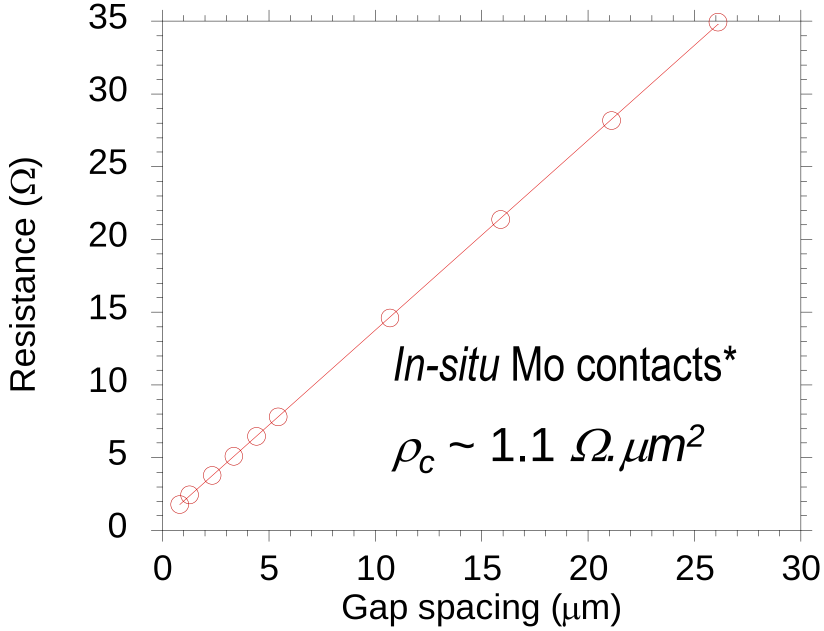
Junction Width via SEM, TEM



100 nm emitter metal-semiconductor junction

110 nm emitter-base junction

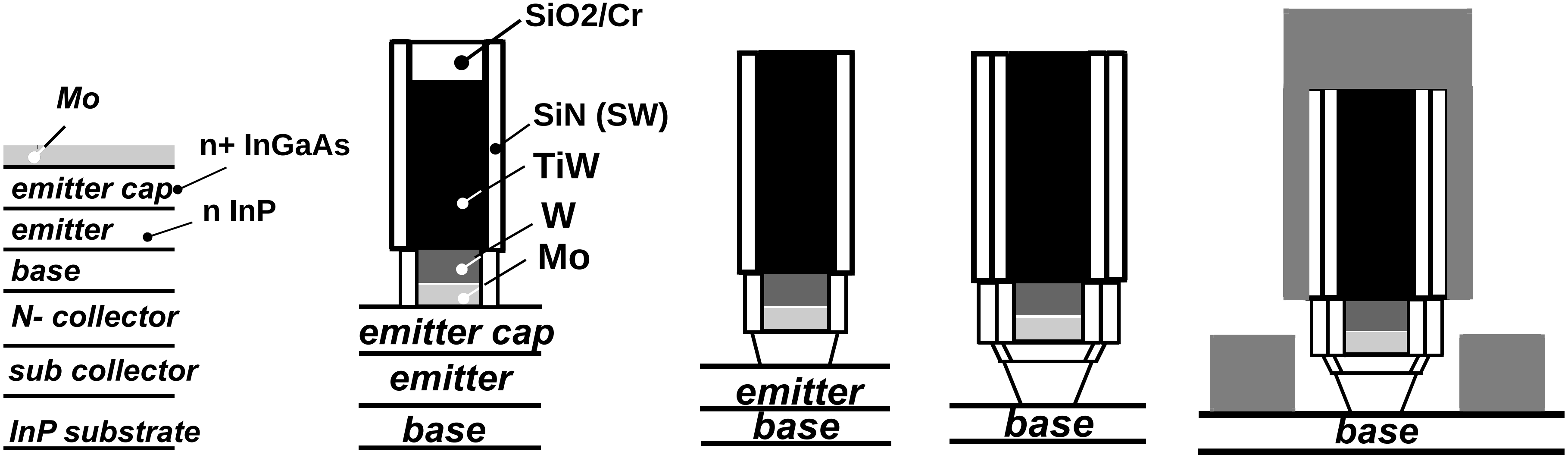
In-situ Emitter Contact



- Highly doped n-InGaAs regrown on IQE InGaAs and *in-situ* Mo deposited
  - Active carriers ~ 5×10^{19} cm^{-3}
- *In-situ* Mo deposition on n-InGaAs - $\rho_c \sim 1.1\ \Omega.\mu m^2$ *
- ***In-situ deposition*** → repeatable contact resistivity

* A. Baraskar *et al.*, *J. Vac. Sci. Tech. B*, 27, 4, 2009

Process flow



Regrown InGaAs emitter cap

In-situ Mo dep

W/TiW/SiO$_2$/Cr dep

SF$_6$/Ar etch

SiN$_x$ Sidewall

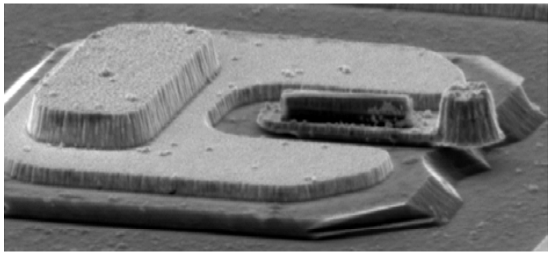
SiO$_2$/Cr removal

InGaAs Wet Etch

Second SiN$_x$ Sidewall

InP Wet Etch

Base Contact Lift-off



W/TiW interface acts as shadow mask for base lift off

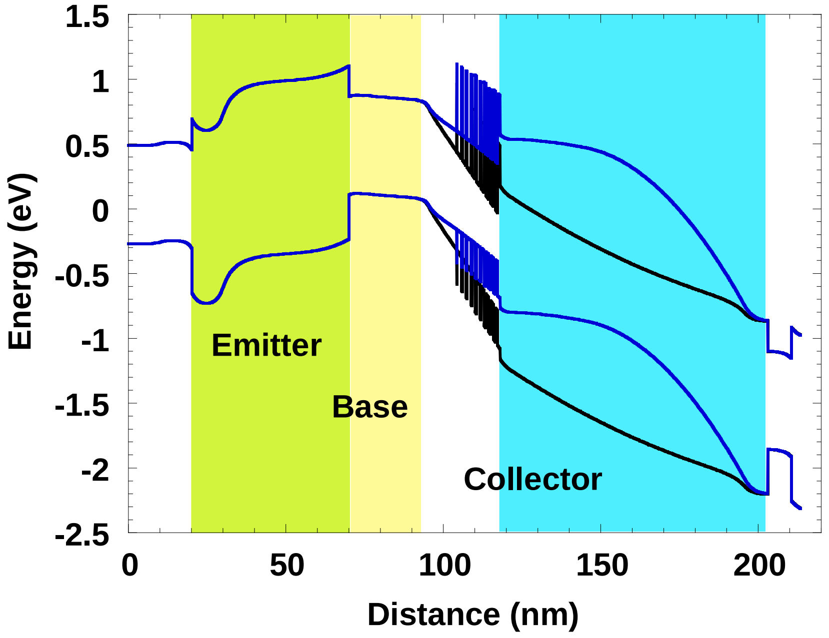
Base and ***collector*** formed via ***lift off*** and ***wet etch***

BCB used to passivate and planarize devices

Self-aligned process flow for 110 nm DHBT

Epitaxial Design

T(nm)	Material	Doping (cm^{-3})	Description
10	$In_{0.53}Ga_{0.47}As$	$5\cdot10^{19}$: Si	Regrown Cap
10	$In_{0.53}Ga_{0.47}As$	$5\cdot10^{19}$: Si	Emitter Cap
10	InP	$4\cdot10^{19}$: Si	Emitter
10	InP	$1\cdot10^{18}$: Si	Emitter
30	InP	$8\cdot10^{17}$: Si	Emitter
25	$In_{0.53}Ga_{0.47}As$	$7\text{-}4\cdot10^{19}$: C	Base
7.5	$In_{0.53}Ga_{0.47}$ As	$9\cdot10^{16}$: Si	Setback
15	InGaAs / InAlAs	$9\cdot10^{16}$: Si	B-C Grade
3	InP	$5\cdot10^{18}$: Si	Pulse doping
74.5	InP	$9\cdot10^{16}$: Si	Collector
7.5	InP	$1\cdot10^{19}$: Si	Sub Collector
7.5	$In_{0.53}Ga_{0.47}$ As	$2\cdot10^{19}$: Si	Sub Collector
300	InP	$2\cdot10^{19}$: Si	Sub Collector
Substrate	SI : InP		



V_{be} = 1 V, V_{cb} = 0.7 V, J_e = 0, 30 mA/μm^2

Thin emitter semiconductor

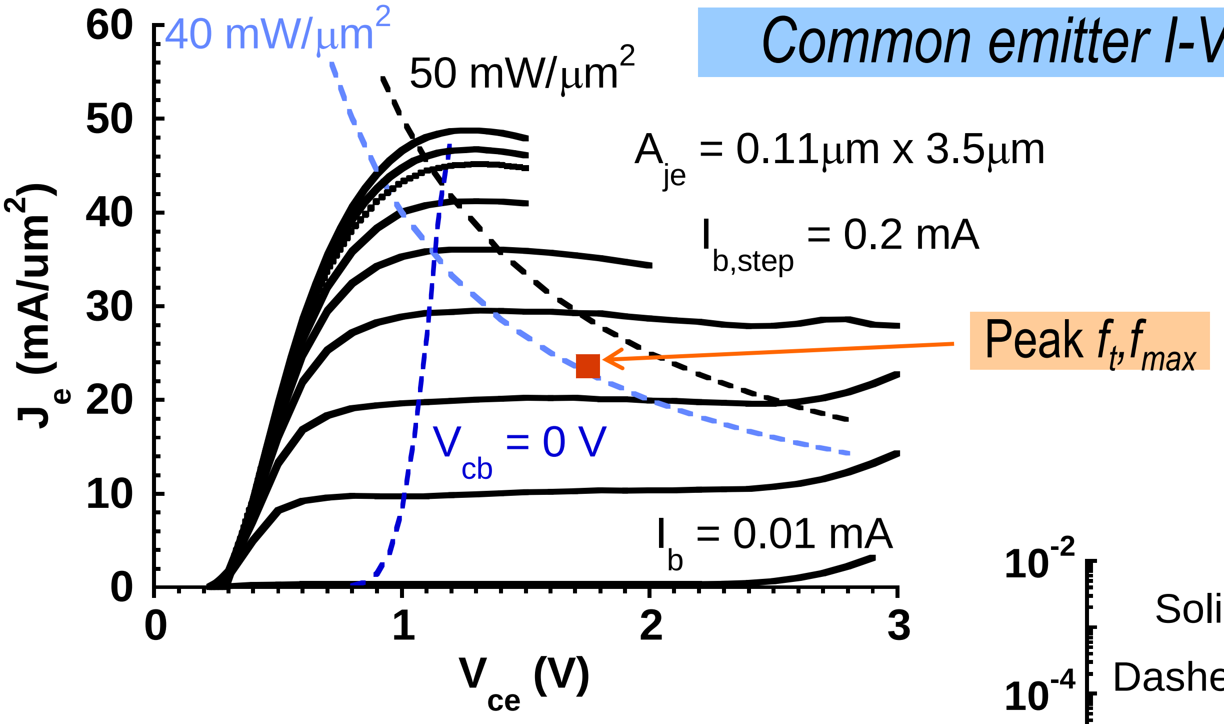
→ Enables wet etching

High collector doping

→ High Kirk threshold

Results - DC Measurements

Common emitter I-V



@Peak f_t,f_{max}

J_e = 23.1 mA/µm^2

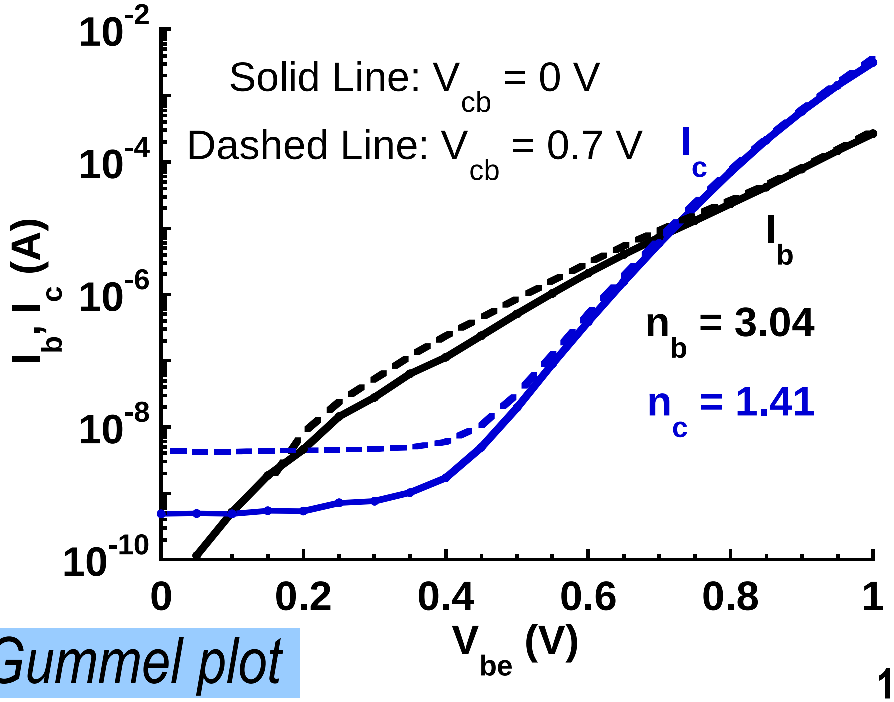
P = 41 mW/µm^2

BV_{ceo} = ***2.5 V*** @ J_e = 1 kA/cm^2

β = ***18***

Base ρ_{sheet} = **730 *Ω/□***, ρ_c < ***4 Ω·µm²***

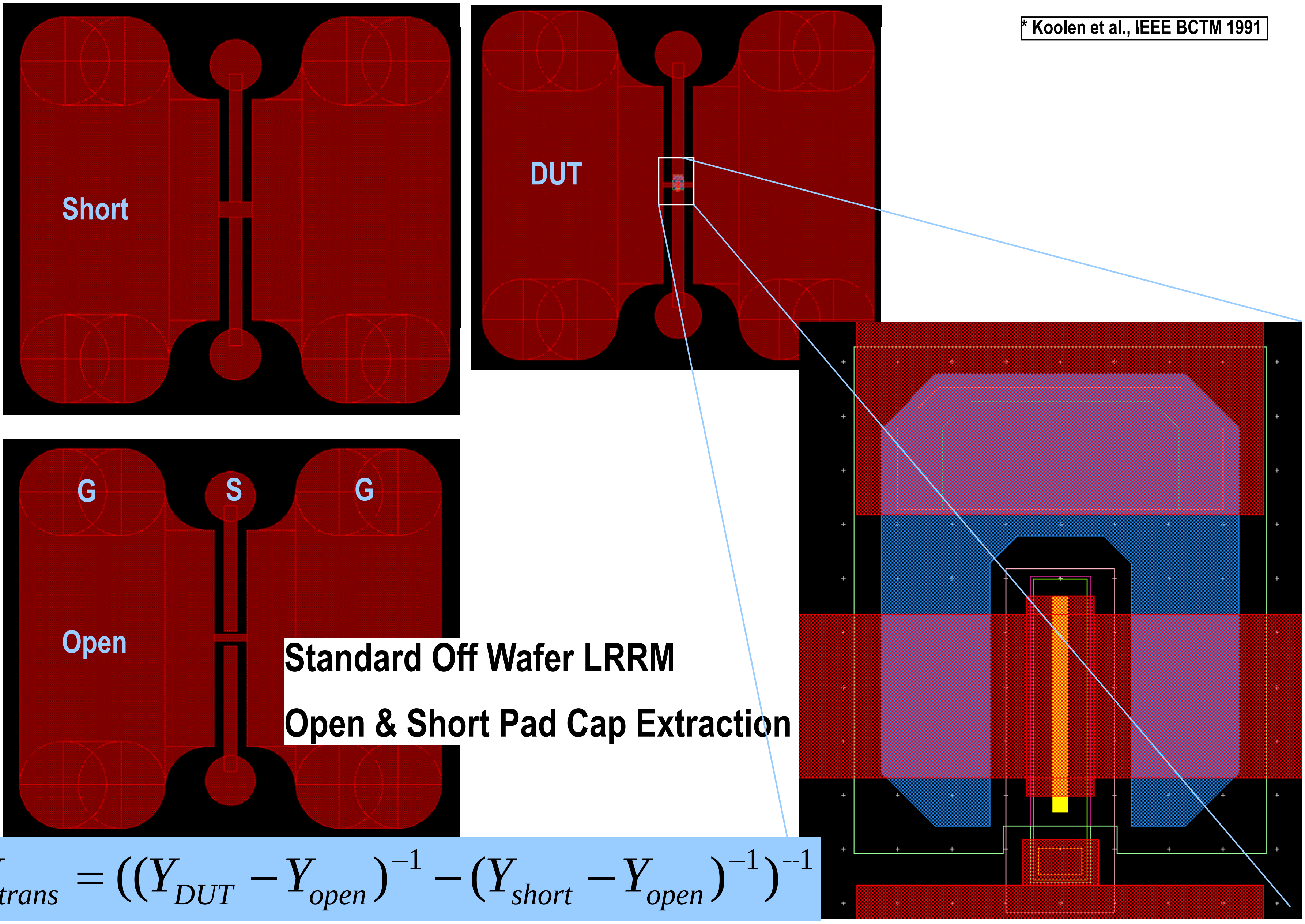
Collector ρ_{sheet} = ***12 Ω/□***, ρ_c = **9 *Ω·µm²***



Gummel plot

Results - RF Measurements using Off-Wafer LRRM

* Koolen et al., IEEE BCTM 1991

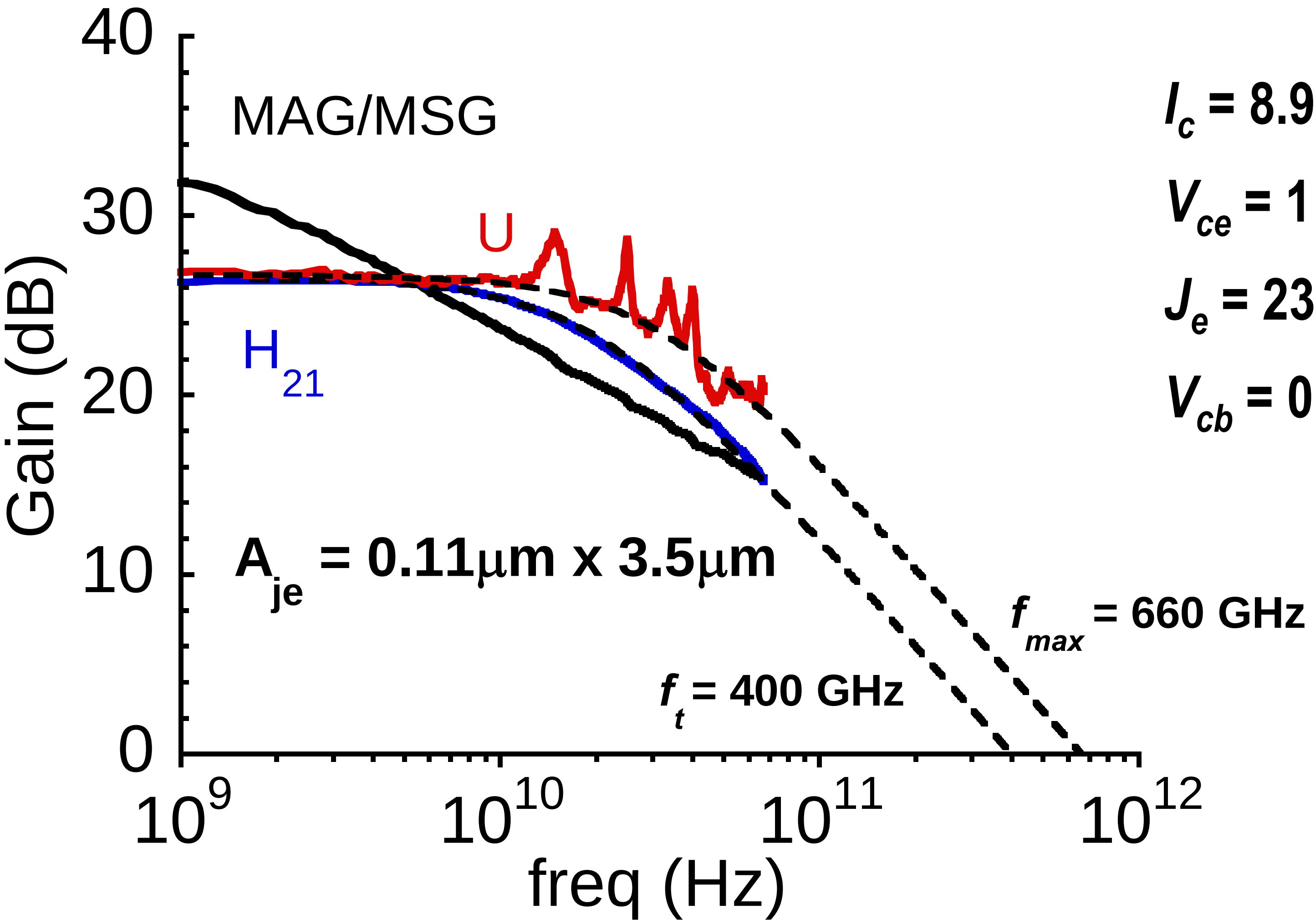


Standard Off Wafer LRRM

Open & Short Pad Cap Extraction

$$Y_{trans} = ((Y_{DUT} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1})^{--1}$$

1-67 GHz RF Data and Extrapolated Cutoff Frequencies



I_c = 8.9 mA

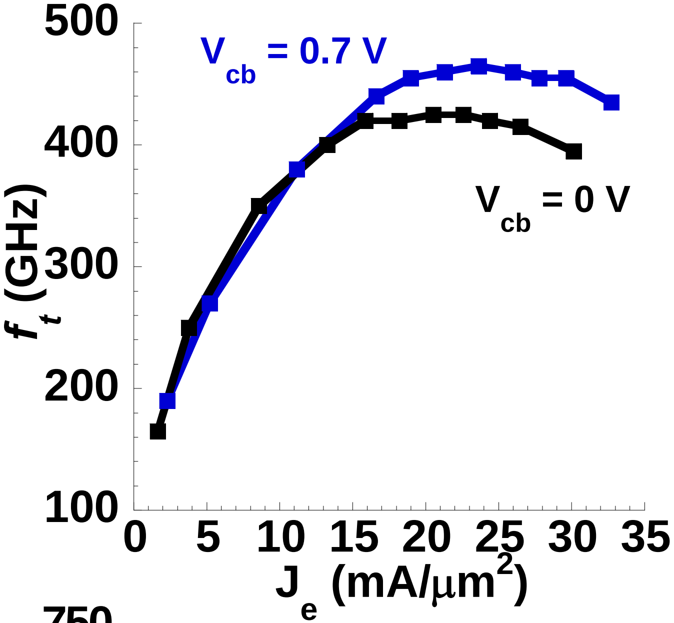
V_{ce} = 1.74 V

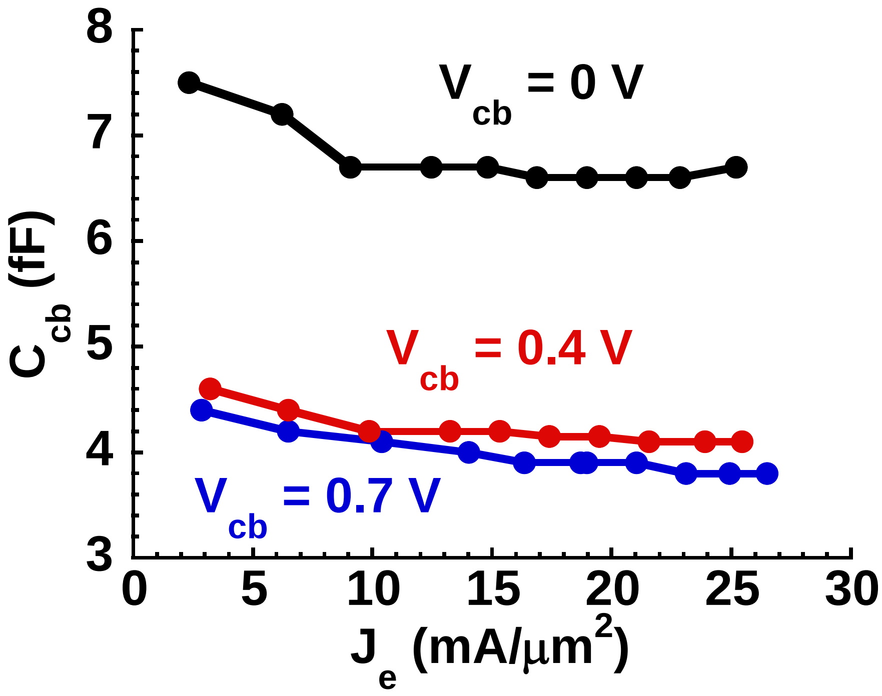
J_e = 23.1 mA/µm^2

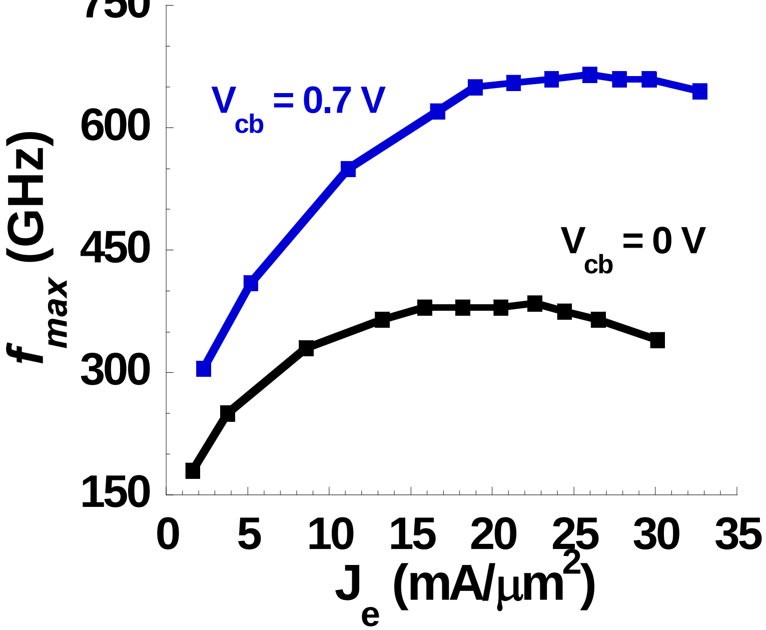
V_{cb} = 0.7 V

Single-pole fit to obtain cut-off frequencies

Parameter Extraction





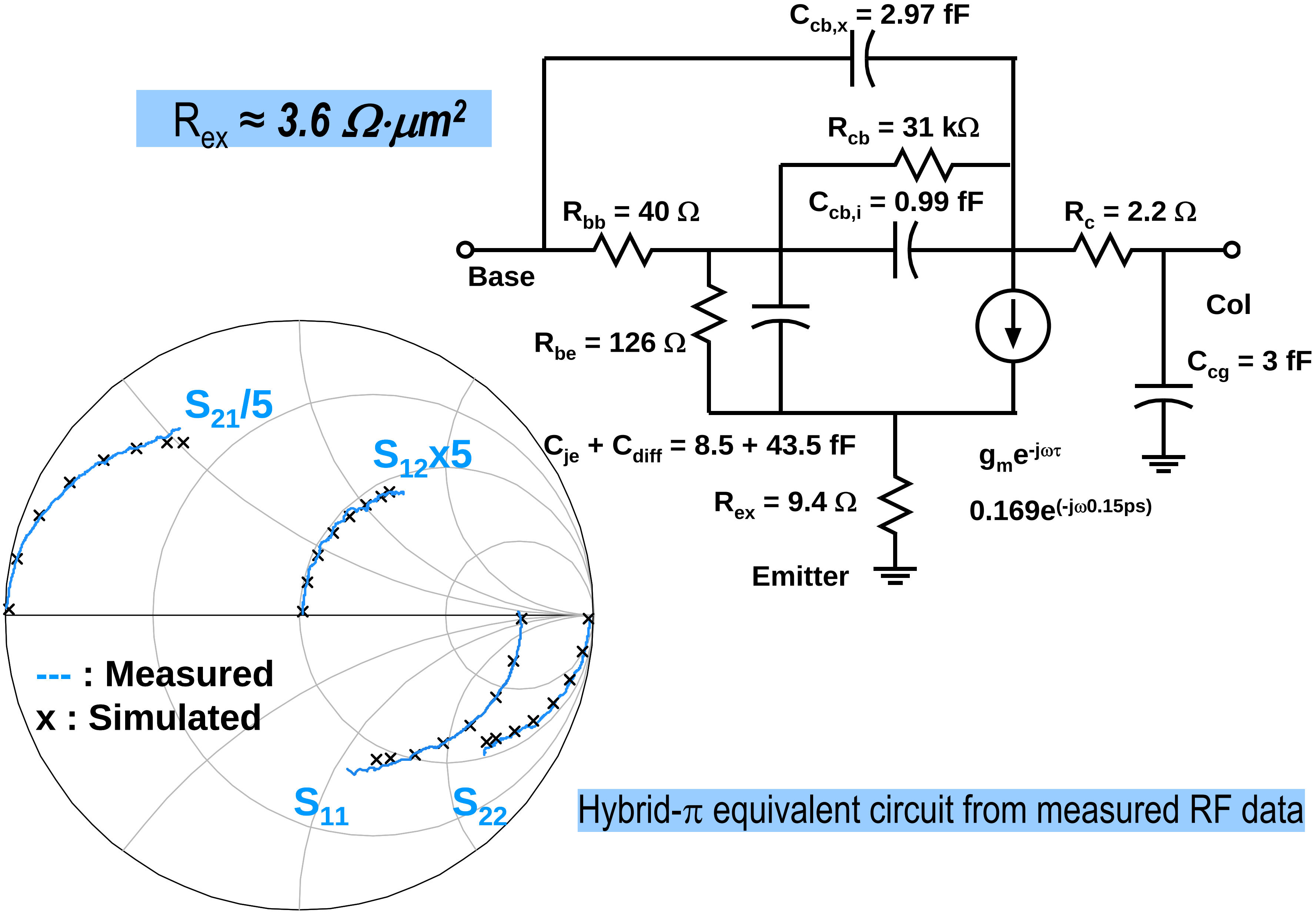


J_{kirk} = 32 mA/μm^2 (@V_{cb} = 0.7V)

C_{cb}/I_c = 0.43 psec/V

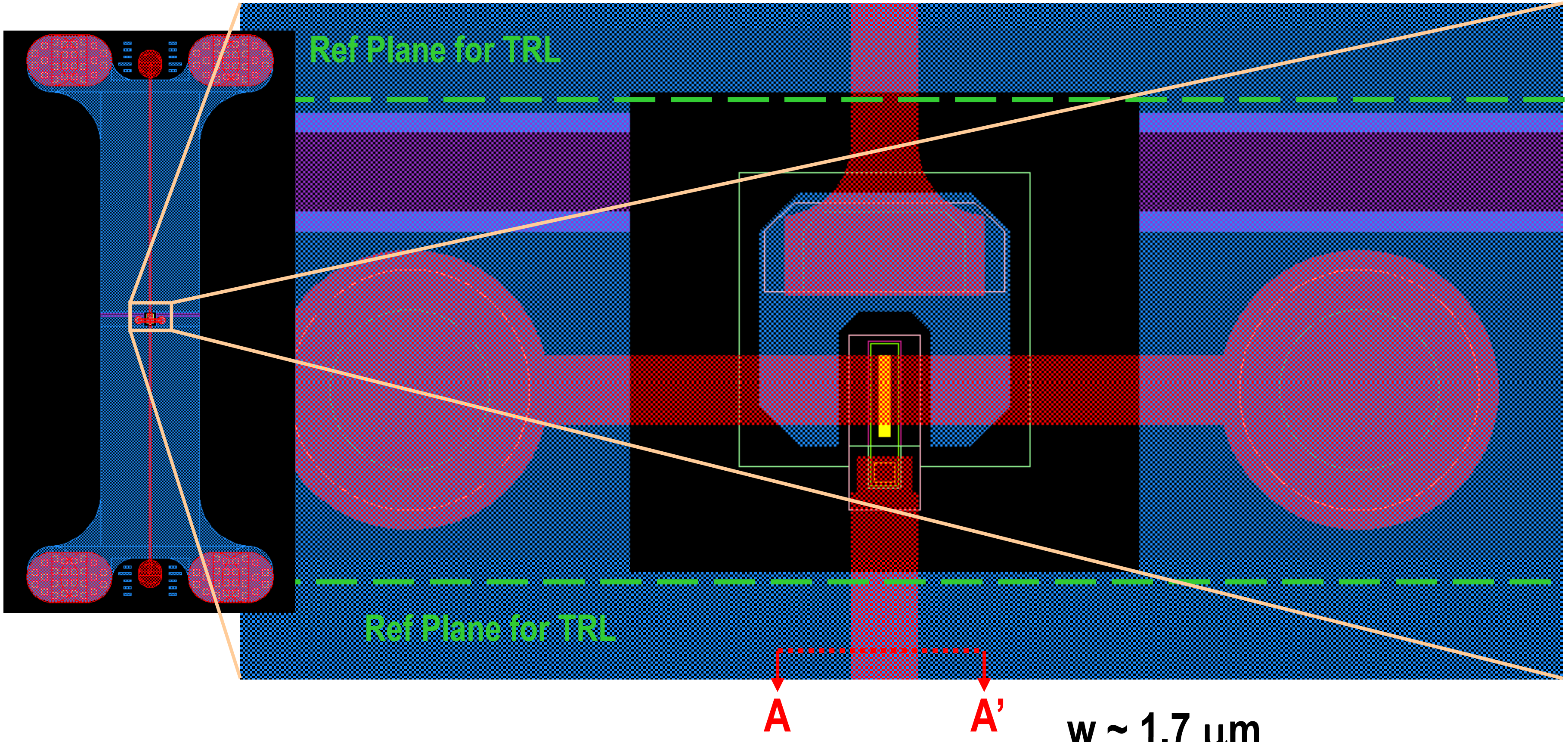
Equivalent Circuit

$R_{ex} \approx 3.6\ \Omega \cdot \mu m^2$



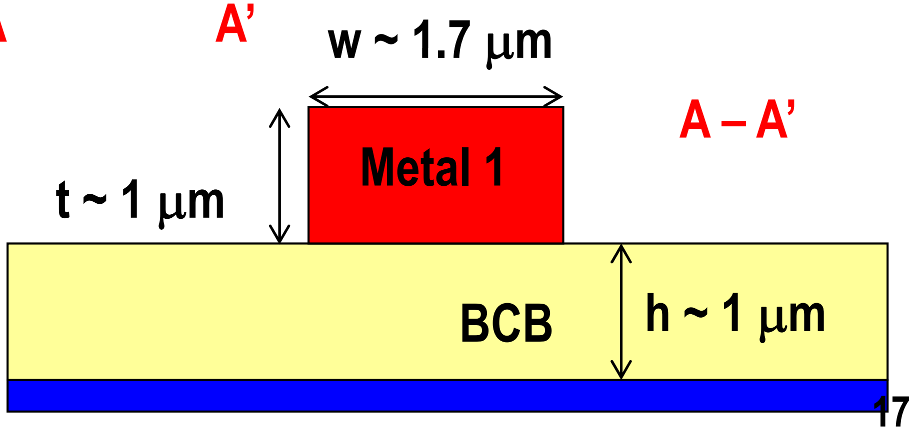
Hybrid-π equivalent circuit from measured RF data

Microstrip Style TRL Calibration

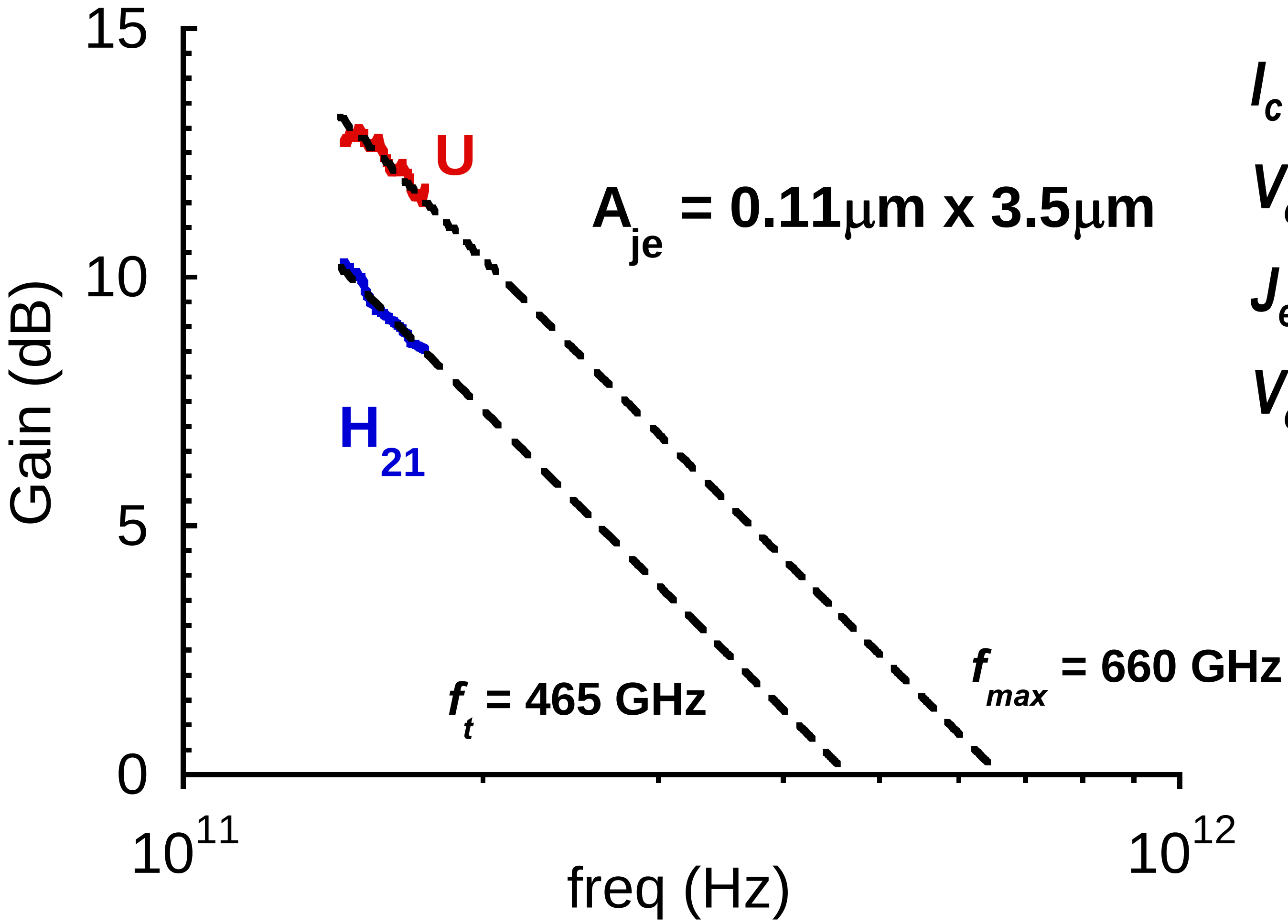


Ref Plane set at device edge

No further de-embedding required



140-180GHz RF data



A_{je} = 0.11µm x 3.5µm

f_t = 465 GHz

f_{max} = 660 GHz

I_c = 9.1 mA

V_{ce} = 1.75 V

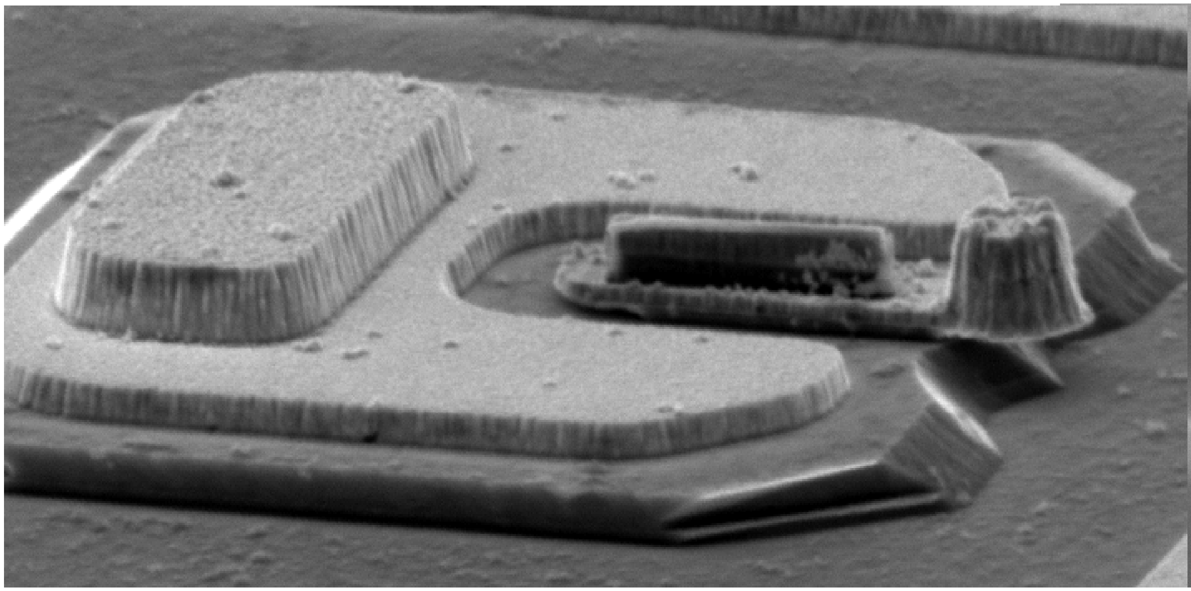
J_e = 23.6 mA/µm^2

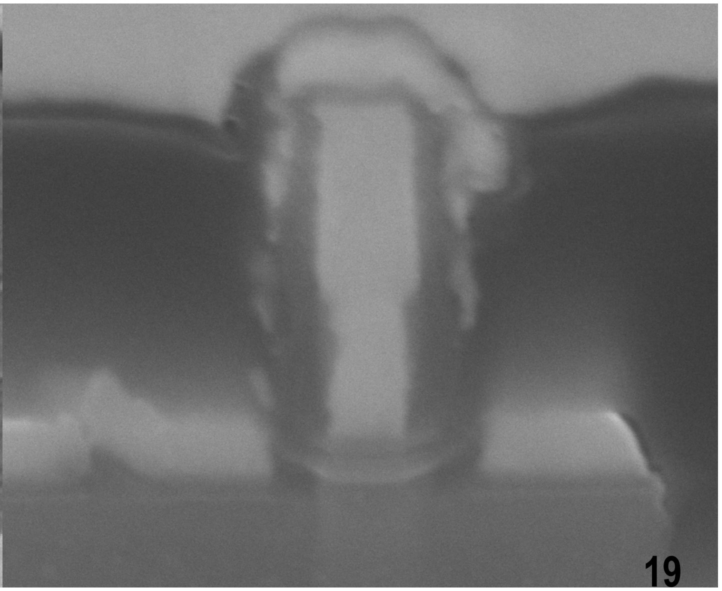
V_{cb} = 0.7 V

-20dB/decade fit to obtain cut-off frequencies

Conclusion

- Demonstrated smallest junction width for a III-V DHBT (110 nm)
- Peak f_t/f_{max} = 465/660 GHz
  - J_e = 23.6 mA/μm^2
  - Power Density (P) = 41 mW/μm^2
- High current and power density operation (P > 50 mW/μm^2)





Thank You

Questions?

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