100-1000 GHz Bipolar ICs: Device and Circuit Design Principles

Part II: Design / Testing of 300 GHz ICs in InP HBT Technology

Munkyo Seo (mkseo@ieee.org)

Mixed-Signal Product Group,

Teledyne Scientific Company (TSC),

Thousand Oaks, CA

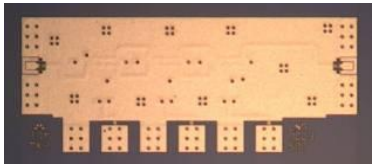
Collaborators / Funding Source

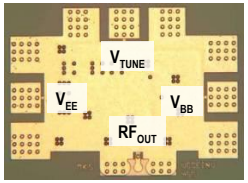
- **Teledyne Scientific Company**
  - — Technology/RF/MMIC Group: Miguel Urteaga, Jon Hacker, Adam Young, Zach Griffith, Richard Pierson, and Petra Rowell
  - — Mixed-Signal Product Group: M.J. Choe
  - — Cleanroom Staff
  - — Internal oversight and vision provided by Dr. Bobby Brar (President, Teledyne Scientific Company)
- **University of California, Santa Barbara (UCSB)**
  - — Professor Mark Rodwell and his Device Team.
- **NASA Jet Propulsion Lab., CA**
  - — Dr. Anders Skalare, Alejandro Peralta, Robert Lin
- **University of Virginia**
  - — Professor Robert Weikle, Professor Scott Barker and their team
- **Program support from Dr. John Albrecht (DARPA) and Dr. Alfred Hung (ARL) is gratefully acknowledged.**
  - — **DARPA THz Electronics Program (Contract #: HR0011-09-C-0060)**
  - — **DARPA Hi-Five Program (Contract #: W911NF-08-C-0050)**

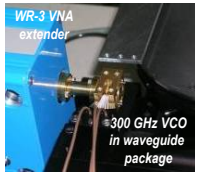
**The views, opinions and/or findings contained in this presentation are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Defense Advanced Research Projects Agency, or the Department of Defense.*

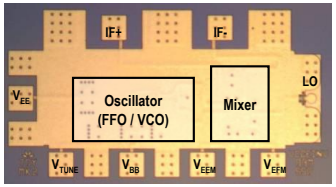
Outline

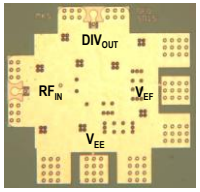
- Overview / General Considerations in > 300 GHz IC Design
- Transceiver Building Blocks
  - 350 GHz Differential LNA
  - 300 GHz Differential Oscillator
  - 300 GHz Dynamic Frequency Divider
- 350 GHz Single-Chip Receiver IC
- 300 GHz Single-Chip PLL IC
- Conclusion

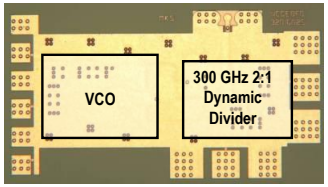


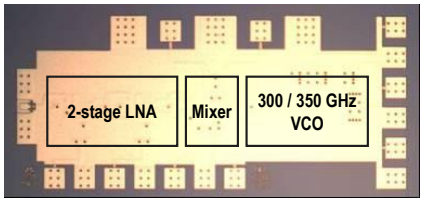


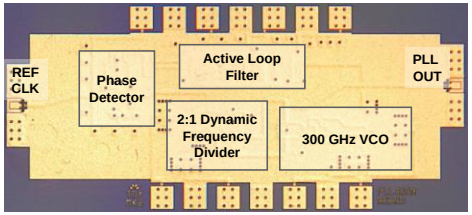


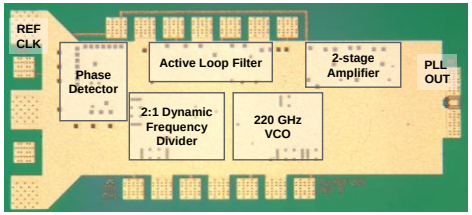






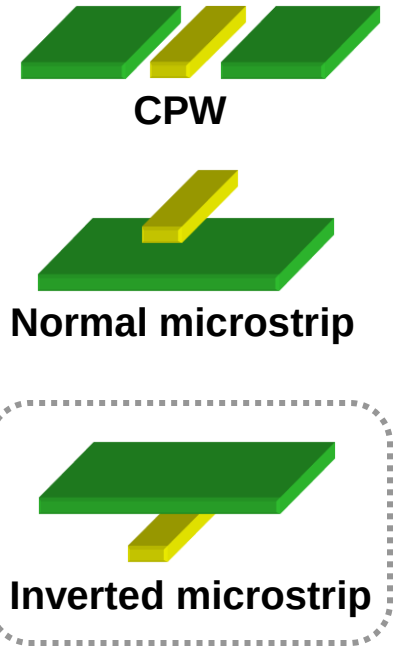




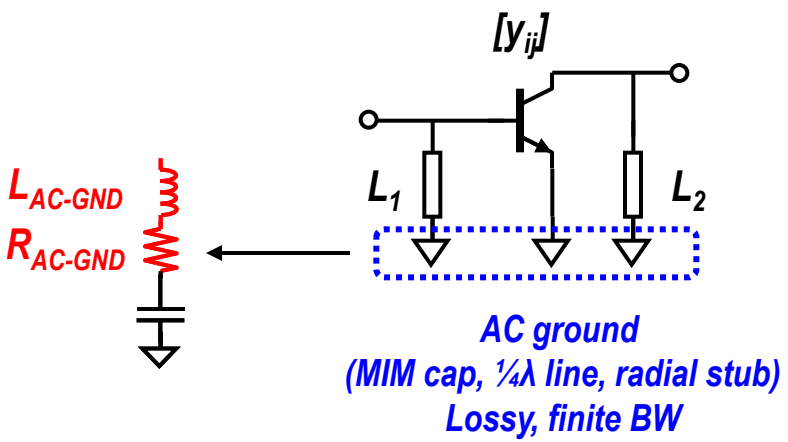


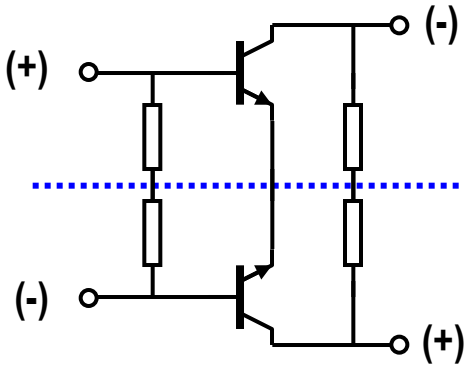
Challenges in > 300 GHz IC Design & Characterization

- **Low transistor gain / high passive loss**
  - — Diff. topology removes AC-ground loss
- **Modeling (Device / *EM*) uncertainties**
  - — Diff. topology removes AC-ground impedance
  - — Inverted Microstrip → Guaranteed *solid* ground plane
    - Normal microstrip → Many holes due to HBT conn.
    - CPW → Not suitable for complex / feedback ckts
- **Many *CKT-EM* cycles**
- **Testing**
  - — Everything is $$$ (money / delivery time) : VNA / mixer / source / probe…
  - — Exploit on-chip self-testing:
    - – Integrated OSC+Mixer / OSC+Divider / LNA+Mixer



Differential Topology for mm-wave ICs





$$\text{Gain drop per stage} = \left(\frac{Q_{L1,eff}}{Q_{L1,eff}+Q_{11}}\right)\left(\frac{Q_{L2,eff}}{Q_{L2,eff}+Q_{22}}\right)$$

$$\text{BW reduction per stage} = \left(\frac{L_1}{L_1+L_{AC-GND}}\right)\left(\frac{L_2}{L_2+L_{AC-GND}}\right)$$

- **Differential topology eliminates**
  - — **(1) Gain reduction due to $R_{AC\text{-}GND}$**
  - — **(2) BW reduction due to $L_{AC\text{-}GND}$**
  - — **(3) Detuning due to MIM cap model errors → Robust design**
  - — **(4) Detuning due to bias ckt & via (→ 3D) model errors → Robust design**
- **Differential topology decouples RF from DC BIAS → Flexible design**

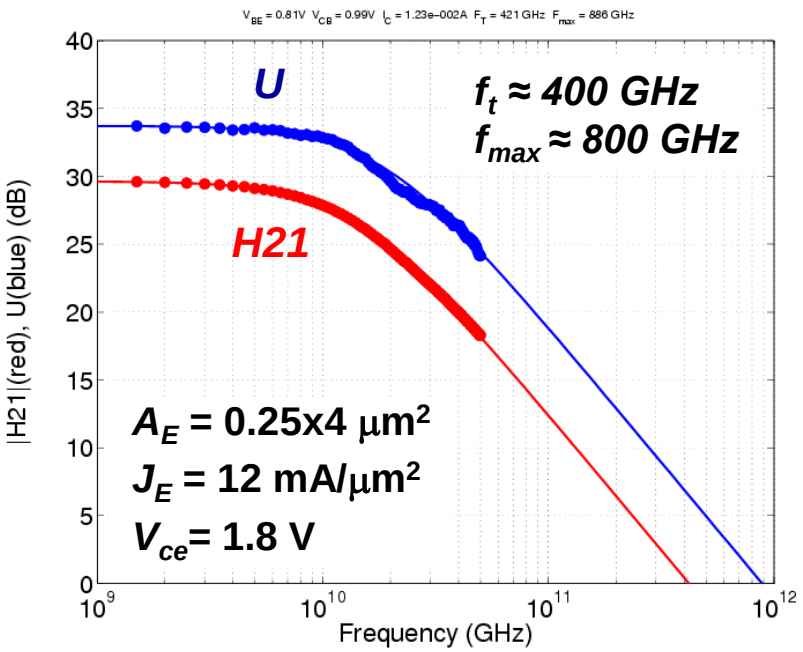
  …at the cost of P_{DC}↑, Area↑, # device↑
- **Caution: Common-mode Stability**

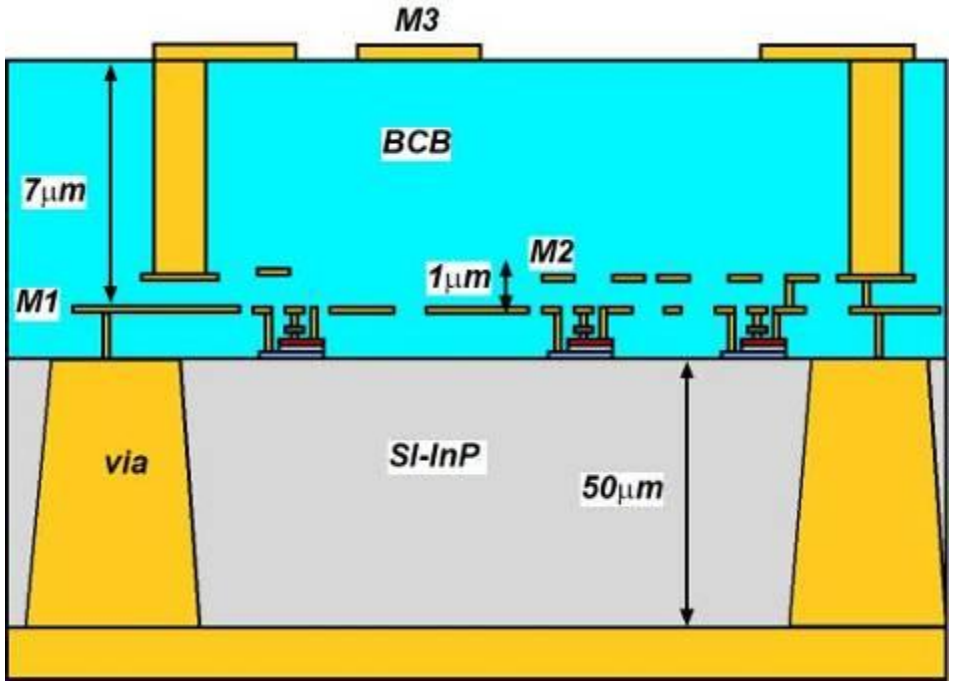
L_1, L_2 input/output matching inductance
R_{AC-GND} ac-ground resistance at resonance
L_{AC-GND} ac-ground series inductance

$Q_{L1,eff} = \omega L_1/(R_{L1}+R_{AC-GND})$
$Q_{11} = \text{Im}(y_{11})/\text{Re}(y_{11})$
$[y_{ij}]$ Transistor $y-$parameter
$Q_{L2,eff}, Q_{22}$ similarly defined.

$$\begin{pmatrix} S_{11}S_{12}S_{13}S_{14} \\ S_{21}S_{22}S_{23}S_{24} \\ S_{31}S_{32}S_{33}S_{34} \\ S_{41}S_{42}S_{43}S_{44} \end{pmatrix} \rightarrow \begin{pmatrix} S_{DM}S_{DM} & 0 & 0 \\ S_{DM}S_{DM} & 0 & 0 \\ 0 & 0 & S_{CM}S_{CM} \\ 0 & 0 & S_{CM}S_{CM} \end{pmatrix}$$

Teledyne 0.25μm InP HBT Process: Overview

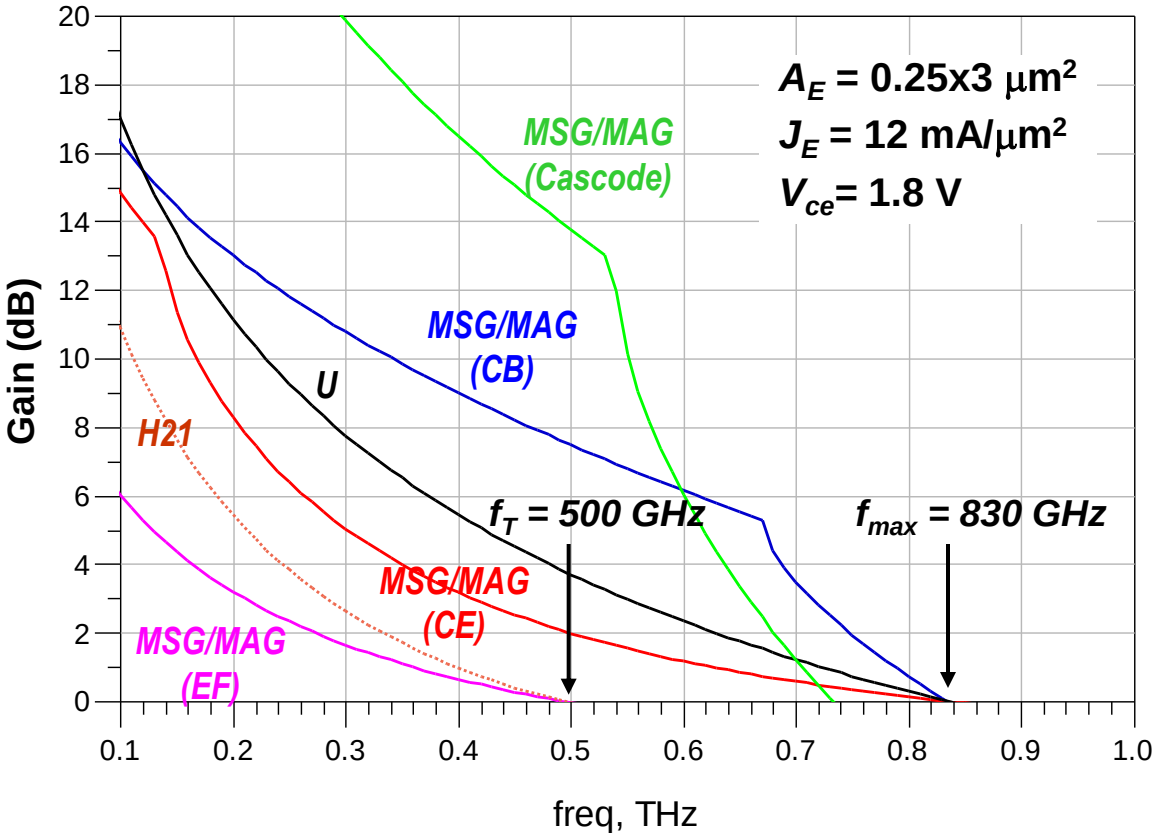


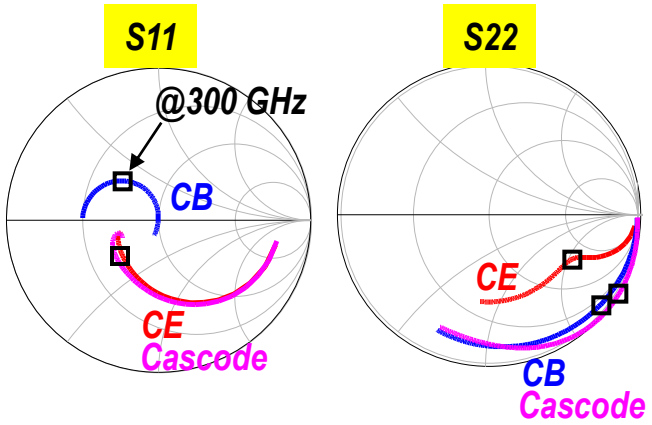


VCO, DIV *VCO, DIV, PLL, LNA, Receiver*

- Two process generations: THzIC1 (f_{max}~600G), THzIC2 (f_{max}~800G)
- 3-Metal (*Au*) back-end: M1, M2, M3 (all 1μm thick)
- Thin-film resistor (50Ω/sq), MIM cap (0.3fF/μm²), B-C junction varactor
- Optional wafer thinning & Thru-wafer vias
- Packaging in a silicon micromachined waveguide block.

0.25μm InP HBT RF Performance

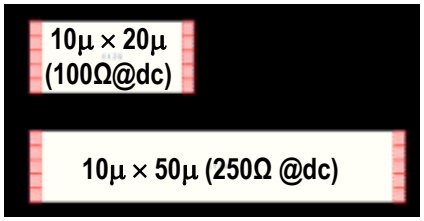


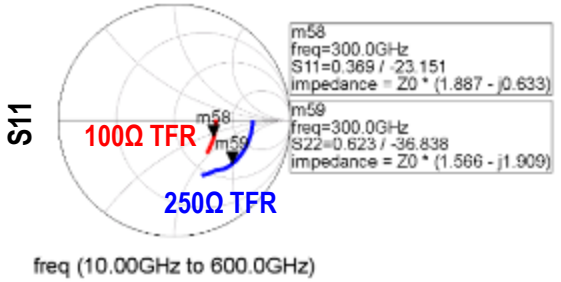


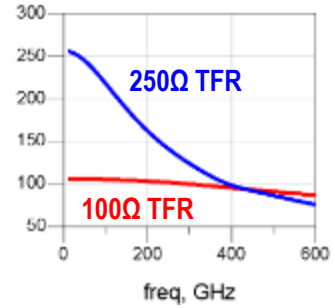
- At 300 GHz, MAG_{CE}= 5 dB, MSG_{CB}=10.8 dB, $MSG_{cascode}$ = 20 dB
- In actual circuits, operating gain will be further limited by: (1) stabilization (if unstable), (2) matching network losses, and (3) large-signal operation (e.g. oscillators or power amplifiers)

Passive Device Modeling

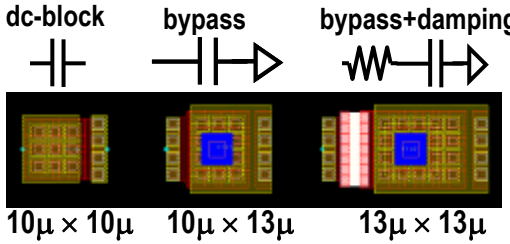
Thin-Film Resistors (TFR)

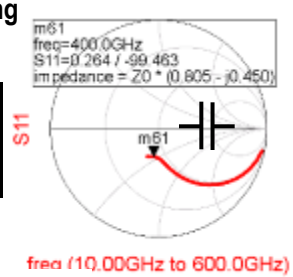


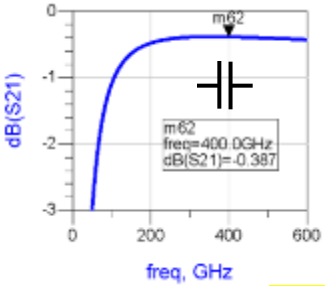


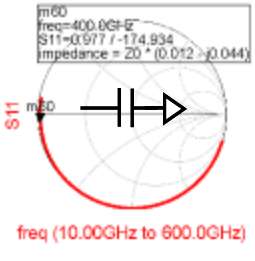


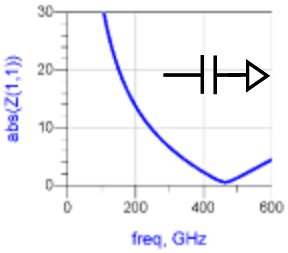
MIM Capacitors



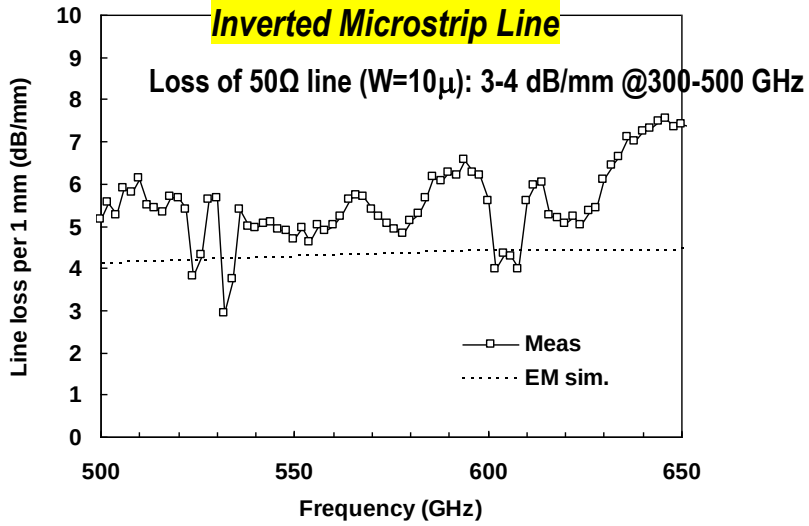




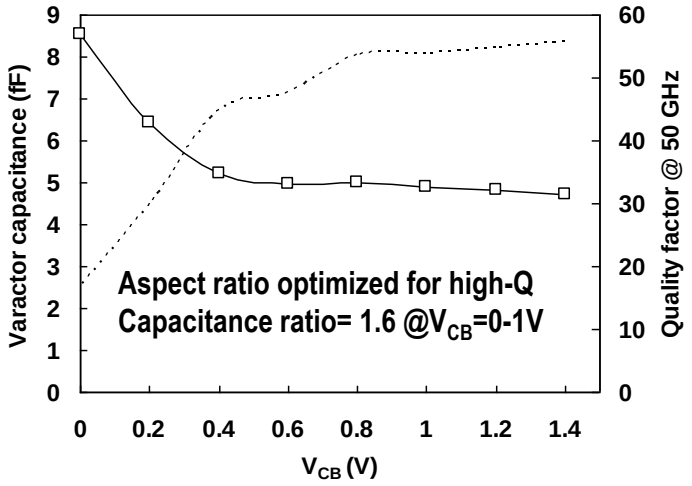




Inverted Microstrip Line



B-C junction varactor



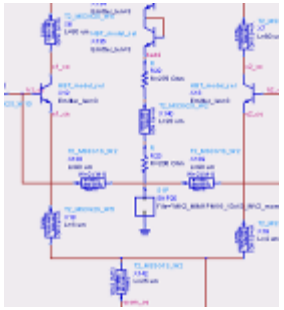
Design Flow

(1) Build passive device library

Transmission lines: (Z_0, β) – compact model from EM sim

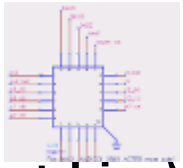
MIM caps, Thin-film resistors: 2-port S-param from EM sim

(2) Initial schematic design using the library



(3) Core circuit layout (i.e. w/o common-mode bias)

(4) EM-sim. → Multi-port S-param



(5) Re-simulation w/ S-param blocks (core + bias)

CKT-EM cycle
~300 GHz: 1~2 cycles
>500 GHz: > 5 cycles

(6) Complete top-level layout w/ bias, interconnects, RF / DC pads, etc.

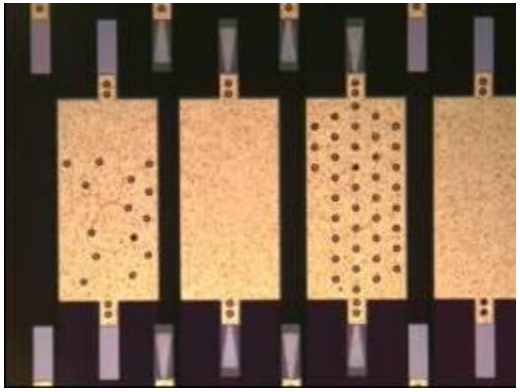
(7) Final Design Verification

DRC (Design-Rule Check)

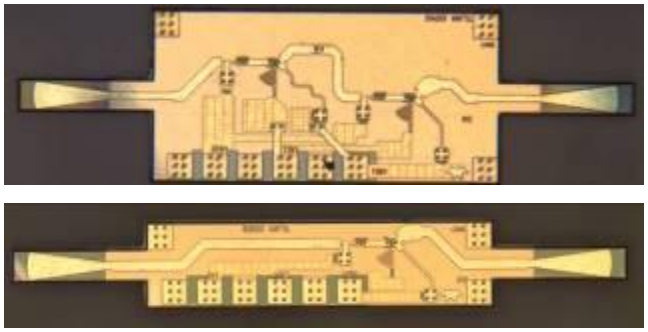
LVS (Layout-versus-Schematic)

Waveguide Packaging of InP Chips

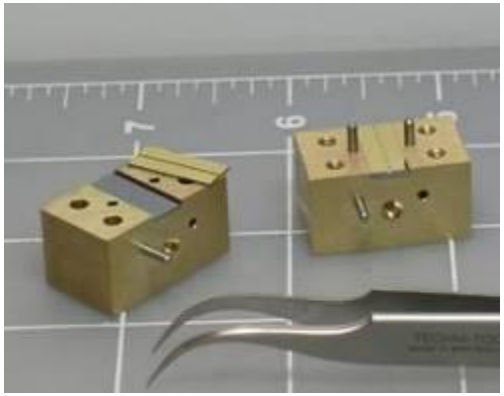
InP chips after backside singulation



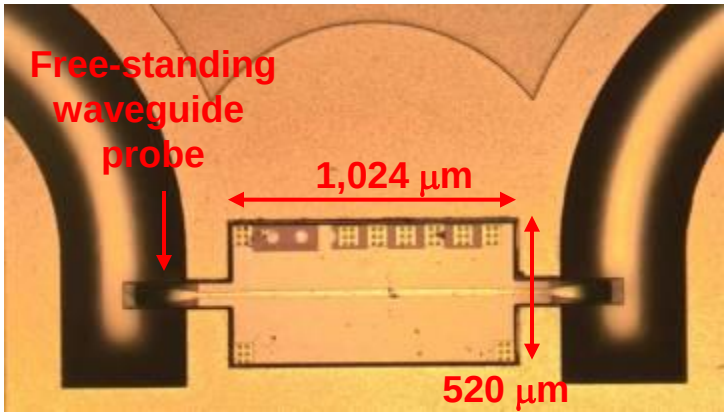
Amplifier ICs after backside release



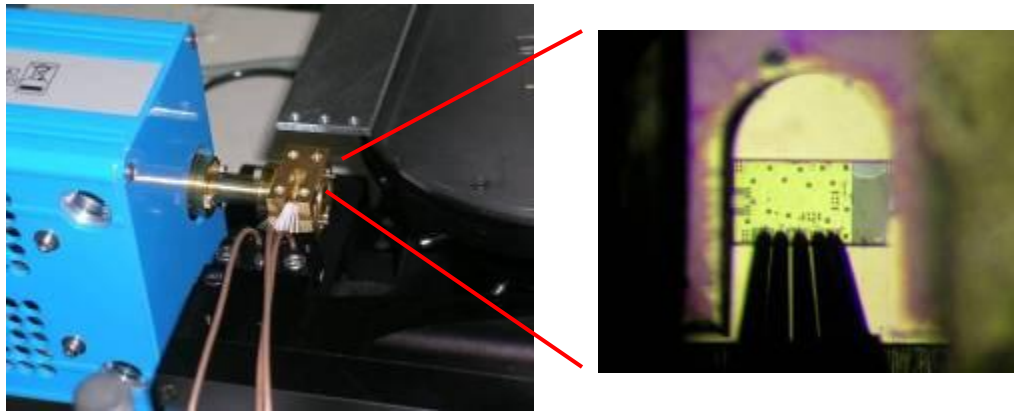
Silicon micromachined waveguide



THRU-line test chip in a silicon WG block



300 GHz oscillator in W/G block under test

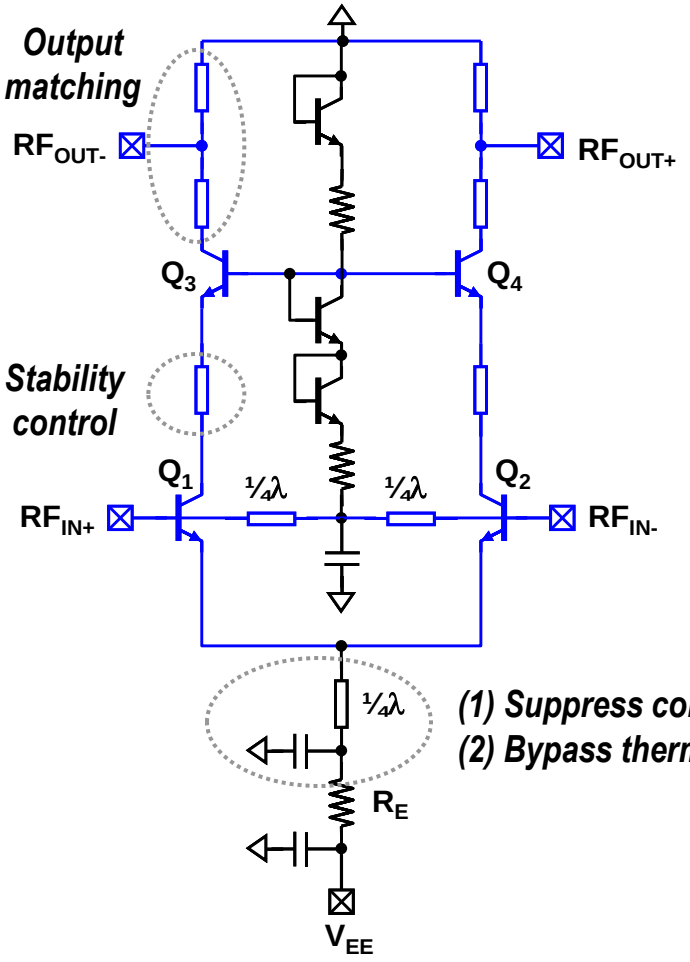


- Through-wafer vias, wafer thinning → backside metallization → dry etch chip singulation → mount in silicon micromachined waveguide block
- WR3 THRU test chip: < 4 dB measured insertion loss @300 GHz, < 1 dB per transition

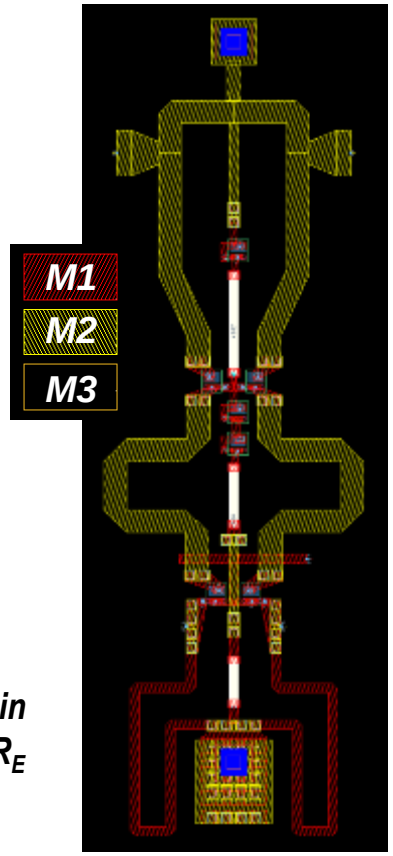
Design of 300 GHz Building Blocks

- *350 GHz Differential LNA*
- *300 GHz Differential Oscillator*
- *300 GHz Dynamic Frequency Divider*

350 GHz Differential Cascode Amplifier



(1) Suppress common-mode gain
(2) Bypass thermal noise from R_E



Size: 60×180 μm²

Layout / EM model

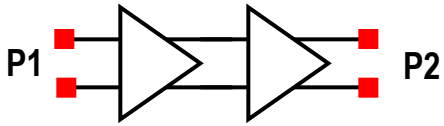
Inverted-Microstrip (Continuous M3 ground plane)

Total 21 ports (16 device, 4 RF, 1 bias) → 21-port S-parameter

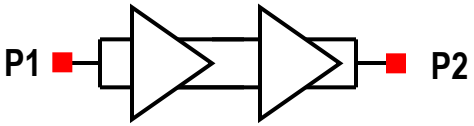
- **Topology: Differential Cascode**
- **RF operation in diff. mode (blue line), DC biasing in common mode (black line)**
- **Make sure no common-mode oscillation (dc-f_{max})**

350 GHz Differential Cascode Amplifier

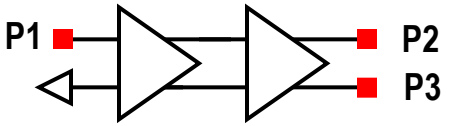
'Differential' (DIFF) Mode



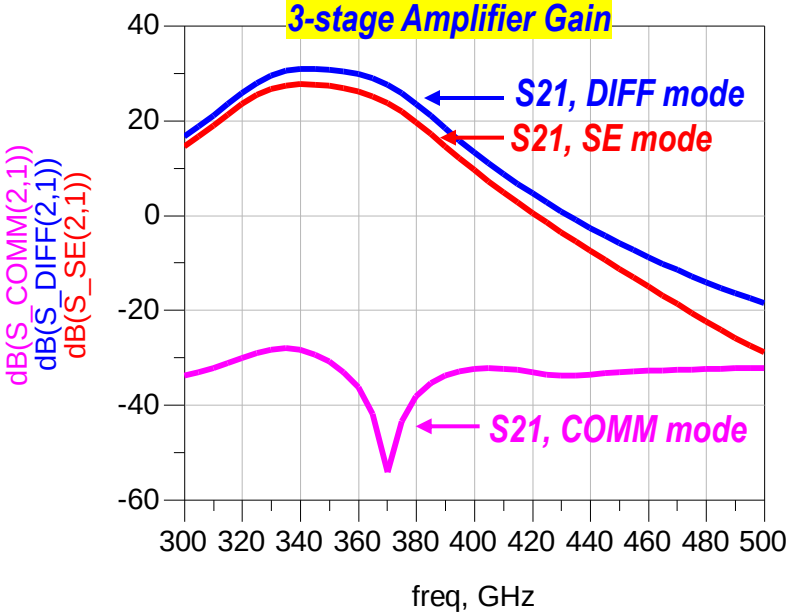
'Common' (COMM) Mode



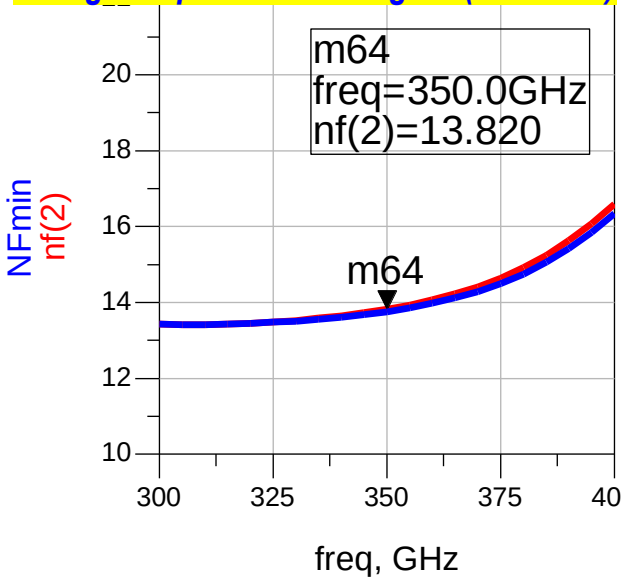
'Single-Ended' (SE) Mode



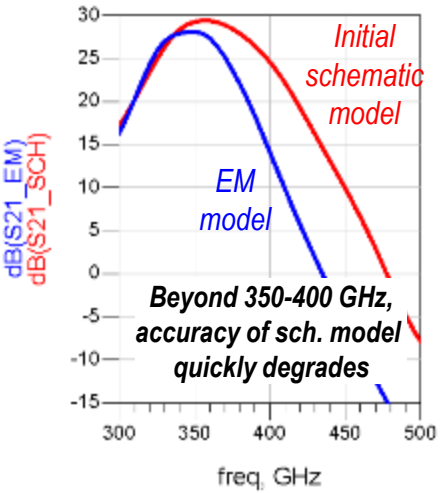
3-stage Amplifier Gain



3-stage Amplifier Noise Figure (SE mode)



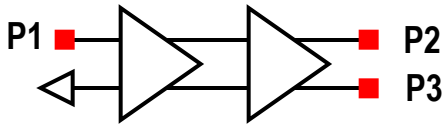
SCH. Vs EM model



- **Three modes of operation of interest: *DIFF, COMM, SE* modes**
- **If *DIFF* gain is sufficiently higher than *COMM*-mode gain, *SE*-mode performance approaches *DIFF*-mode**
  - **i.e. input common-mode will diminish, yielding $|S_{21,SE}|_{dB} \approx |S_{31,SE}|_{dB} \approx |S_{21,DIFF}|_{dB}$ -3dB, $NF_{SE} \approx NF_{DIFF}$.**
  - ***SE* mode operation (1) facilitates testing, and (2) obviates lossy input balun, thus most useful in the receiver front-end.**
- **$S_{21,diff}$ = 10 dB/stage, noise figure = 13.8 dB @ P_{DC}=50 mW/stage**
- **Amplifier must be stable in all three modes.**

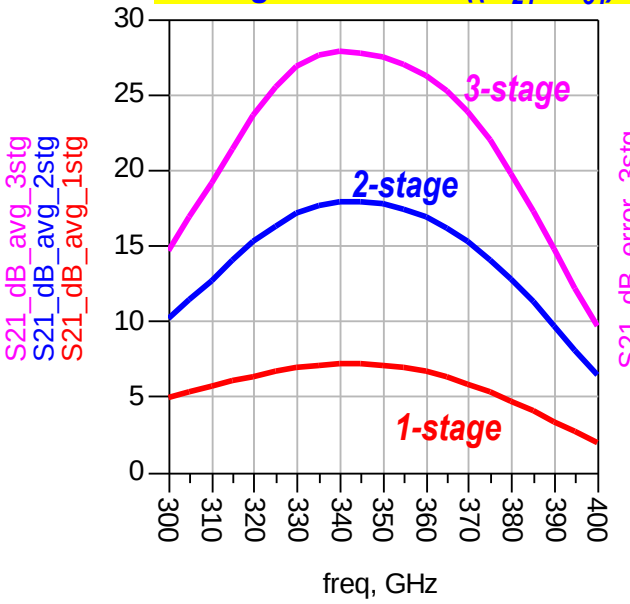
SE Mode Operation: What About Output Balance?

'Single-Ended' (SE) Mode

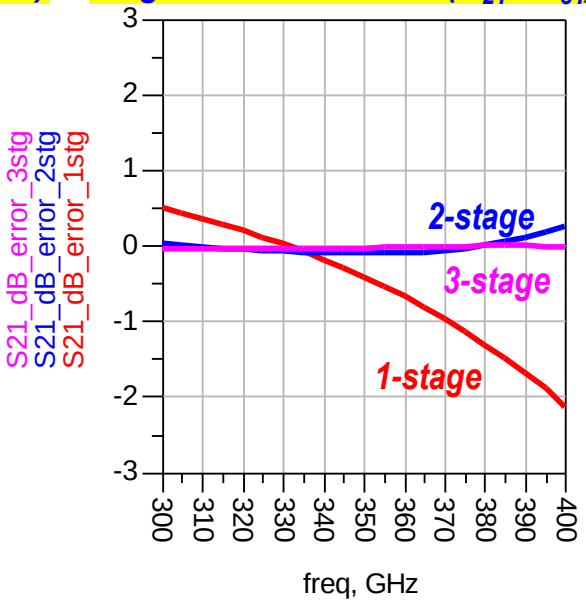


Question: In SE mode, are the amplifier outputs (P2,P3) well balanced?

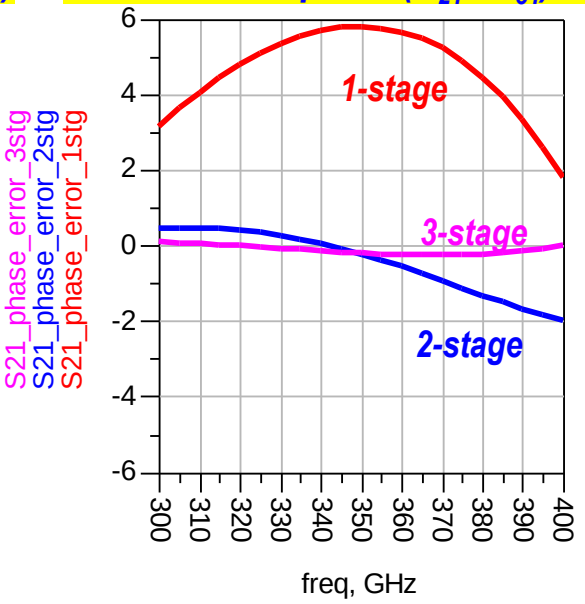
Average Gain = dB((S21+S31)/2)



Magnitude Error = dB(S21 / S31)

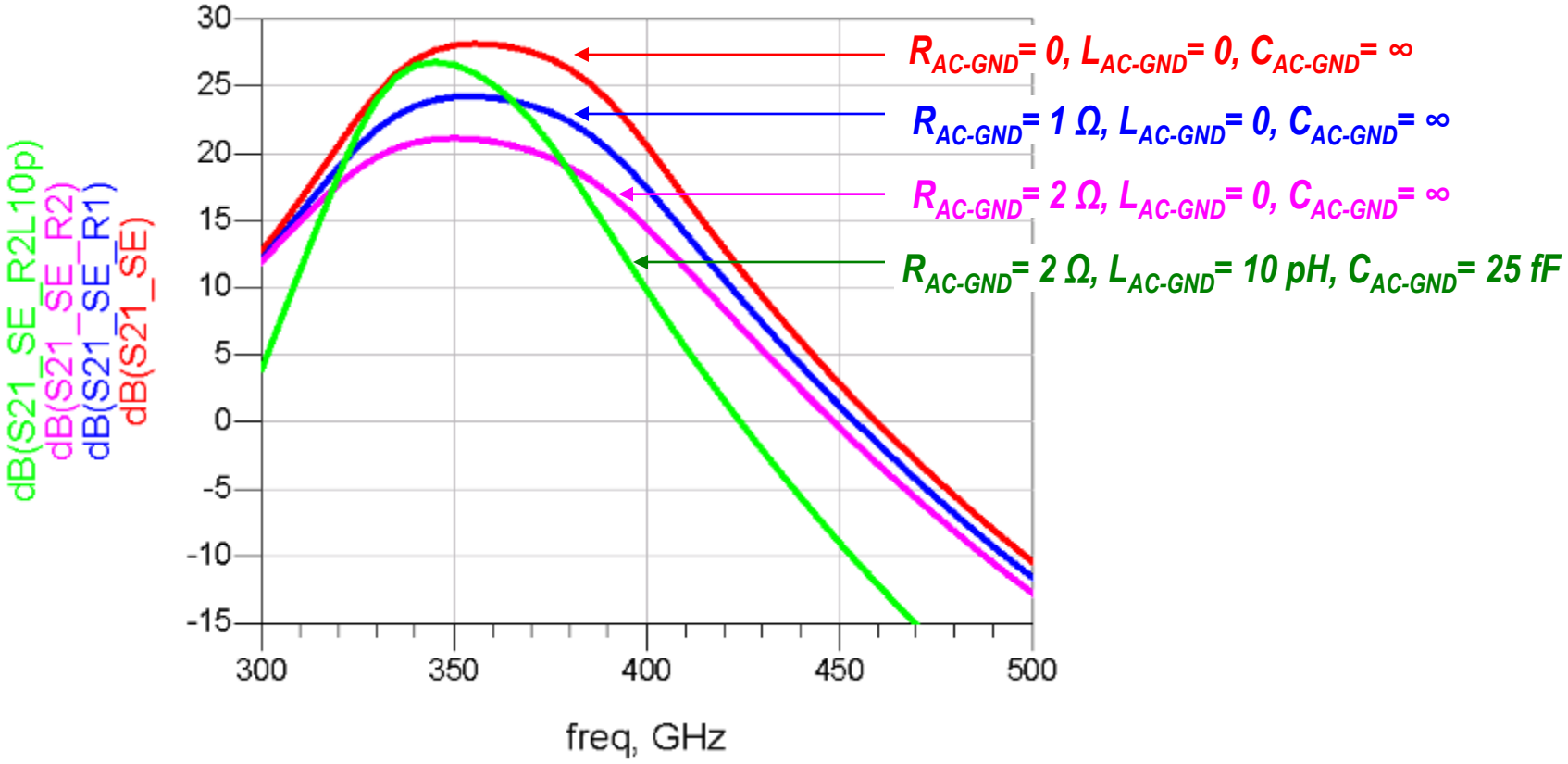


Phase Error = phase(S21 / S31)-180



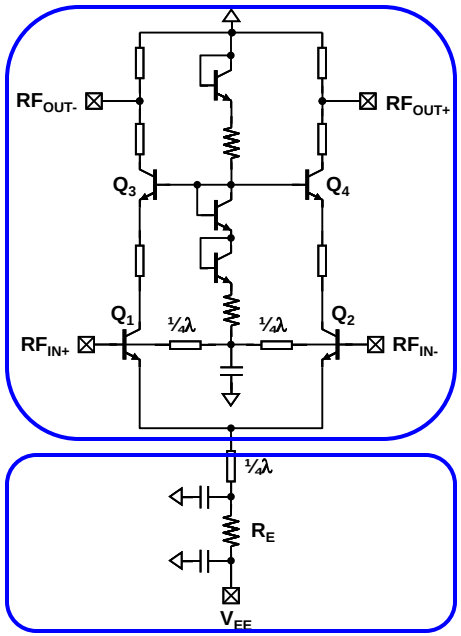
- **For a 3-stage differential configuration, amplitude and phase imbalances are less than 0.1 dB and 0.5 deg, respectively.**

Effects of AC-ground Impedance: Single-Ended Amplifier Example



- Amplifier in a single-ended topology, but otherwise, equivalent to the previous 3-stage differential 350 GHz design (e.g. same matching network, same bias)
- Effects of AC-ground resistance / inductance are clearly seen: Even $R_{AC\text{-}GND}$ = 1 Ω degrades circuit gain by 4-5 dB (= 1.5 dB reduction per stage).
- $L_{AC\text{-}GND}$ = 10 pH reduces amplifier 3-dB bandwidth by half !!

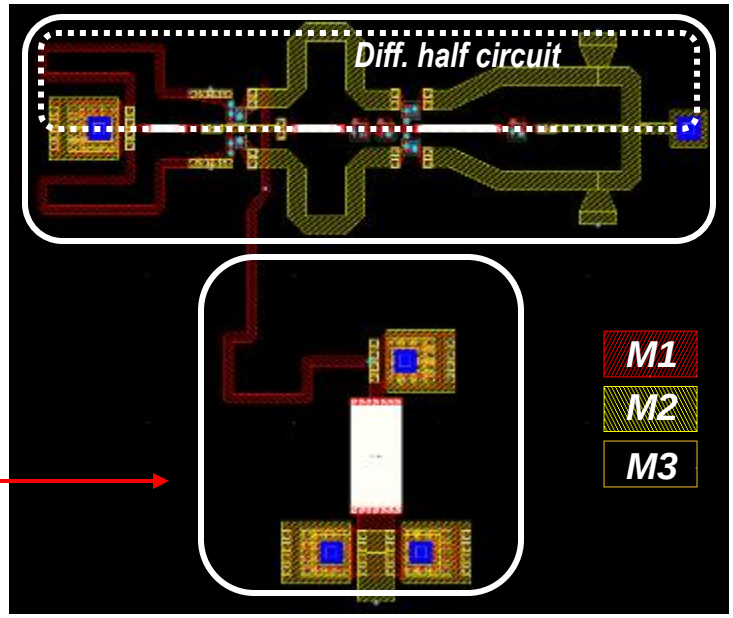
350 GHz Differential Cascode Amplifier: Layout & Hierarchy



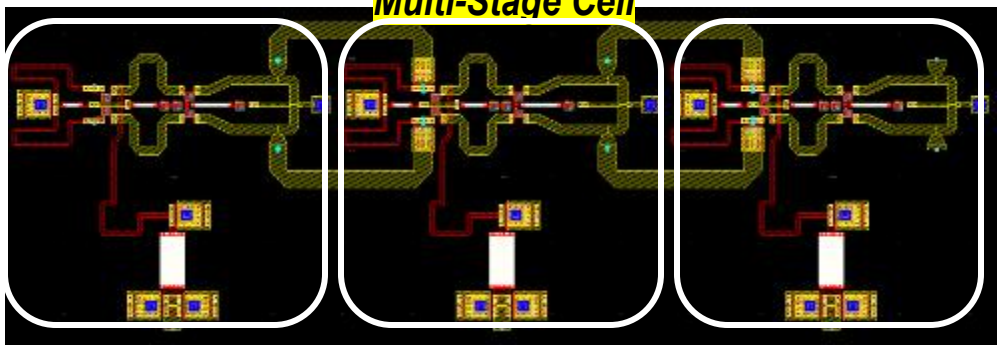
Single-stage cell

Core circuit block
(mostly diff.)
→ Full EM model
(multi-port S-param)

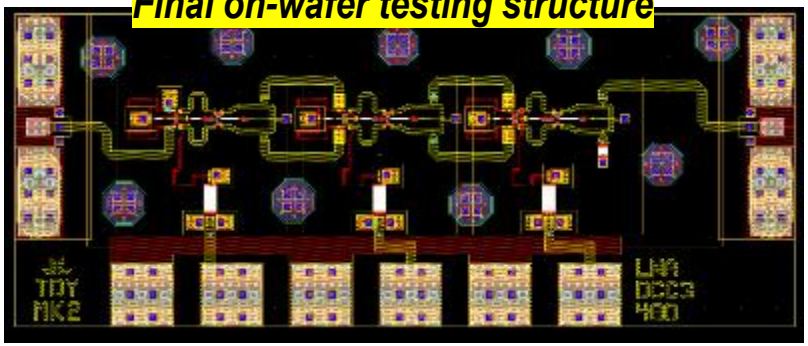
Bias circuitry (SE)
→ EM or compact model



Multi-Stage Cell



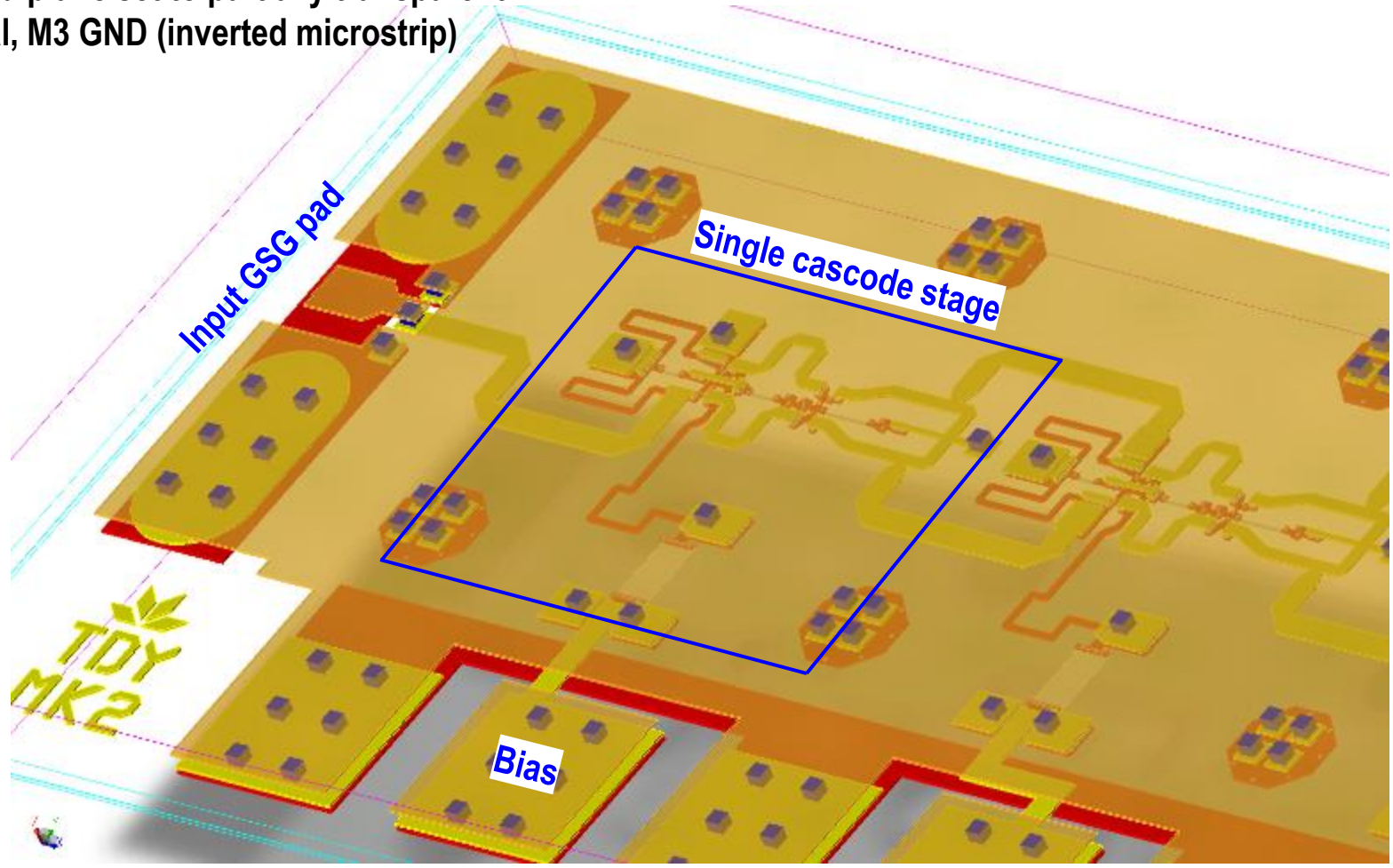
Final on-wafer testing structure



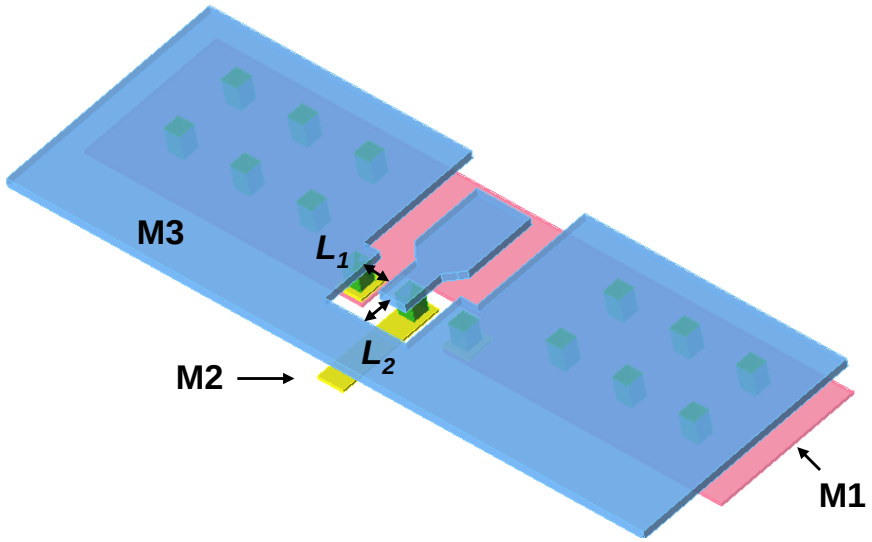
- General layout hierarchy: core_half → core → single_stage → multi_stage → top_cell
- Note M3 top ground plane covers entire circuit.

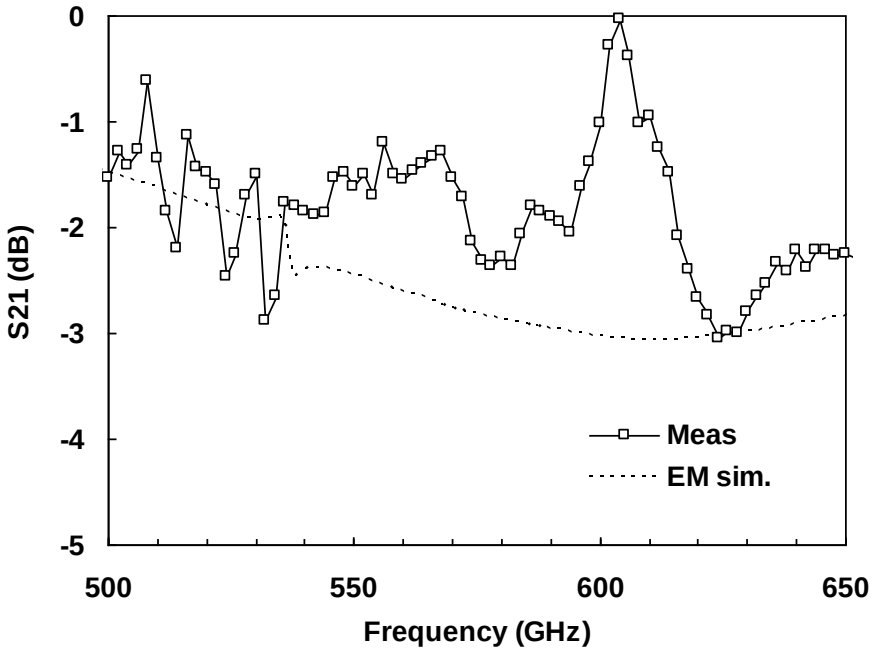
3-D Top View

Top M3 ground plane set to partially transparent
M1 / M2 Signal, M3 GND (inverted microstrip)



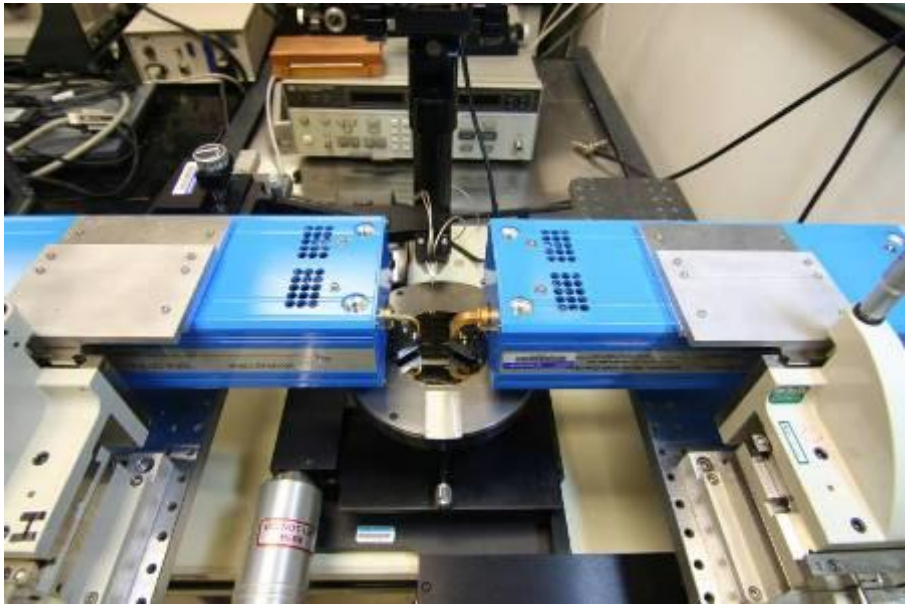
Inverted MSL-to-Pad Transition



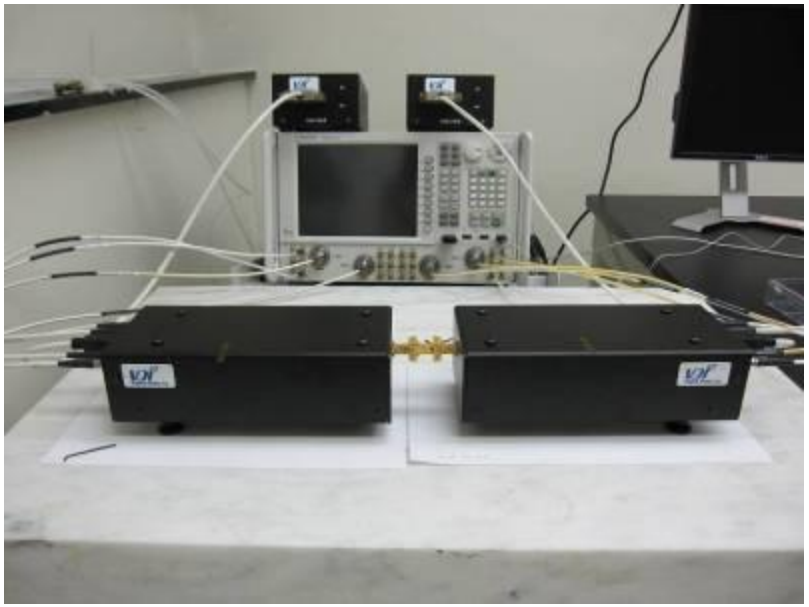


- On-wafer testing of inverted-MSL-based circuits requires a transition to a co-planar GSG pad.
- Distance from M3 GND plane to signal pad (L_1, L_2) was adjusted for broadband low-loss transition.
- Simulated S_{21}= -0.5dB @300 GHz, -1.4dB @550 GHz (S_{11} < -12 dB)

2-port Vector Network Analyzer (VNA) Setup



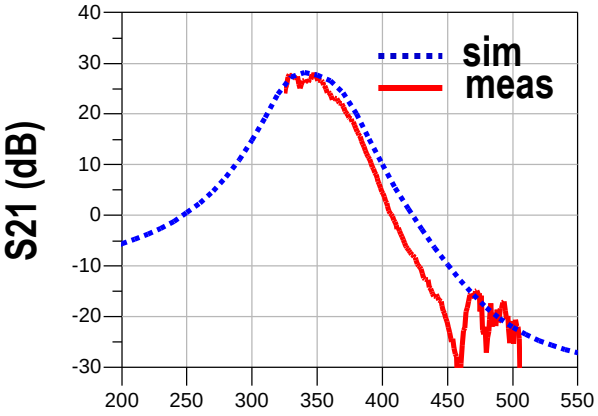
- 220-325 GHz (WR3) OML VNA Extenders
- Interfaced with HP8510C

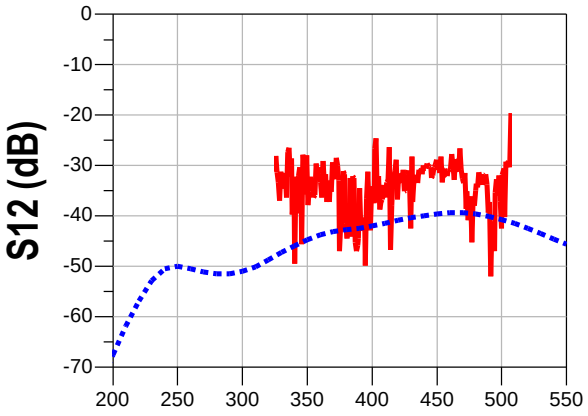


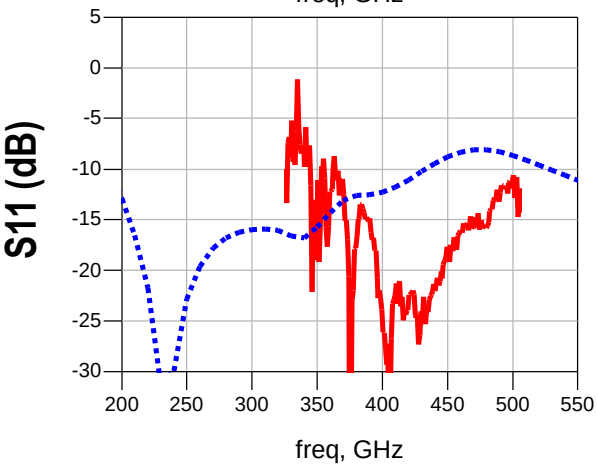
- 500-750 GHz (WR1.5) VDI VNA Extenders
- Interfaced with Agilent PNA-X

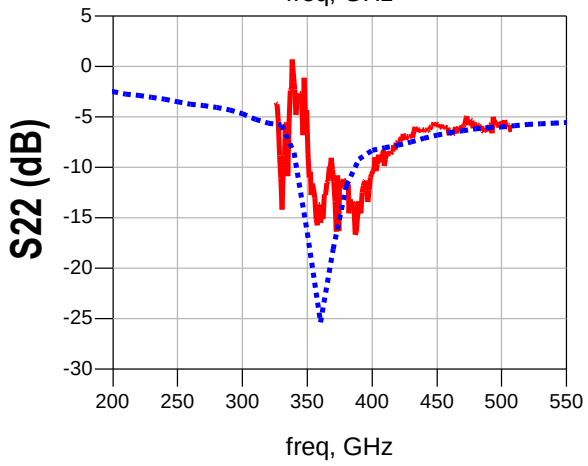
- mm-wave extenders interface with main VNA module via IF / LO
- VNA setup for 325-500 GHz (WR2.2) band available at JPL
- A VNA extender can also be used as a Up/Down conversion harmonic mixer
  - —e.g. oscillator frequency measurement (Watch out for image responses!!)

350 GHz 3-Stage Differential Cascode Amplifier: Measurement Results

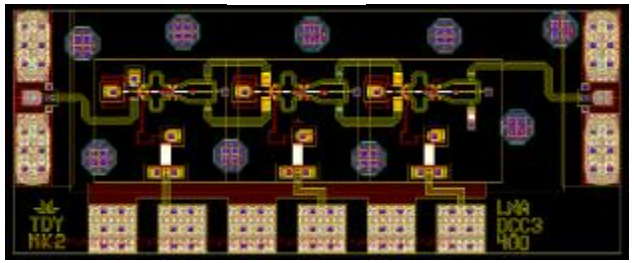




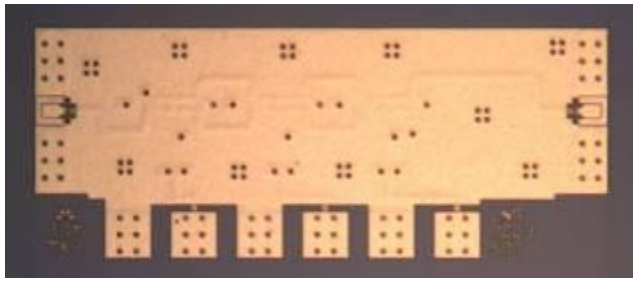




Layout



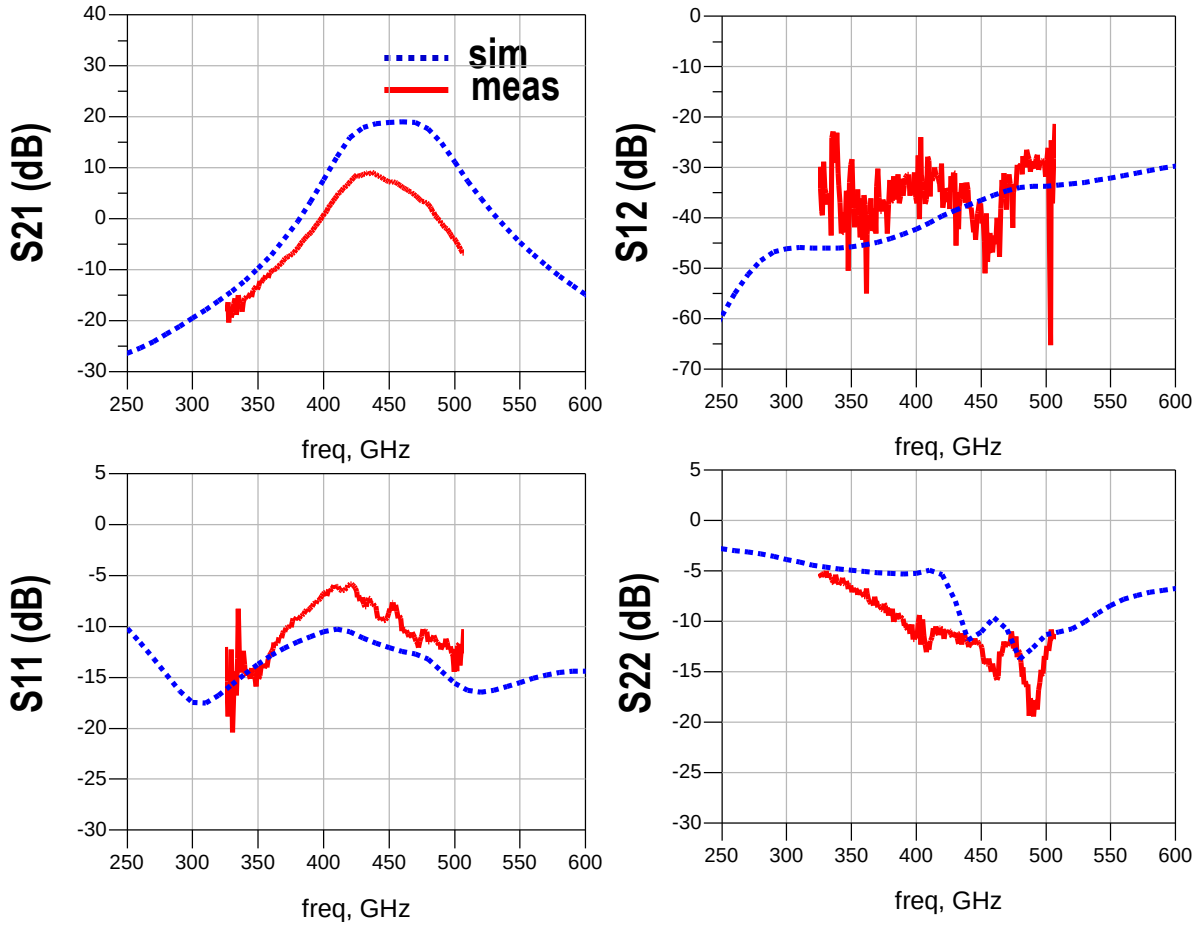
Chip photograph



Size: 870×350 μm²

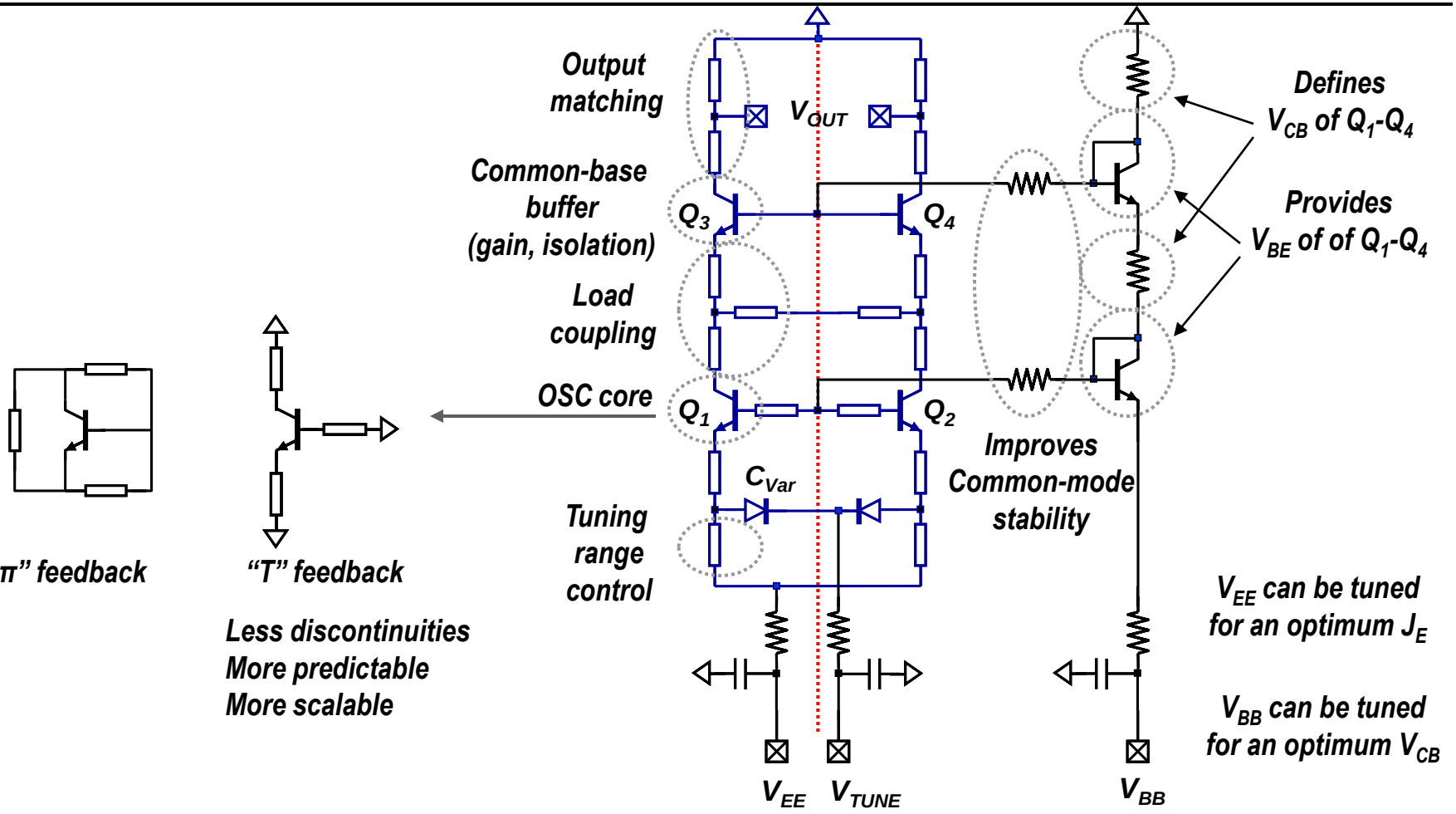
- **Peak $S_{21,SE}$ = 27 dB @350 GHz, @ P_{DC}=150 mW**
- **Testing in 2-port *SE* mode, with unused output port (P3) terminated on-chip.**
- **Noise figure of receiver chain (3-stage LNA + down-mixer) was measured to be 13 dB (will be shown later)**

450 GHz 3-Stage Differential Cascode Amplifier: Measurement Results



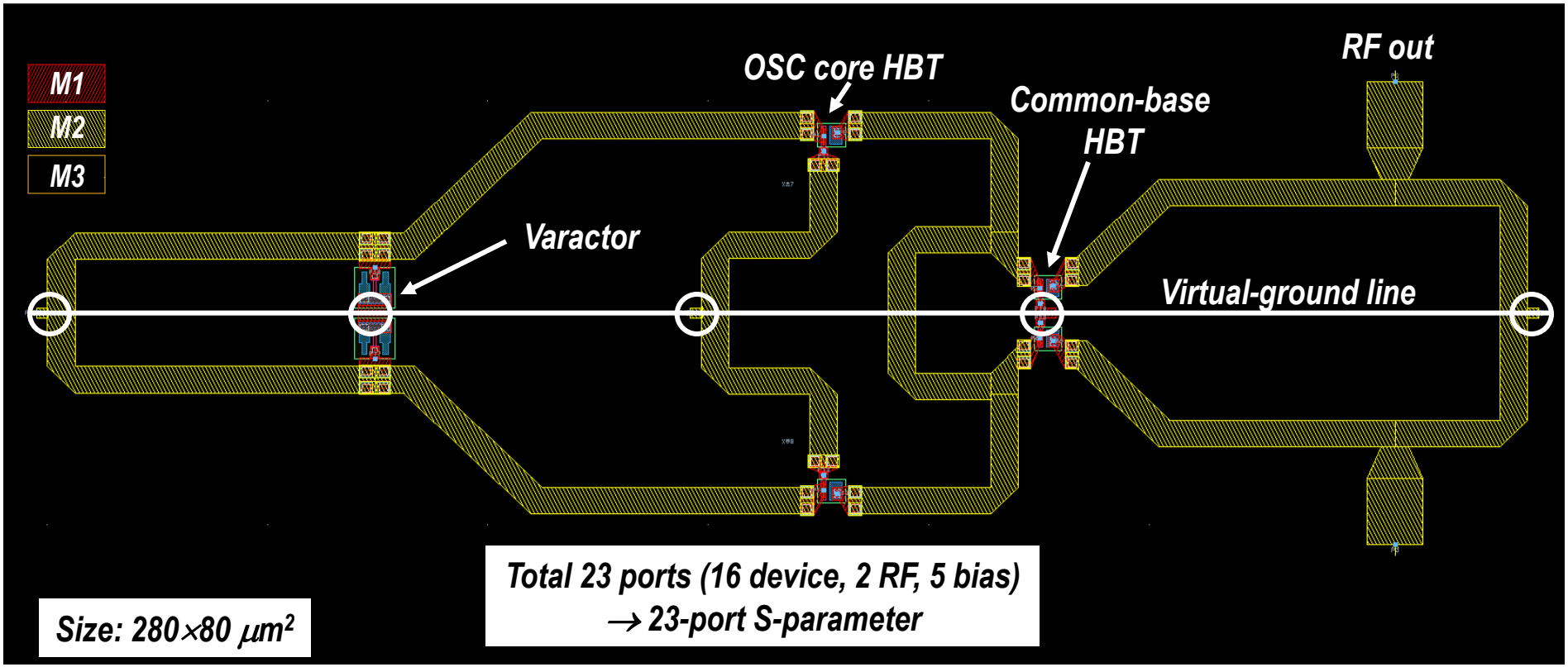
- Peak $S_{21,SE}$ = 9 dB @440 GHz, @ P_{DC}=150 mW
- Testing in 2-port *SE* mode, with unused output port (P3) terminated on-chip.

300 GHz Oscillator: Schematic

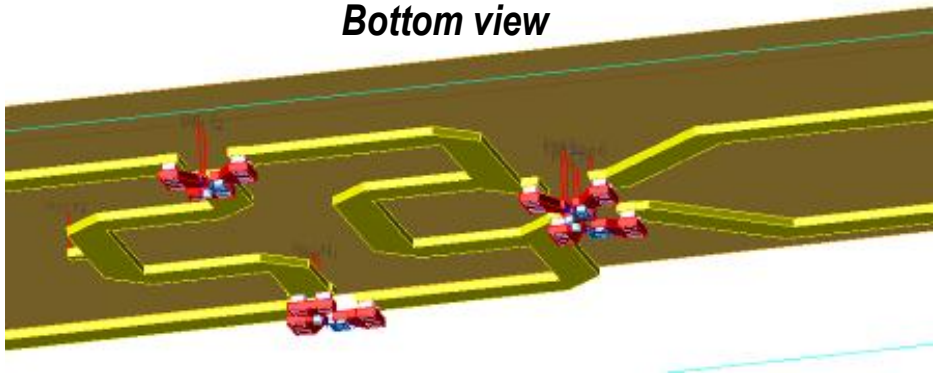


- Topology: Differential series-tuned oscillator w/ stacked common-base buffer
  - — Fixed-frequency designs (FFO) and voltage-controlled designs (VCO)
- RF operation in diff. mode (blue line), DC biasing in common mode (black line)
- Make sure no common-mode oscillation (dc-f_{max})

300 GHz VCO: Core Layout / *EM* Model



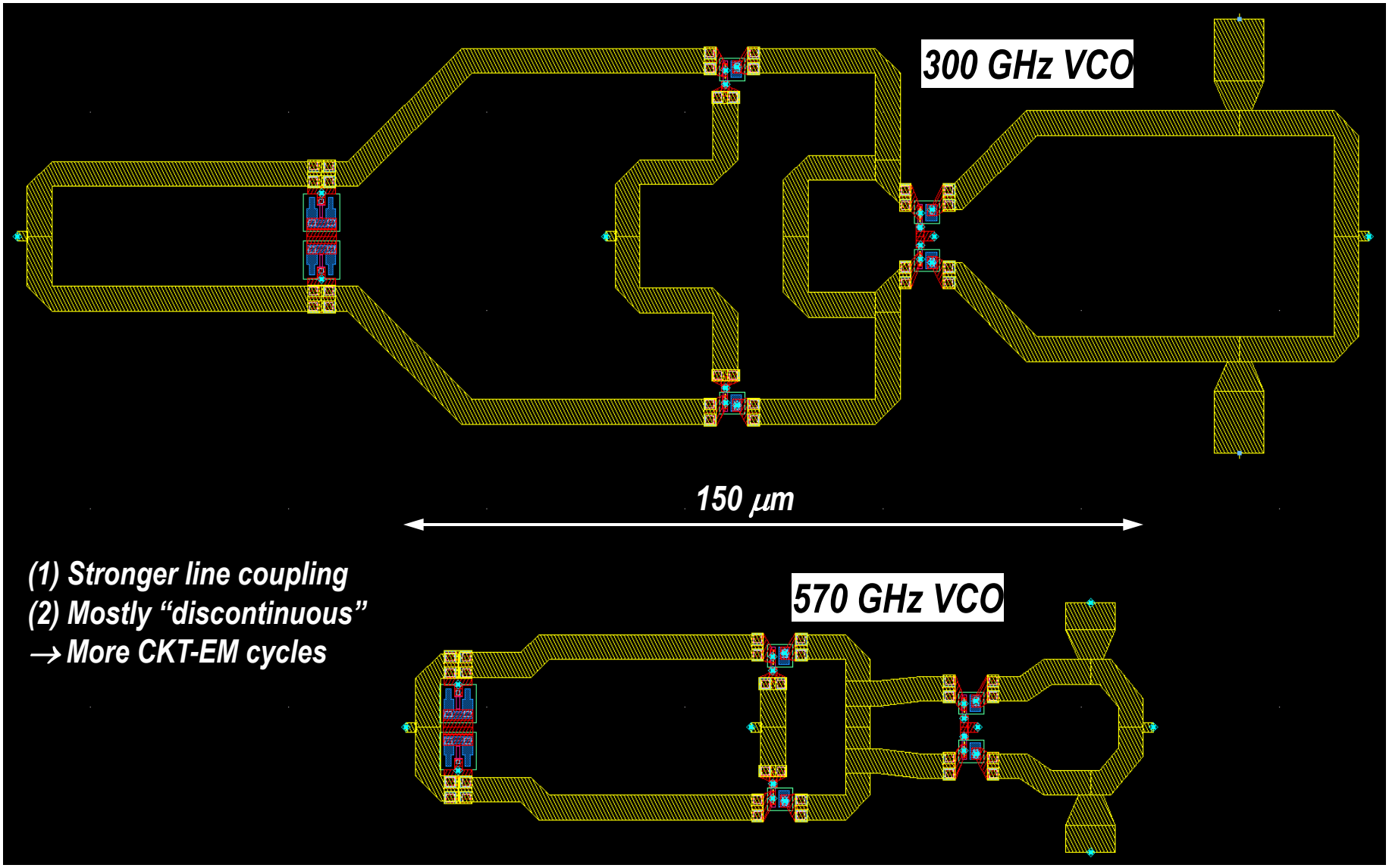
Bottom view



Inverted-Microstrip: M1/M2 Signal, M3 GND

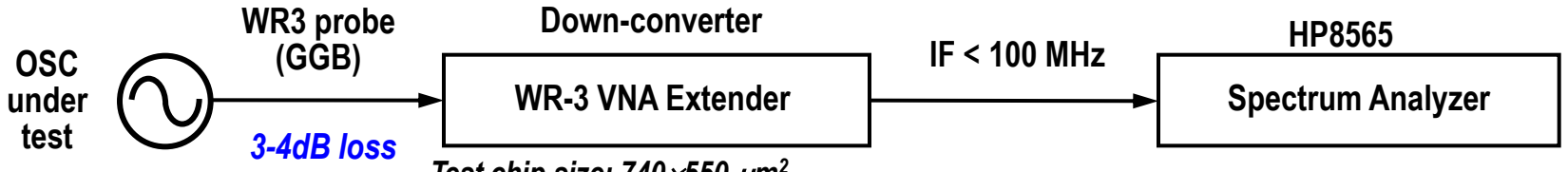
Line width= 5μm (except for 50Ω output line)

Layout: 300 GHz versus 570 GHz

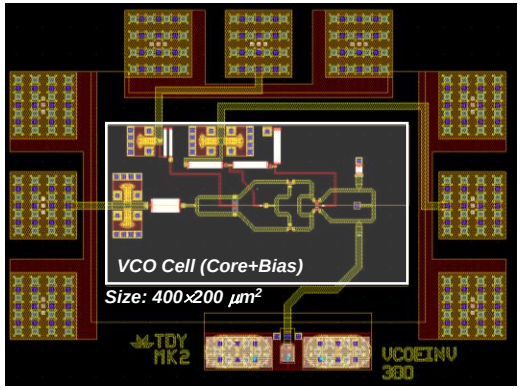


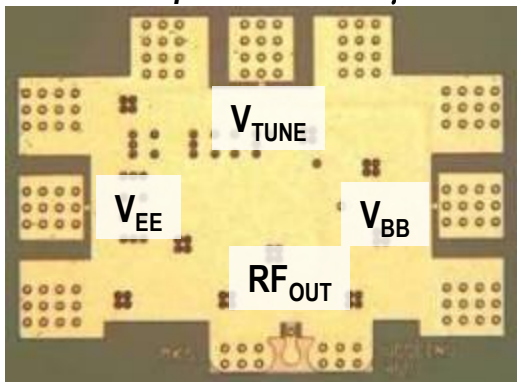
(1) Stronger line coupling
(2) Mostly "discontinuous"
→ More CKT-EM cycles

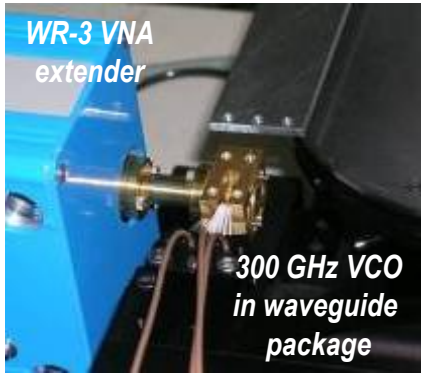
Freq. Testing with an External Mixer



Test chip size: 740×550 μm²



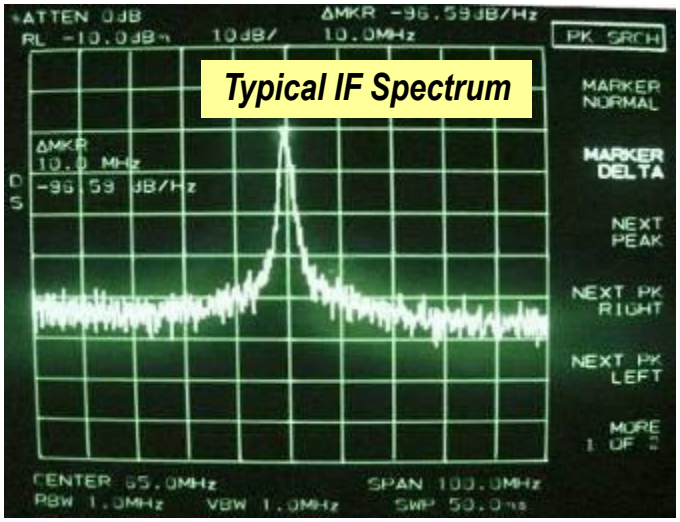


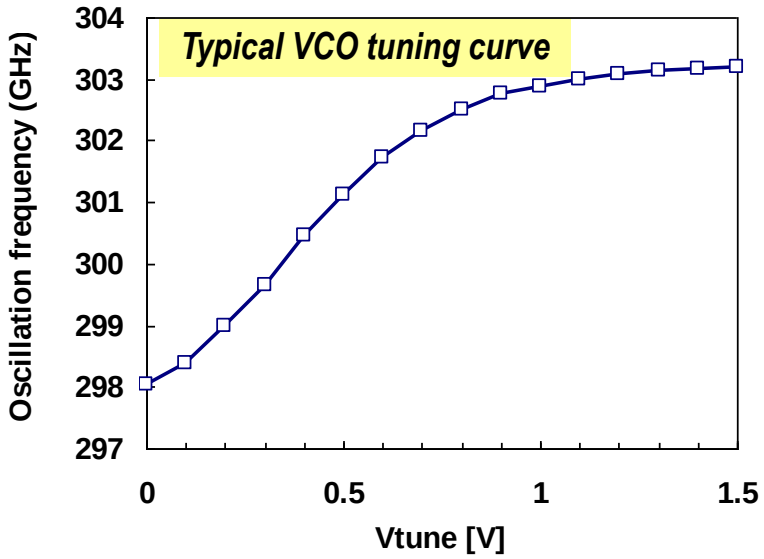


HBT J_E = 7-10 mA/μm2

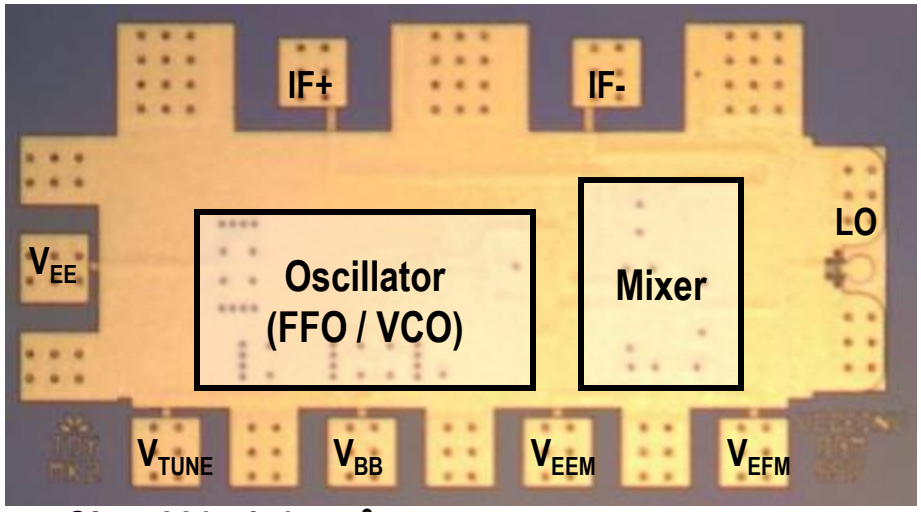
P_{DC}= 70-110 mW

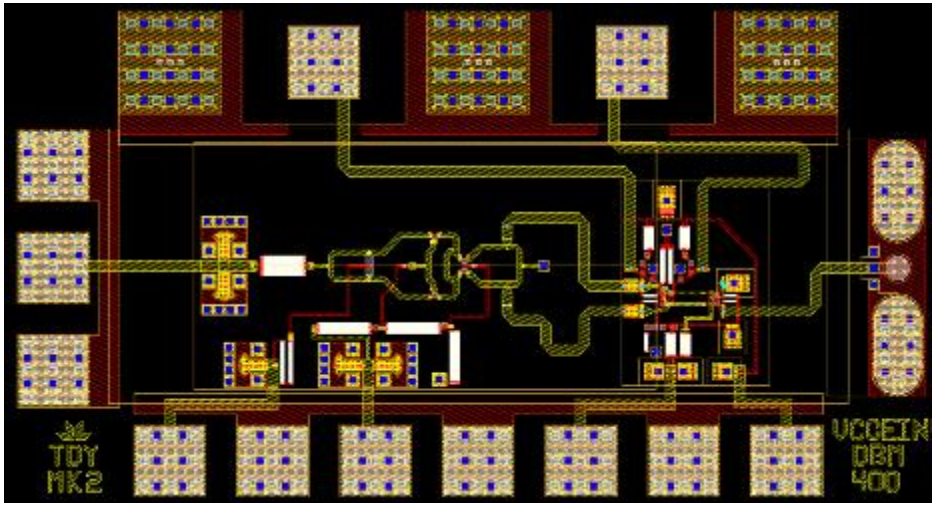
Fixed-frequency & voltage-controlled designs from 250 to > 600 GHz



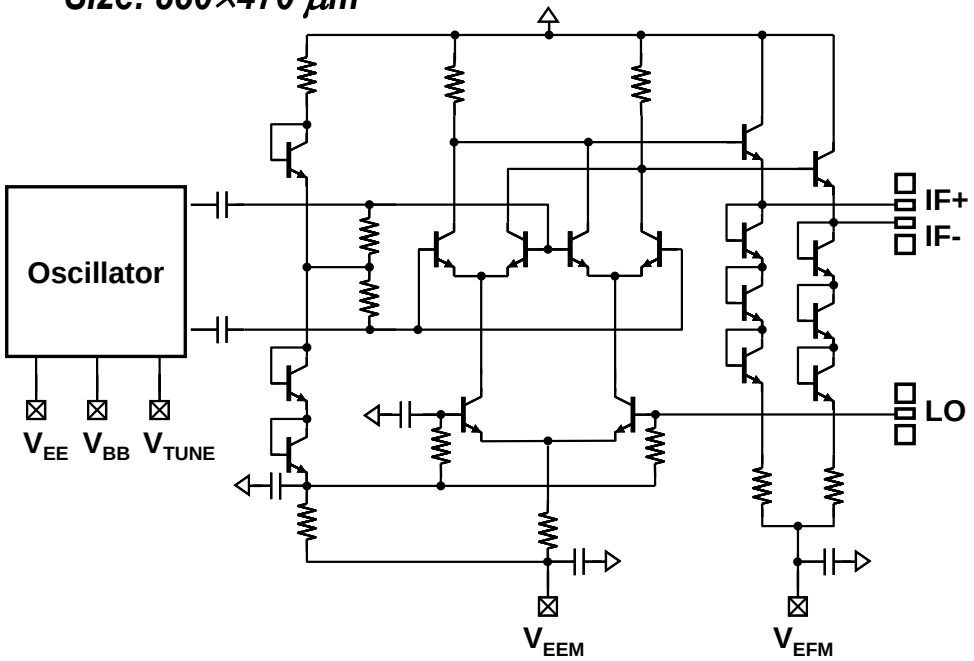


OSC Freq. Testing: Integrated OSC+MIX



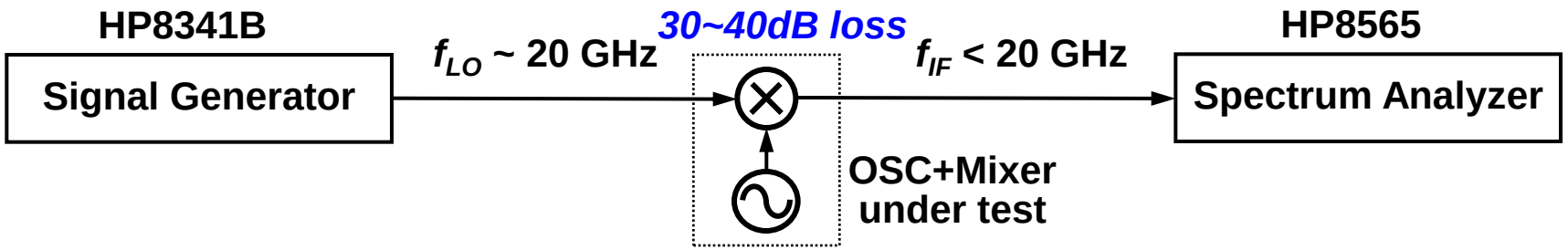


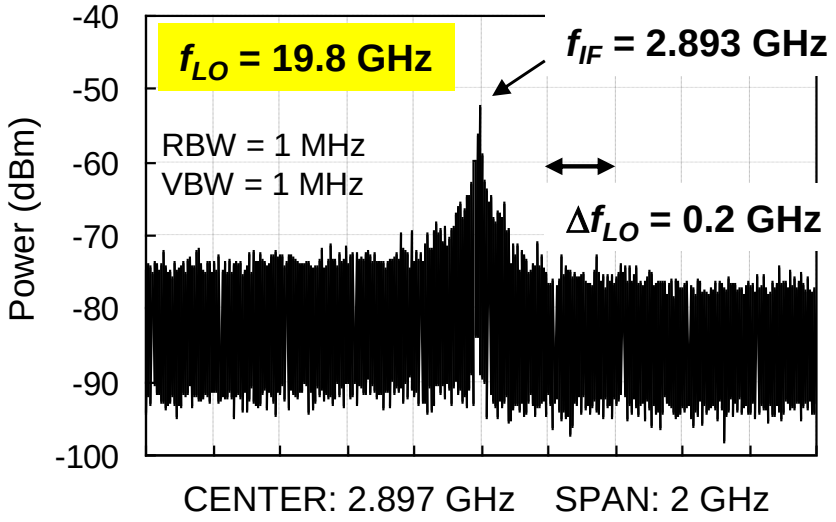
Size: 880×470 μm^2

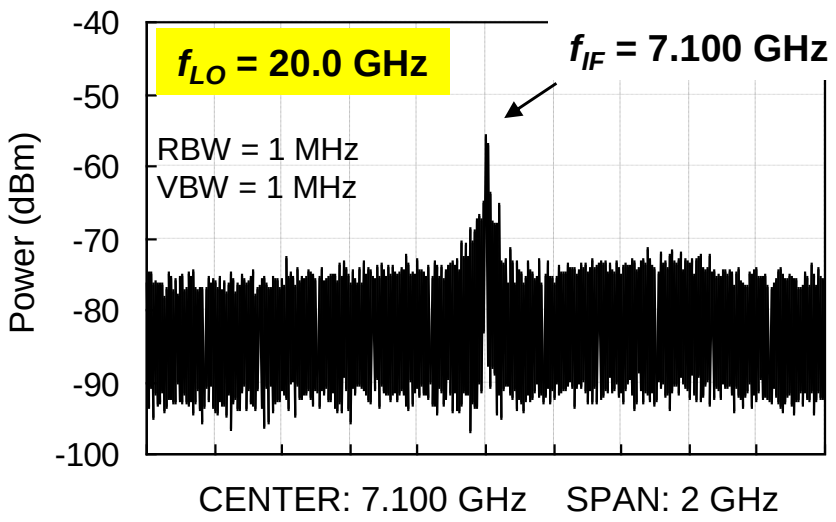


- Integrated mixer facilitates spectrum measurement.
  - — *No > 300 GHz mm-wave interface*
- Sub-harmonic operation
  - — f_{LO} ~ 20 GHz (BW_{IF} > 25 GHz)
  - — *N*=21-31 for 400-600 GHz RF input
  - — Conv. Loss = 30-40 dB
- Mixer consumes 60 mW.

OSC Freq. Testing: Integrated OSC+MIX







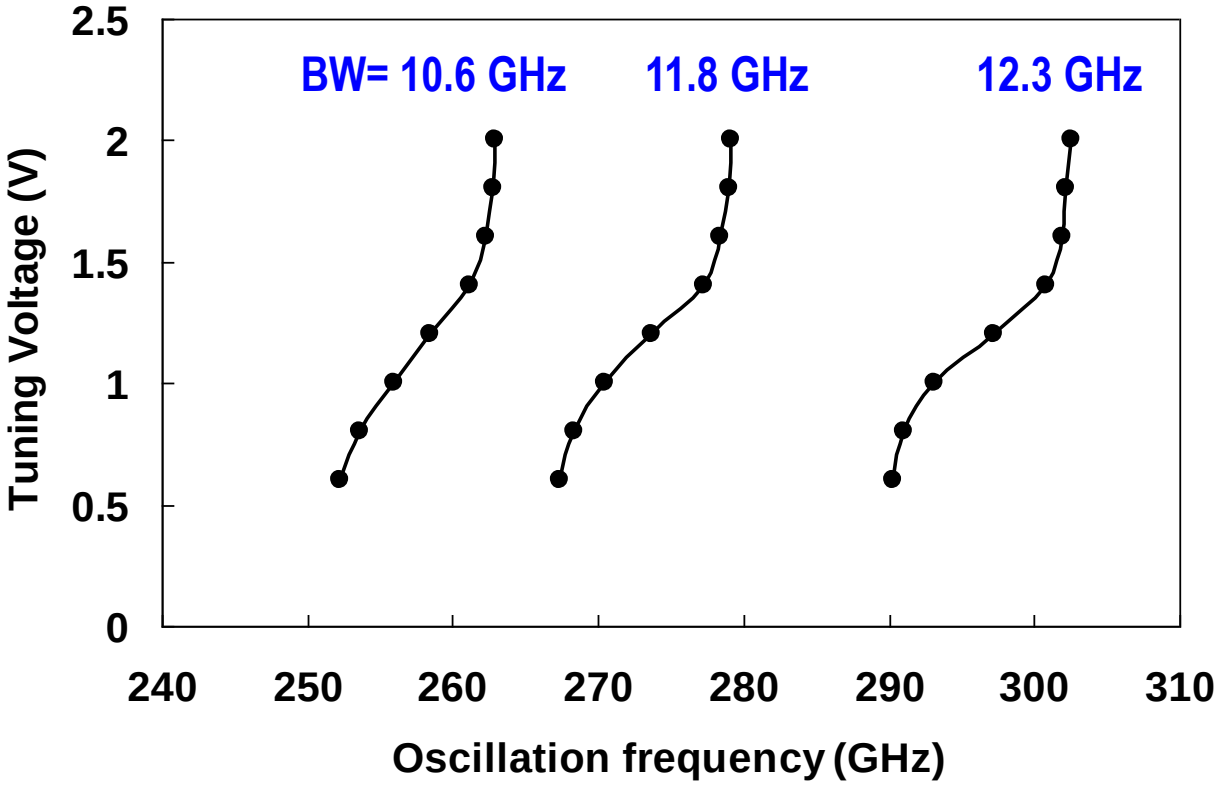
$$f_{IF} = |Nf_{LO} - f_{OSC}|$$

$$\frac{\Delta f_{IF}}{\Delta f_{LO}} > 0 \longrightarrow f_{IF} = Nf_{LO} - f_{OSC}$$

$$N = \text{Round}\left[\left|\frac{\Delta f_{IF}}{\Delta f_{LO}}\right|\right] = \text{Round}\left[\left|\frac{7.1 - 2.893}{0.2}\right|\right] = \text{Round}[21.035] = 21$$

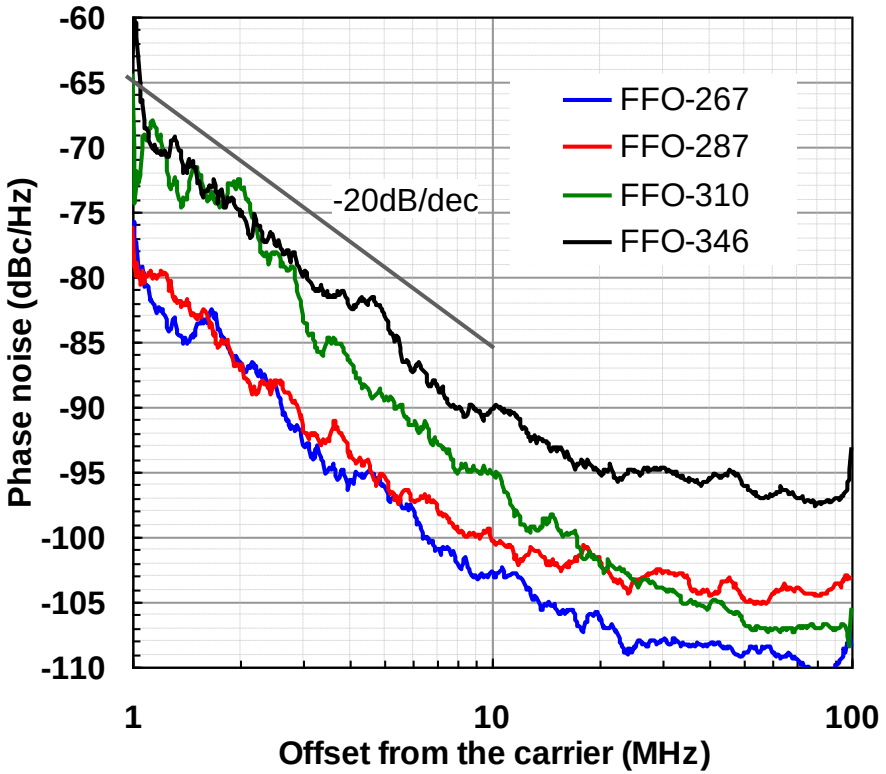
Small

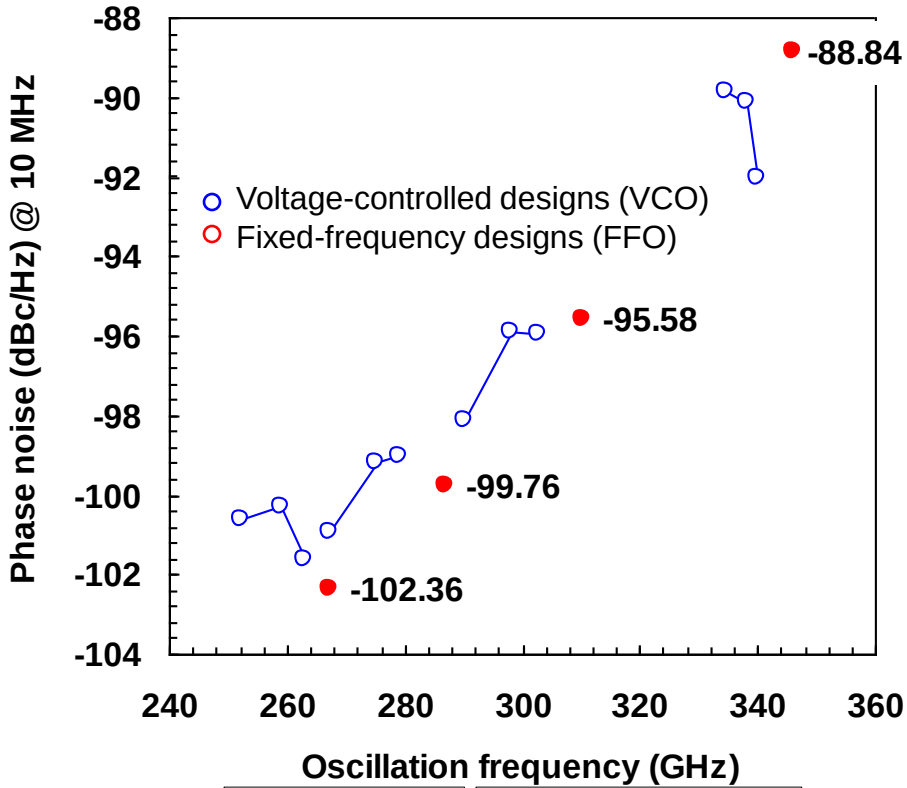
300 GHz VCO Tuning Bandwidth



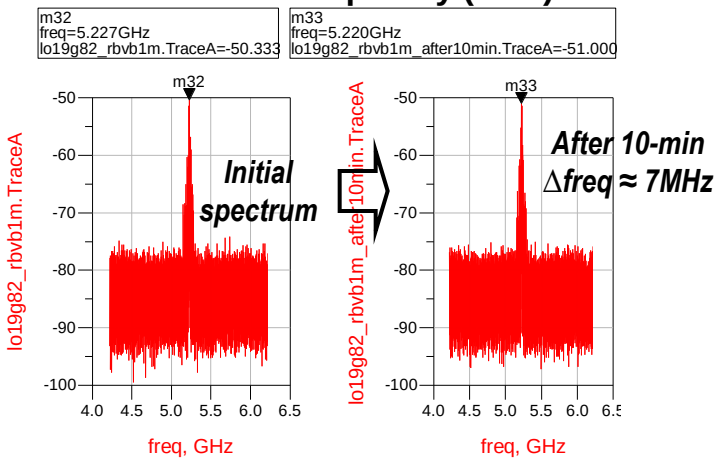
- **Theoretical max. tuning range =** $\sqrt{C_{RATIO}} = \sqrt{1.4} \approx 1.2\,(20\%)$
- **Varactors lightly coupled (Q_{VAR}~8, Q_{TL}~25)**

Measured Phase Noise



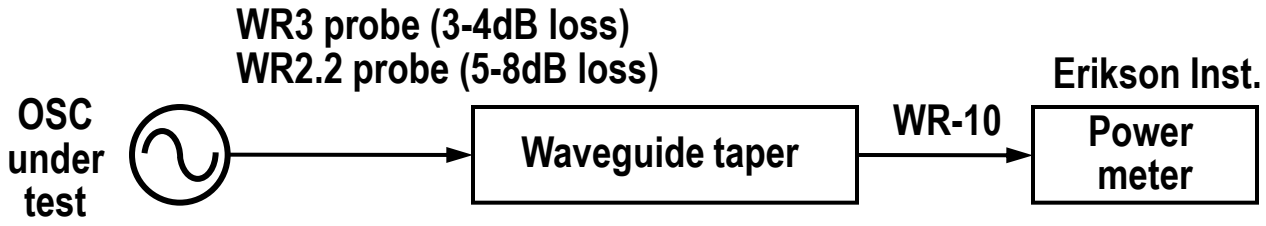


- Approximately follow -20 dB/dec curve
  - —1/f noise corner < 1 MHz
- IF noise floor limits measurement for offsets > 20 MHz
- Drifts in oscillation frequency must be minimized for accurate phase noise testing
  - — Stable, low-noise power supplies



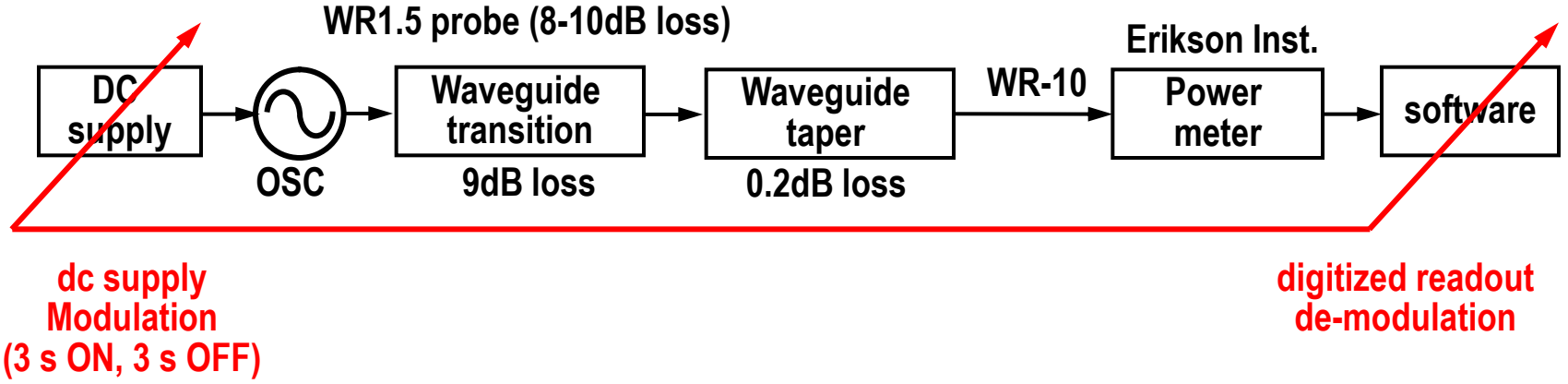
Oscillator Power Testing

WR3 (220-330G)
WR2.2 (330-500G)



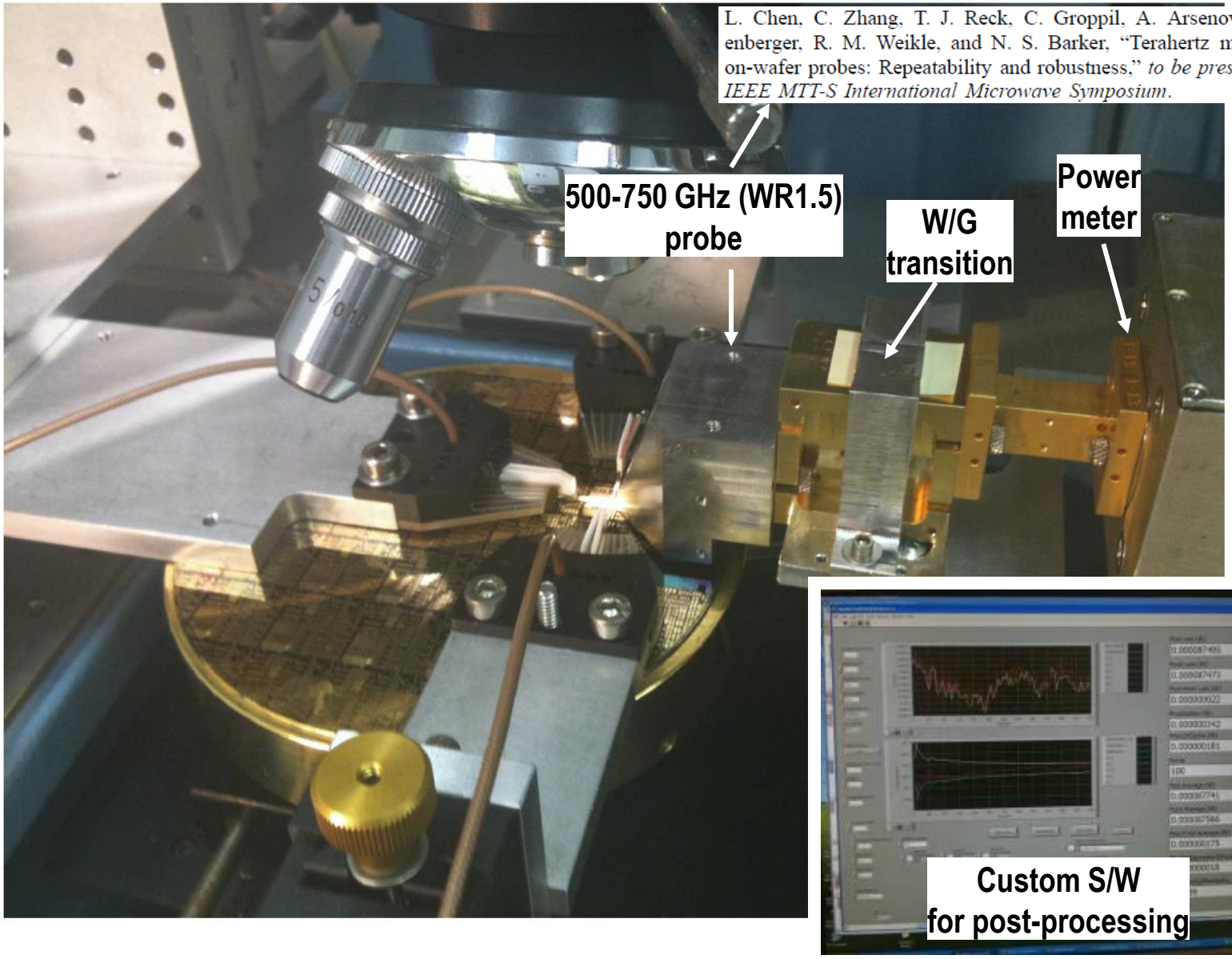
WR1.5 (500-750G)

Problem: Tiny raw power → Lowest full-scale → Long settling time → Subject to drift
Solution: Modulated sensing



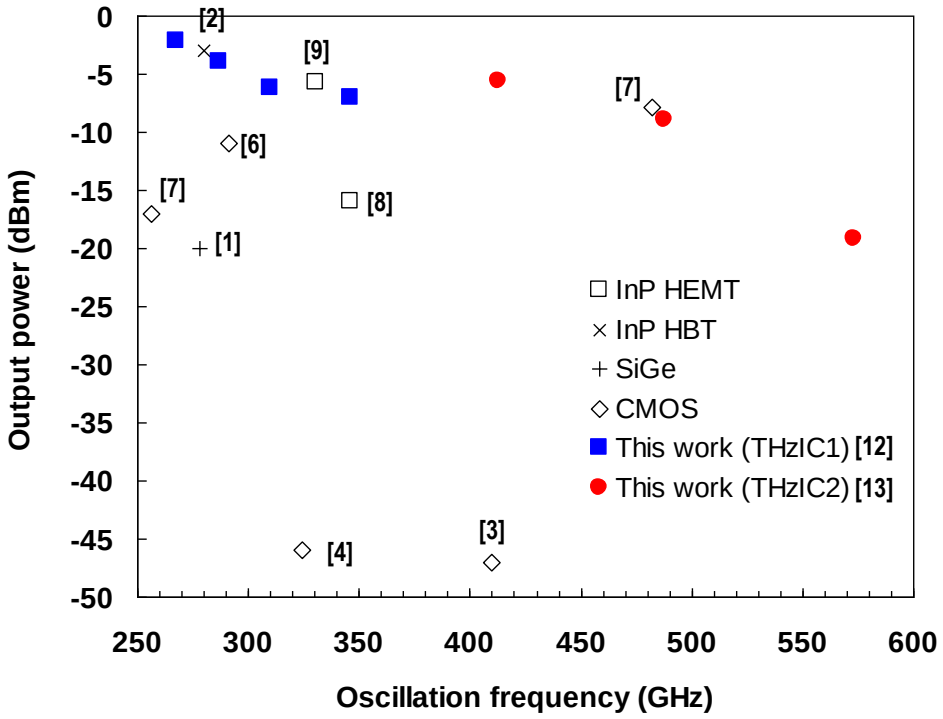
WR-1.5 Power Testing Setup (JPL)

L. Chen, C. Zhang, T. J. Reck, C. Groppil, A. Arsenovic, A. Lichtenberger, R. M. Weikle, and N. S. Barker, "Terahertz micromachined on-wafer probes: Repeatability and robustness," *to be presented at 2011 IEEE MTT-S International Microwave Symposium*.



Oscillator Measurement Summary / Performance Comparison

Process Technology	Oscillation Frequency			Single-ended output power[1] (dBm)			Phase noise @ 10 MHz offset
	Design	Measured	Simulation w/ revised HBT model	Simulation w/ revised HBT model[2]	Measured (uncorrected)	Measured (corrected[3])	
THzIC1	292.4 GHz	267.4 GHz	261.5 GHz	-3.6 dBm	-5.1 dBm	-2.1 dBm	-102.4 dBc/Hz
THzIC1	315.4 GHz	286.8 GHz	280.6 GHz	-4.7 dBm	-6.9 dBm	-3.9 dBm	-99.8 dBc/Hz
THzIC1	336.5 GHz	310.2 GHz	303.7 GHz	-6.4 dBm	-9.2 dBm	-6.2 dBm	-95.6 dBc/Hz
THzIC1	387.8 GHz	346.2 GHz	346.0 GHz	-7.7 dBm	-11.0 dBm	-7.0 dBm	-88.8 dBc/Hz
THzIC2	397.0 GHz	412.9 GHz	394.5 GHz	-3.5 dBm	-11.1 dBm	-5.6 dBm	-
THzIC2	508.0 GHz	487.7 GHz	505.9 GHz	-5.2 dBm	-16.4 dBm	-8.9 dBm	-
THzIC2	587.9 GHz	573.1 GHz	586.3 GHz	-9.0 dBm	-36.2 dBm	-19.2 dBm	-



mm-wave OSC beyond 250 GHz: References

[1] R. Wanner, R. Lachner, G. Olbrich, and P. Russer, "A SiGe Monolithically Integrated 278 GHz Push-Push Oscillator," *IEEE/MTT-S International Microwave Symposium*, pp. 333 –336, June 2007.

[2] Y. Baeyens, N. Weimann, V. Houtsma, J. Weiner, Y. Yang, J. Frackoviak, P. Roux, A. Tate, and Y. Chen, "Highly efficient harmonically tuned InP D-HBT push-push oscillators operating up to 287 GHz," *IEEE/MTT-S International Microwave Symposium*, pp. 341 –344, June 2007.

[3] E. Seok, C. Cao, D. Shim, D. Arenas, D. Tanner, C.-M. Hung, and K. O, "A 410GHz CMOS Push-Push Oscillator with an On-Chip Patch Antenna," *IEEE ISSCC Dig. Tech. Papers*, pp. 472 –629, Feb. 2008.

[4] D. Huang, T. LaRocca, L. Samoska, A. Fung, and M.-C. Chang, "324GHz CMOS Frequency Generator Using Linear Superposition Technique," *IEEE ISSCC Dig. Tech. Papers*, pp. 476 –629, Feb. 2008.

[5] Q. Gu, Z. Xu, H.-Y. Jian, X. Xu, M. Chang, W. Liu, and H. Fetterman, "Generating terahertz signals in 65nm CMOS with negative-resistance resonator boosting and selective harmonic suppression," *IEEE Symposium on VLSI Circuits*, pp. 109 –110, june 2010.

[6] K. Sengupta and A. Hajimiri, "Distributed active radiation for THz signal generation," *IEEE ISSCC Dig. Tech. Papers*, pp. 288 –289, feb. 2011.

[7] O. Momeni and E. Afshari, "High power terahertz and millimeter-wave oscillator design: A systematic approach," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 3, pp. 583 –597, march 2011.

[8] V. Radisic, X. Mei, W. Deal, W. Yoshida, P. Liu, J. Uyeda, M. Barsky, L. Samoska, A. Fung, T. Gaier, and R. Lai, "Demonstration of sub-millimeter wave fundamental oscillators using 35-nm inp hemt technology," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 3, pp. 223 –225, March 2007.

[9] V. Radisic, L. Samoska, W. Deal, X. Mei, W. Yoshida, P. Liu, J. Uyeda, A. Fung, T. Gaier, and R. Lai, "A 330-GHz MMIC oscillator module," *IEEE/MTT-S International Microwave Symposium*, pp. 395 –398, June 2008.

[10] V. Radisic, D. Sawdai, D. Scott, W. Deal, L. Dang, D. Li, J. Chen, A. Fung, L. Samoska, T. Gaier, and R. Lai, "Demonstration of a 311-GHz Fundamental Oscillator Using InP HBT Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 11, pp. 2329 –2335, Nov. 2007.

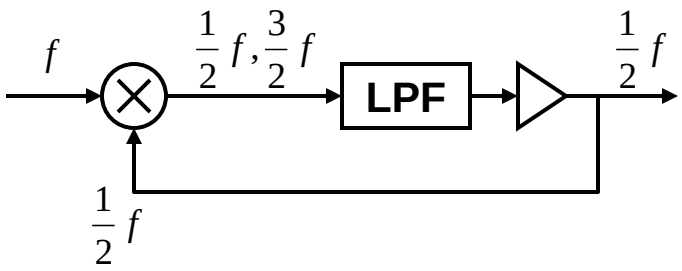
[11] B. Razavi, "A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, pp. 894 –903, april 2011.

[12] M. Seo, M. Urteaga, A. Young, V. Jain, Z. Griffith, J. Hacker, P. Rowell, R. Pierson, and M. Rodwell, ">300 GHz fixed-frequency and voltage-controlled fundamental oscillators in an InP DHBT process," *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 272-275, May 2010.

[13] M. Seo, M. Urteaga, J. Hacker, A. Young, Z. Griffith, V. Jain, R. Pierson, P. Rowell, A. Skalare, A. Peralta, R. Lin, and M. Rodwell, "InP HBT IC technology for terahertz frequencies: Fundamental oscillators up to 0.57 THz," to be published, *IEEE J. Solid-State Circuits*, Oct. 2011.

300 GHz Dynamic Frequency Divider: Schematic

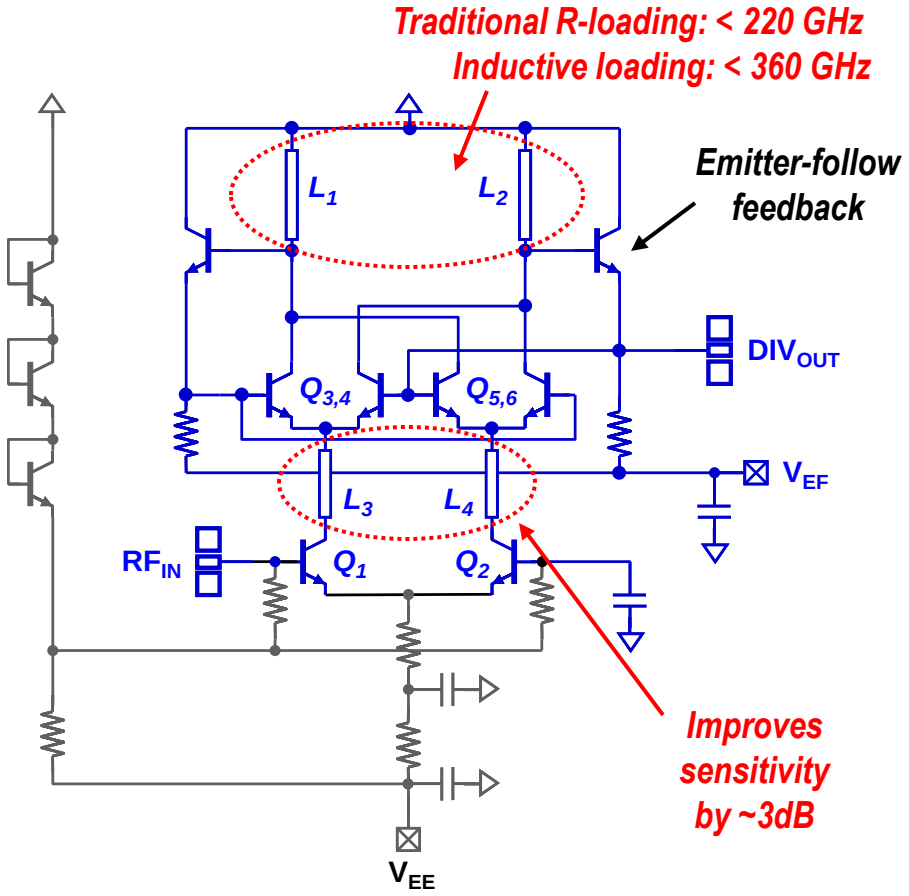
"Regenerative" frequency divider



Many implementations possible

-Single-TR circuit
w/ implicit feedback

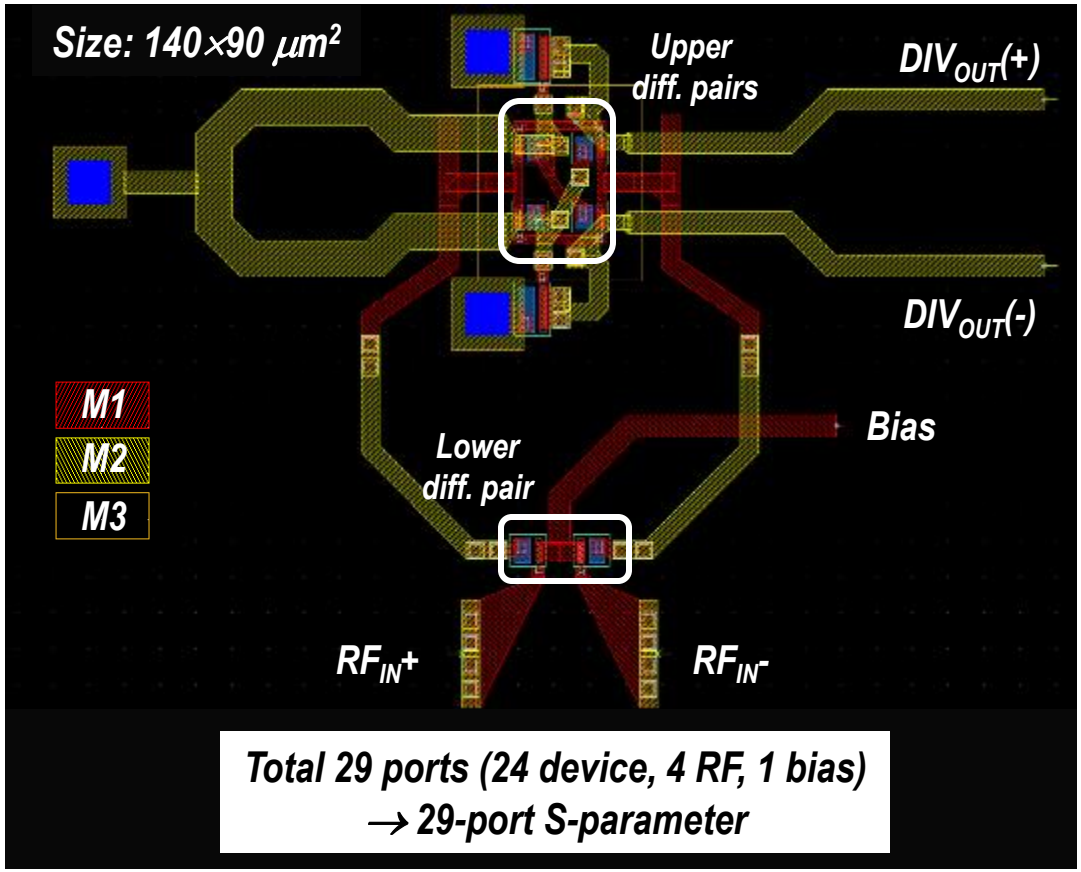
-Multi-TR circuit
w/ explicit feedback



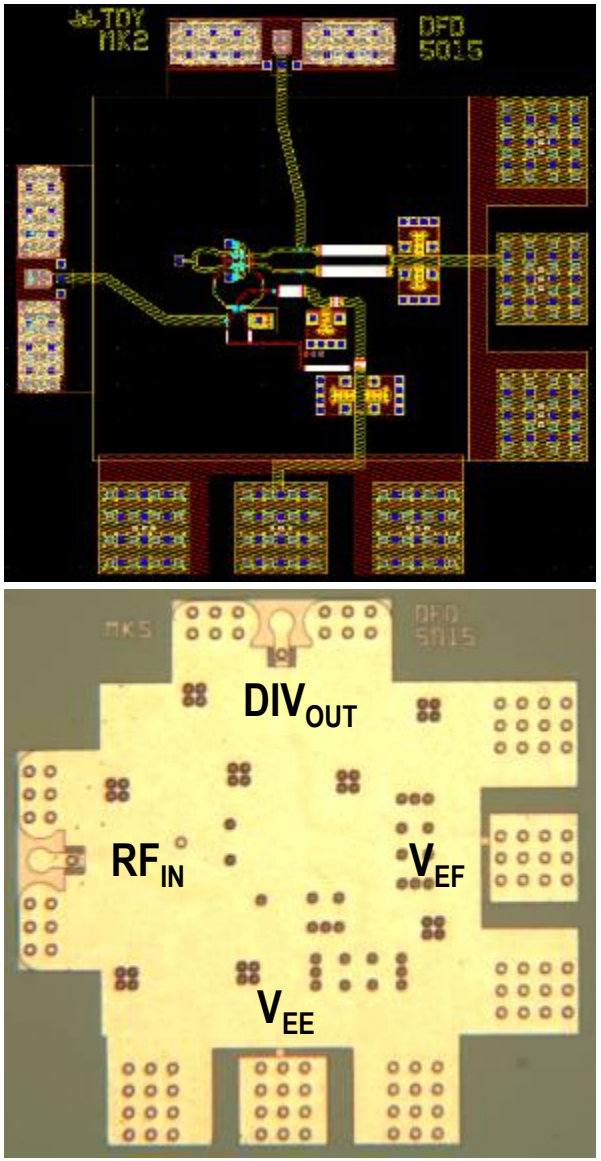
- **Topology: Double-balanced mixer with emitter follower (EF) feedback and inductive loading (Adapted from H. M. Rein's original design)**
- **Compared to a traditional resistive / trans-impedance loading, inductive loading significantly extends divider bandwidth.**
- **Beyond ~400 GHz, divider operation is ultimately limited by the EF stage.**

Divider Layout / *EM* Model

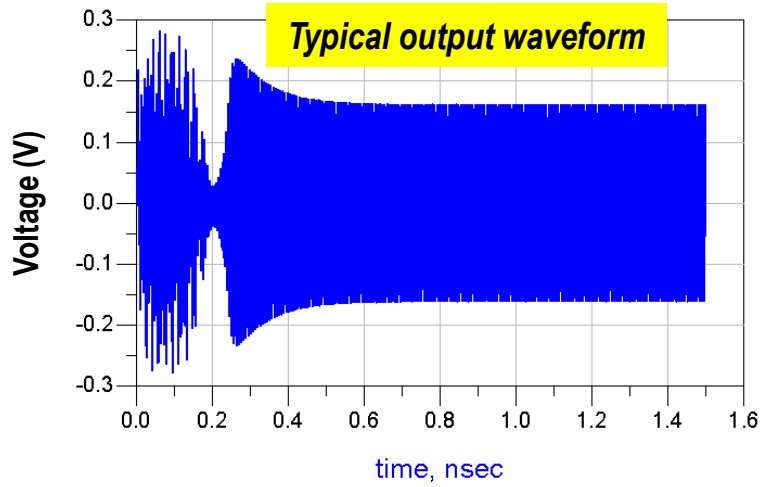
Divider Core (also EM Model)

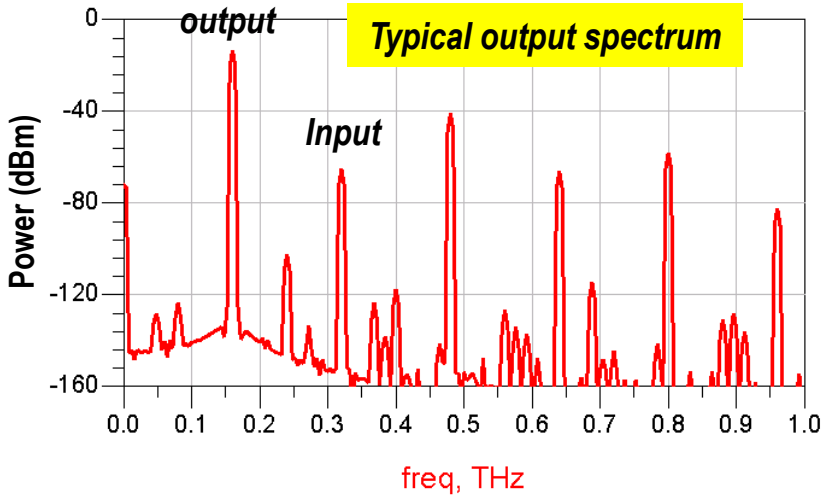


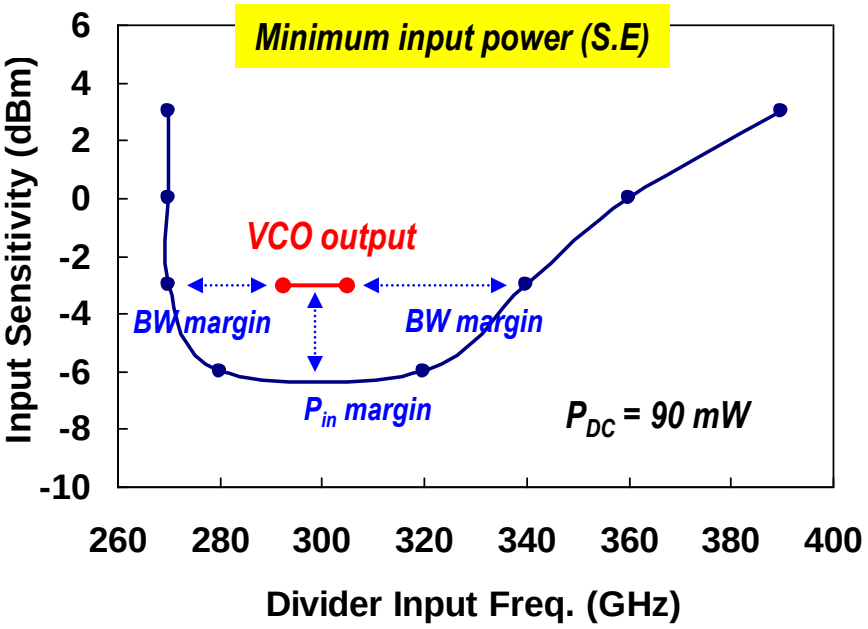
Test Chip (880×470 μm²)

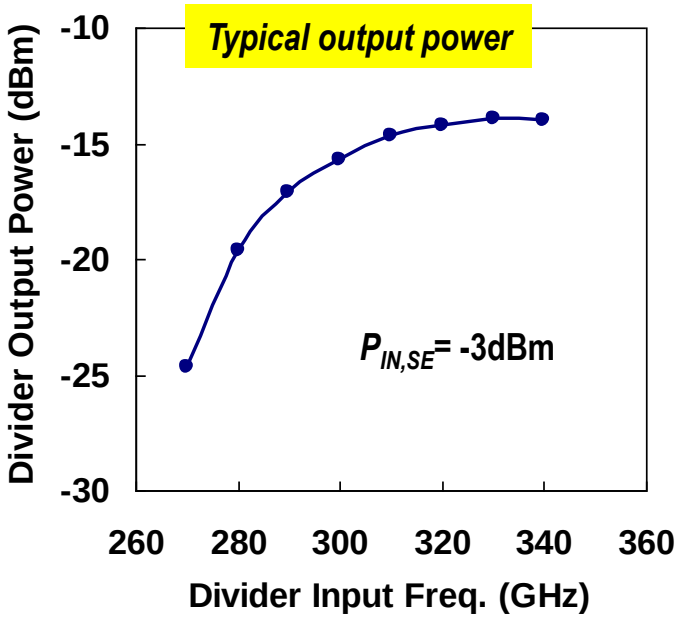


Divider Simulation Results

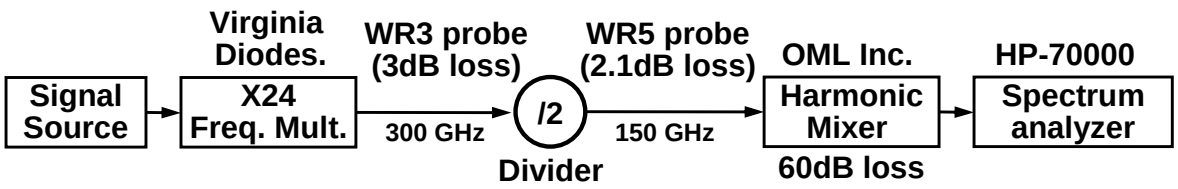


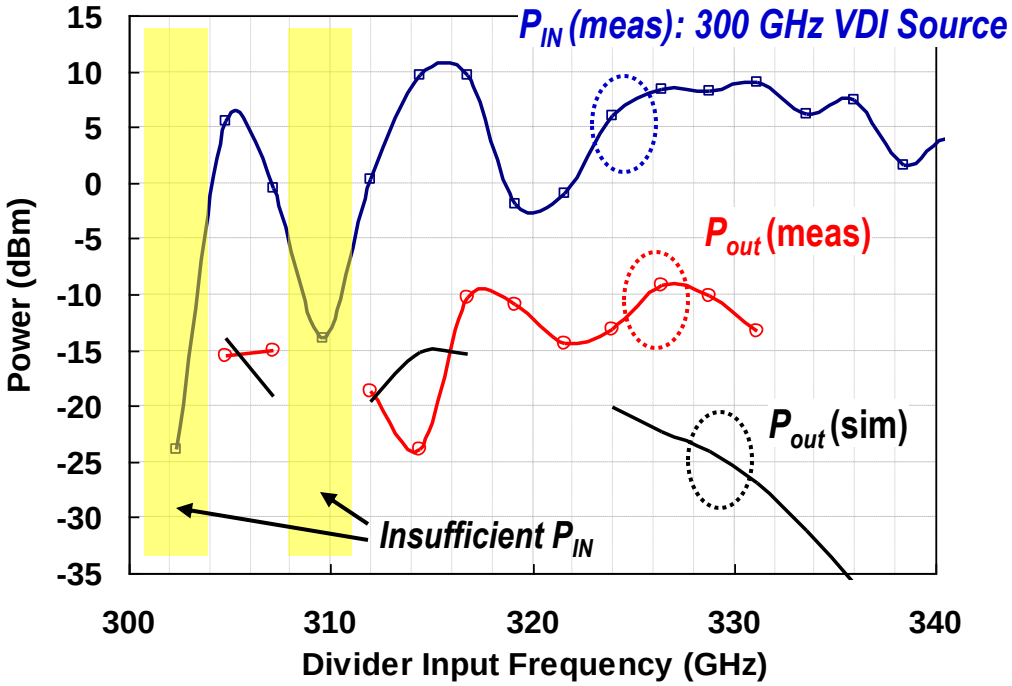


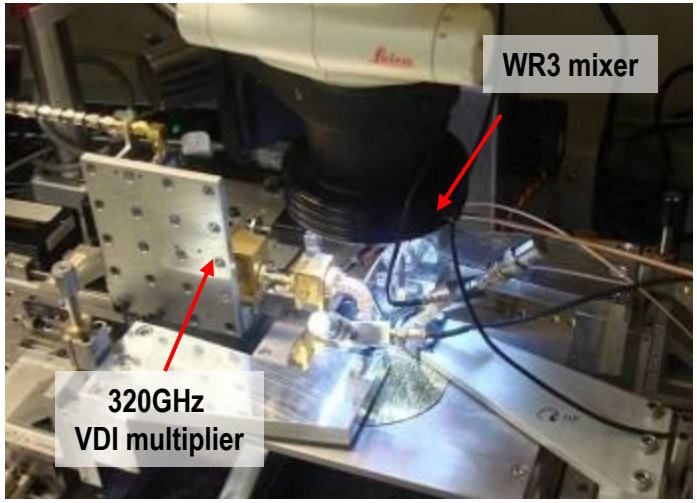


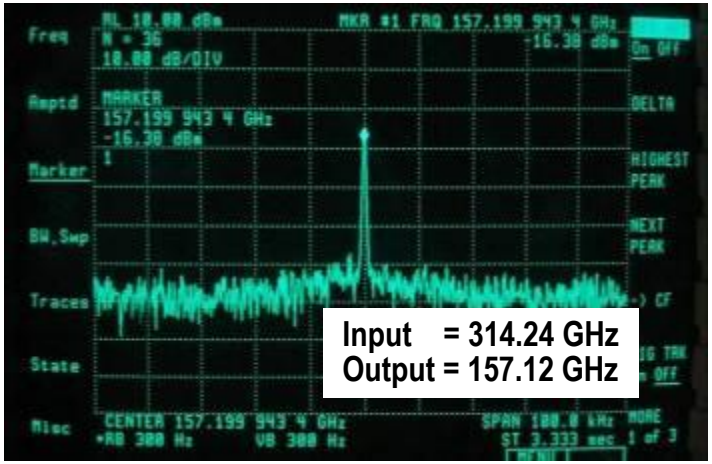


Divider Testing using External 300 GHz Source (UCSB)



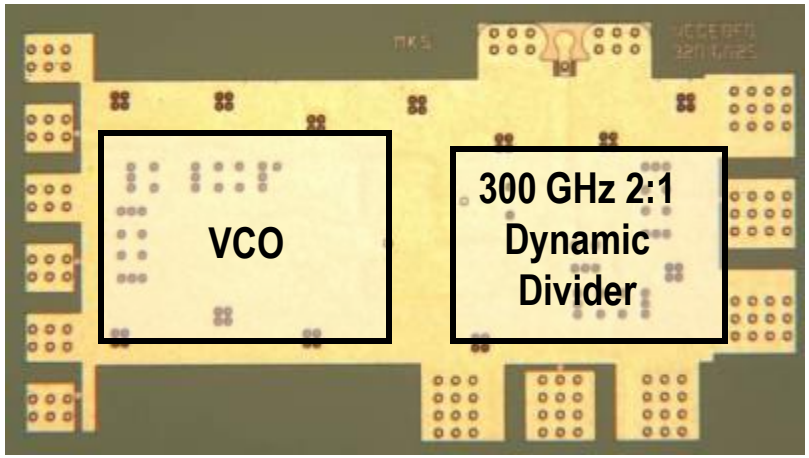


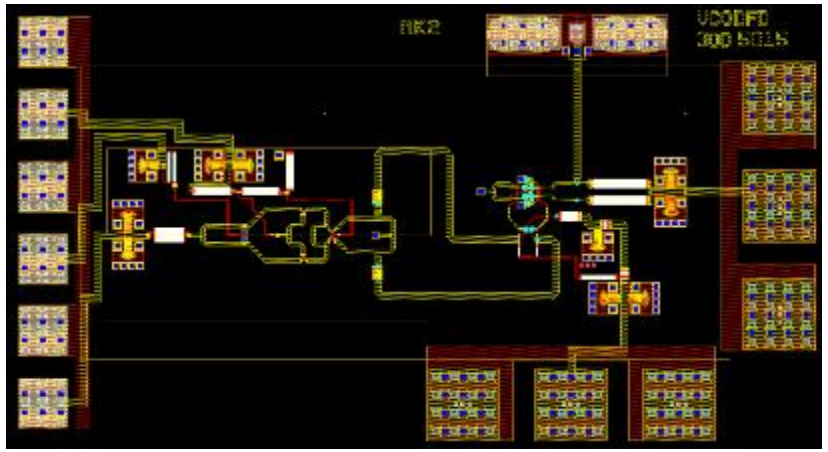




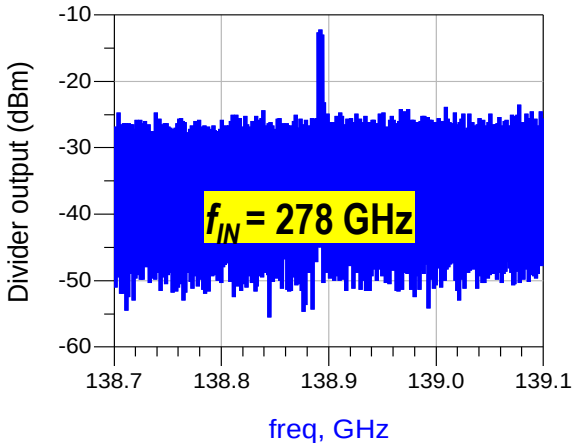
- Divider operating bandwidth: 305-330 GHz (P_{DC} = 100 mW)
- Testing @ < 300 GHz limited by insufficient source power
- Sub-harm. mixer produces multiple image responses → Use "Signal Identification" (spectrum analyzer built-in function) for correct output tone identification.

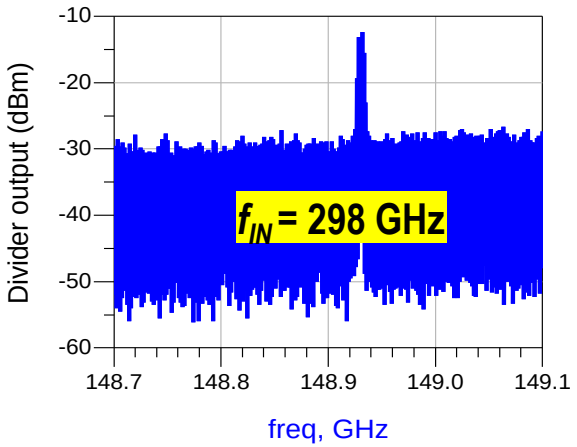
Divider Testing: Integrated VCO+DIV

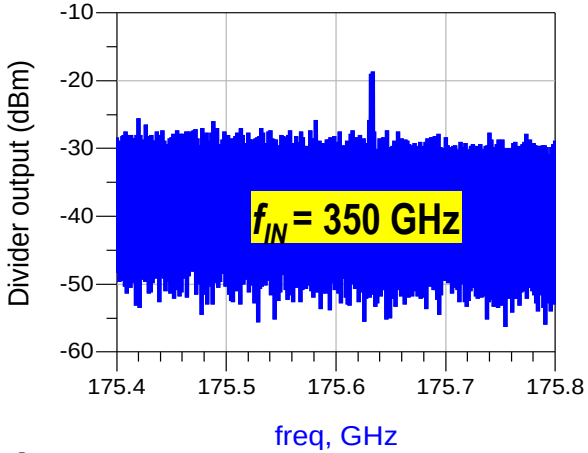




Chip Size: 1,100×600 μm²







- **Each divider design is integrated w/ VCO for on-chip self-testing**
  - **4 VCO designs centered at 275 GHz, 300 GHz, 325 GHz, and 350 GHz, w/ 5-10 GHz tuning bandwidth.**
- **Confirms divider operation from 278 GHz to 350 GHz.**

Divider: Performance Comparison

COMPARISON OF MILLIMETER-WAVE DYNAMIC FREQUENCY DIVIDERS

Ref. (year)	Type	Technology	Div. Ratio	**Max. operating freq. [GHz]**	Min. operating freq. [GHz]	Power Supply [V]	DC power[1] [mW]	Die area[2] [mm^2]
[1] (2003)	Regenerative	SiGe (f_T= 207G)	2	**100**	14	-3.8	285	-
[2] (2006)	Regenerative	SiGe:C (f_T= 200G)	2	**103**	24	+5.2	195	1×0.5
[3] (2003)	Regenerative	mHEMT (f_T= 220G)	2	**108**	86	-	360	1×0.75
[4] (2003)	Regenerative	SiGe (f_T= 200G)	2	**110**[*]	35	-5	310	0.55×0.45
[5] (2009)	Regenerative	SiGe (f_T= 210G)	2	**136**[*]	74	-3.3	118.8	1.78×0.63
[6] (2009)	Injection locking	65 nm CMOS	2	**137**	128.24	+1.1	5.5[1A]	0.6×0.5
[7] (2003)	Clocked inverter	InP HBT (f_T= 245G)	2	**150**[*]	120	-5.5	357	1.5×1.5
[8] (2006)	Regenerative	SiGe (f_T= 225G)	4	**160**	80	-5.5	650	0.55×0.45
[9] (2009)	Regenerative	SiGe:C (f_T= 215G)	2	**168**	51	+4	105[1B]	0.58×0.48
[10] (2010)	Regenerative	InP HBT (f_T= 375G)	2	**331.2**	304.8[*]	-4.1 / -3.3	85.5	0.64×0.62

[1] Including power consumption of the output buffer. [1A] Excluding the bias circuit and buffers. [1B] Excluding the interstage buffer.

[2] Including pads.

[*] Measurement limited by available test setup

References

[1] A. Rylyakov, L. Klapproth, B. Jagannathan and G. Freeman, "100 GHz dynamic frequency divider in SiGe bipolar technology," *Electronics Letter*, vol. 39, pp. 217-218, Jan. 2003.

[2] L. Wang, Y.-M. Sun, J. Borngraeber, A. Thiede and R. Kraemer, "Low power frequency dividers in SiGe:C BiCMOS technology," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits*, Jan. 2006, pp. 357-360.

[3] O. Kappeler, A. Leuther, W. Benz and M. Schlechtweg, "108 GHz dynamic frequency divider in 100 nm metamorphic enhancement HEMT technology," *Electronics Letter*, vol. 39, pp. 989-990, Jun. 2003.

[4] H. Knapp et al., "86 GHz static and 110 GHz dynamic frequency dividers in SiGe bipolar technology," *Proceedings of IEEE Int'l Microwave Sym.*, Jun. 2003, pp. 1067-1070.

[5] E. Laskin and A. Rylyakov, "A 136-GHz dynamic divider in SiGe technology," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits*, Jan. 2009, pp. 168-171.

[6] B.-Y. Lin, K.-H. Tsai and S.-I. Liu, "A 128.24-to-137.00 GHz injection-locked frequency divider in 65nm CMOS," *ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 282-283.

[7] S. Tsunashima et al., "A 150-GHz dynamic frequency divider using InP/InGaAs DHBTs," *IEEE GaAs IC Symposium Digest*, Nov. 2003, pp. 284-287.

[8] S. Trotta et al., "A new regenerative divider by four up to 160 GHz in SiGe bipolar technology," *Proceedings of IEEE Int'l Microwave Sym.*, Jun. 2006, pp. 1709-1712.

[9] H. Knapp et al., "168 GHz dynamic frequency divider in SiGe:C bipolar technology," *IEEE BCTM Digest*, Oct. 2009, pp. 190-193.

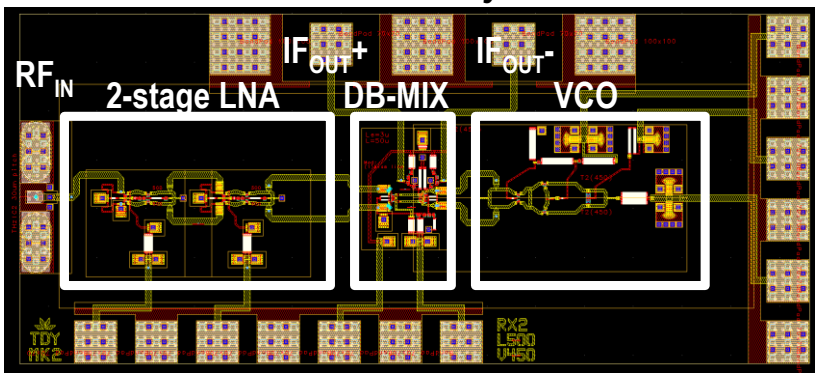
[10] M. Seo, M. Urteaga, A. Young, and M. Rodwell, "A 305-330+ GHz 2:1 Dynamic Frequency Divider using InP HBTs," *IEEE Microwave and Wireless Component Letters*, pp. 468-470, Jun. 2010

350 GHz Single-Chip Receiver

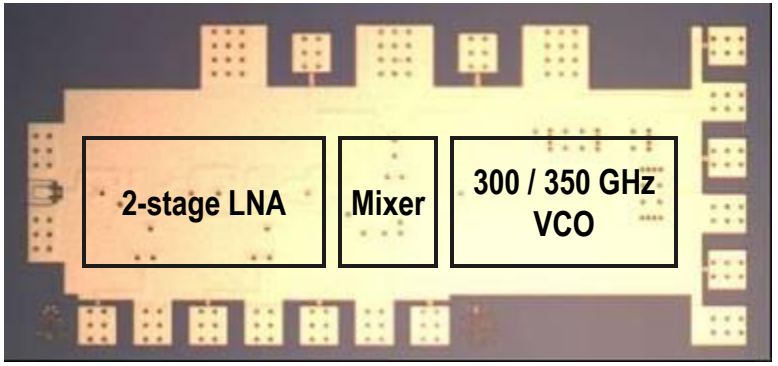
300 GHz Single-Chip PLL

300 GHz / 350 GHz Integrated Differential Receiver

Receiver Layout



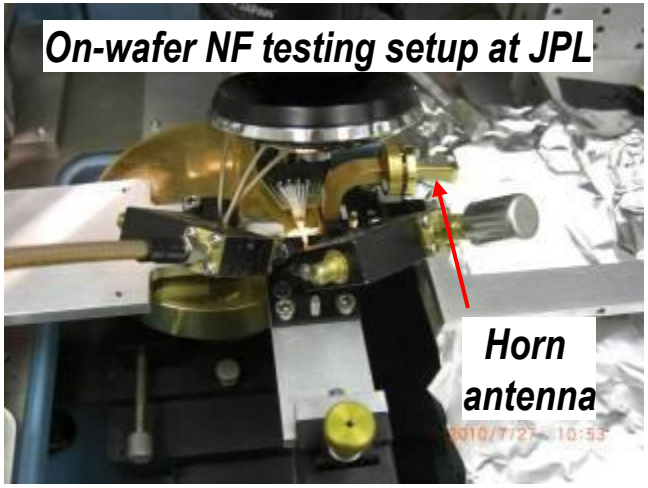
Chip photograph *(1,300×570 μm²)*



Measured Receiver Gain and Noise Figure

VCO Freq.	DC Power	Input Probe Loss	Receiver Gain	Receiver NF
305 GHz	222 mW	3 dB	32dB	10 dB
345 GHz	303mW	5.5 dB	27dB	13dB

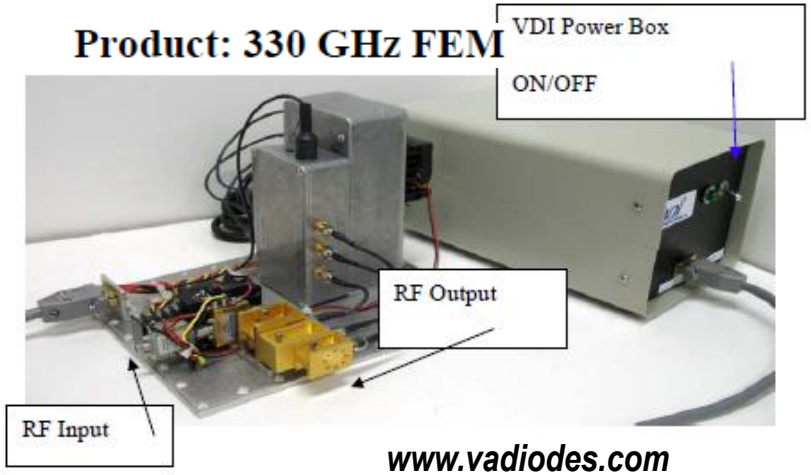
- Includes LNA, double-balanced mixer, and VCO
- Receiver designs at 300 GHz and 350 GHz
- RF input is single-ended, IF output is differential
- On-wafer noise figure (NF) testing performed at JPL
  - Hot/Cold noise source coupled to receiver w/ horn-antenna
  - NF derived using Y-factor method
  - IF frequency: 2.18 GHz, 320 MHz bandwidth



Phase-Locked Source @ 300 GHz

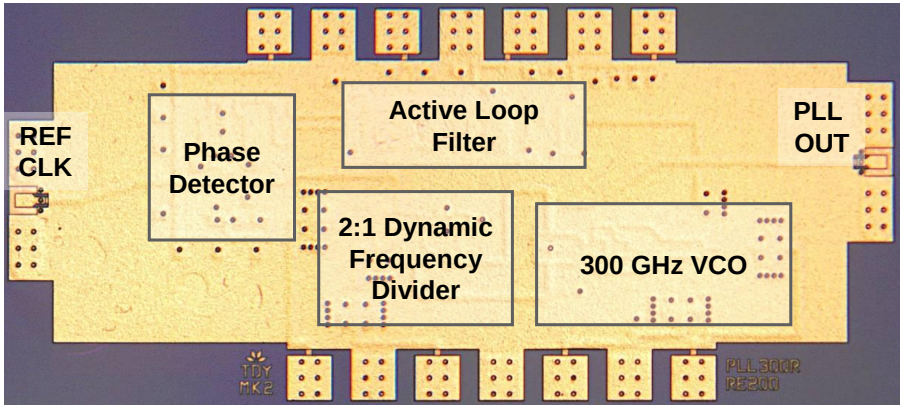
→ *Critical, power hungry, building block for THz imager / instrumentation*

Commercially available source



www.vadiodes.com

Single-Chip 300 GHz InP PLL IC

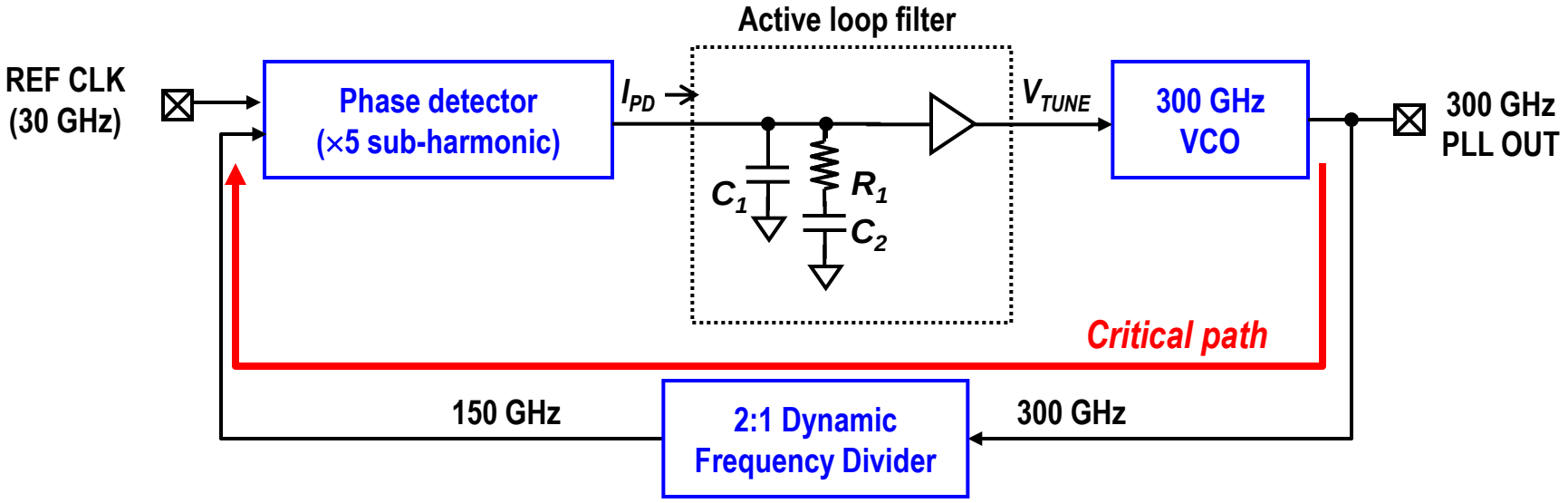


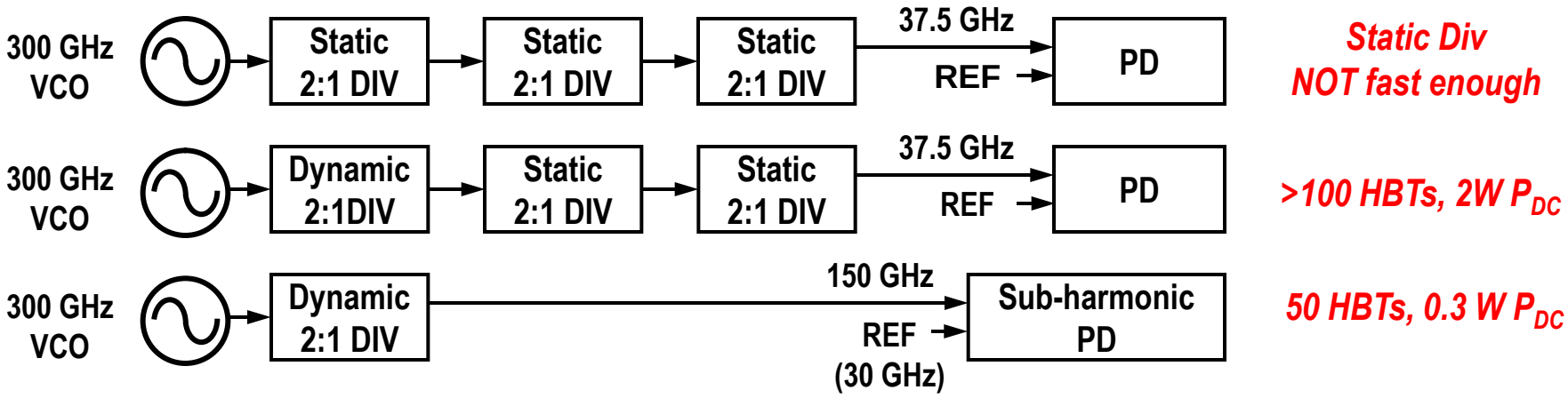
Size: 1,380×610 μm²

Technology	GaAs Shottky diodes (modules)	0.25μ InP HBT (one-chip)
Size	~1000 *cm³*	~1 *mm²* (unpackaged)
Weight	~1 *kg*	~1 *g* (unpackaged)
Power consumption	~ 10 *W*	0.3 *W*
Output power	0 ~ 13 dBm	-23 dBm
Tunable range	20 GHz (320-340 GHz)	0.36 GHz (300.76-301.12 GHz)

Low-power / Portable / Handheld

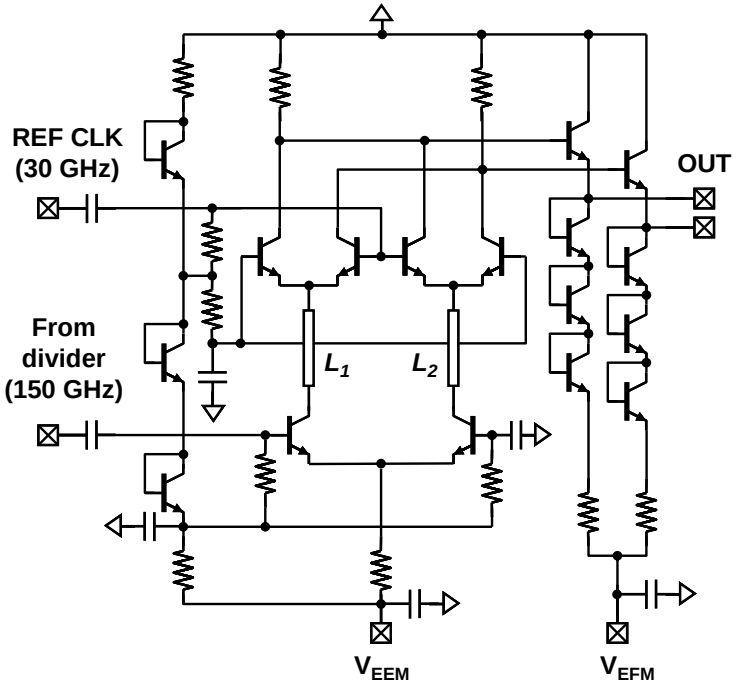
300 GHz InP PLL: Overview

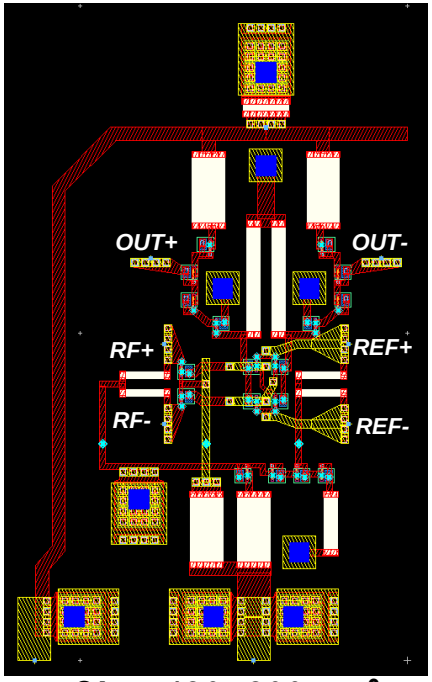




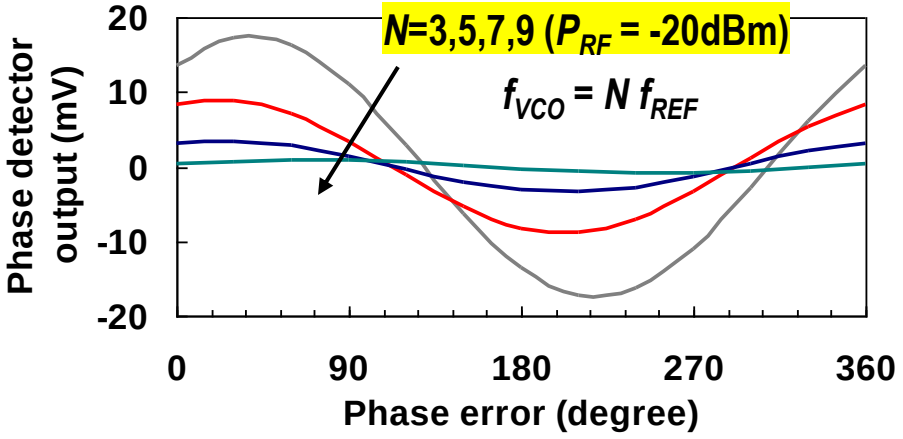
Phase Detector: 5th-order Sub-harmonic

Gilbert Cell as a Odd-sub-harmonic PD





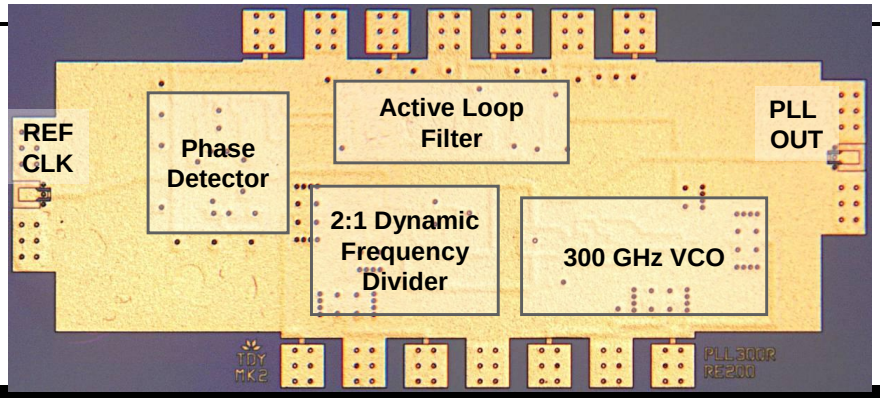
Size: 120×200 μm²

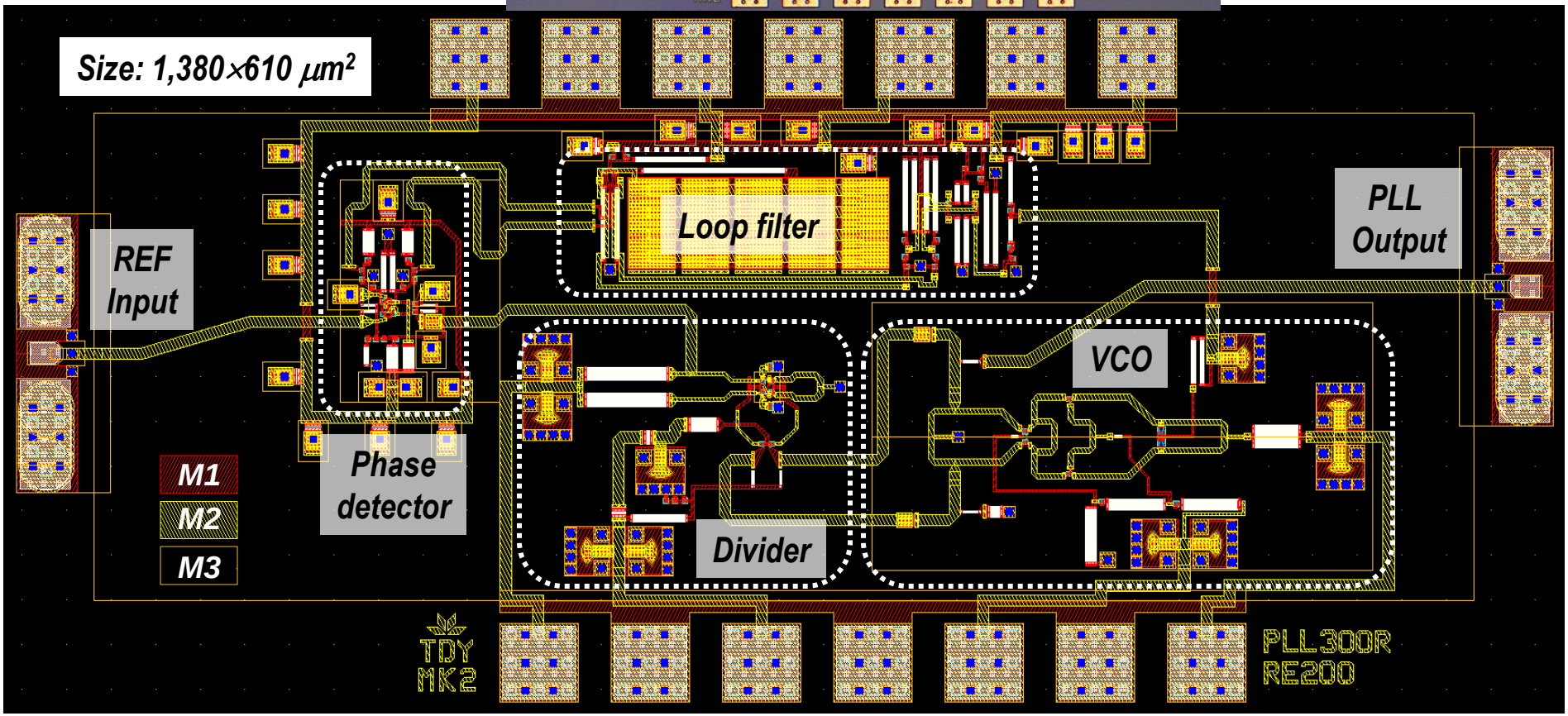


- Gilbert Cell can operate as a phase detector in odd-order sub-harm. mode
- Useful detection gain up to 5th-order (*N*=5) sub-harmonic operation
- Operation at N > 5 may suffer from increased sensitivity of active loop filter offset voltages (phase noise may also degrade).

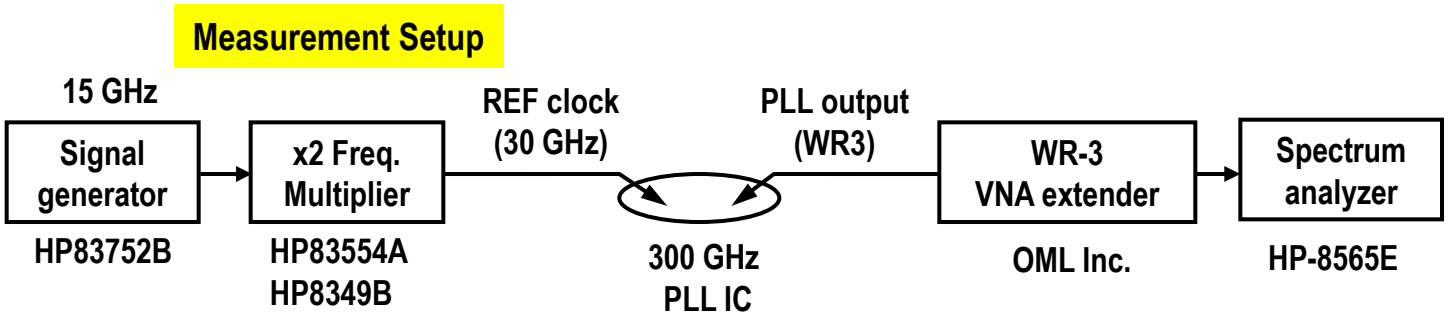
300 GHz PLL: Layout

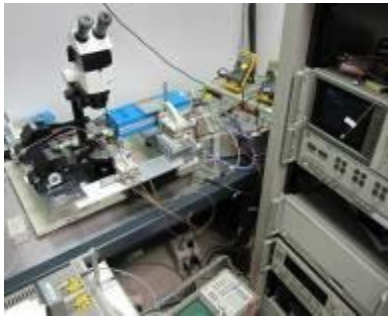
- Total 51 HBTs
- P_{DC} = 302 *mW*
  - VCO: 96 *mW,*
  - DIV: 90 *mW,*
  - PD: 26 *mW,*
  - LF: 90 *mW.*

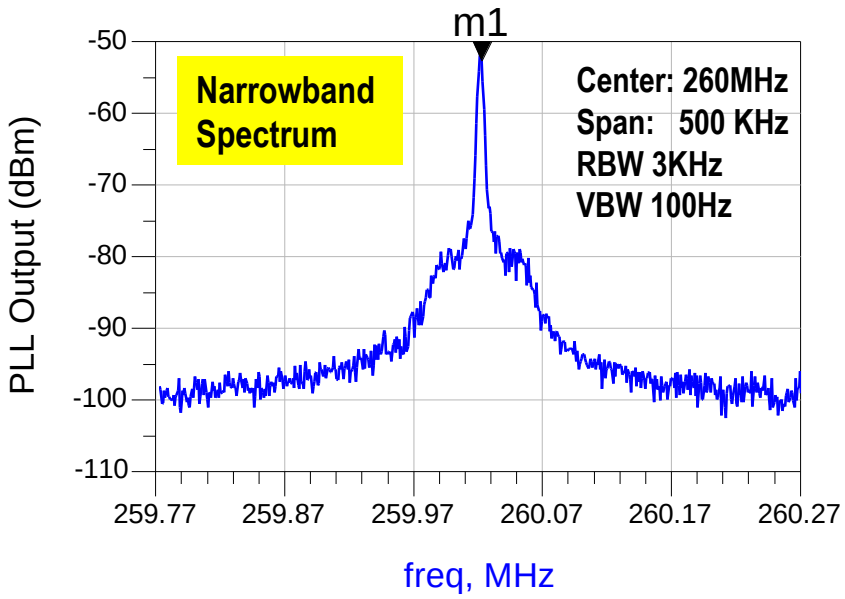


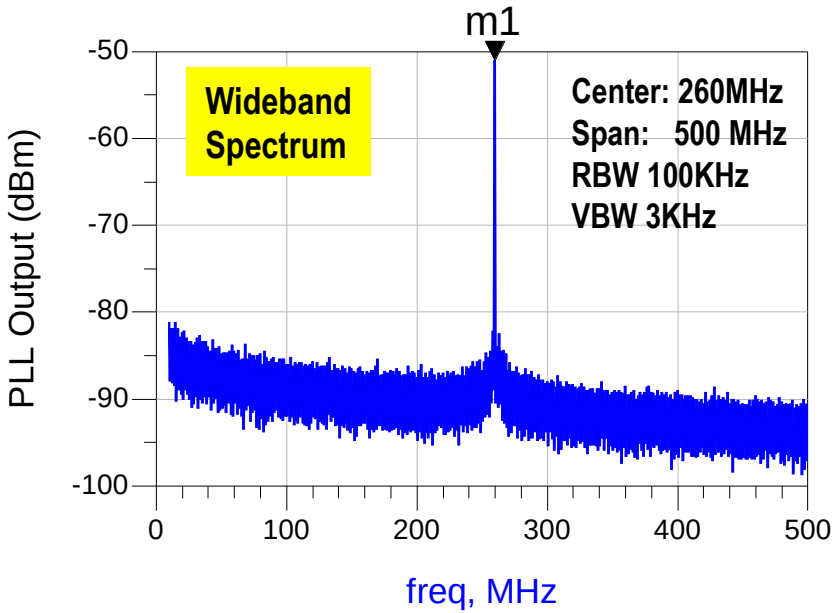


PLL: Measured Spectrum



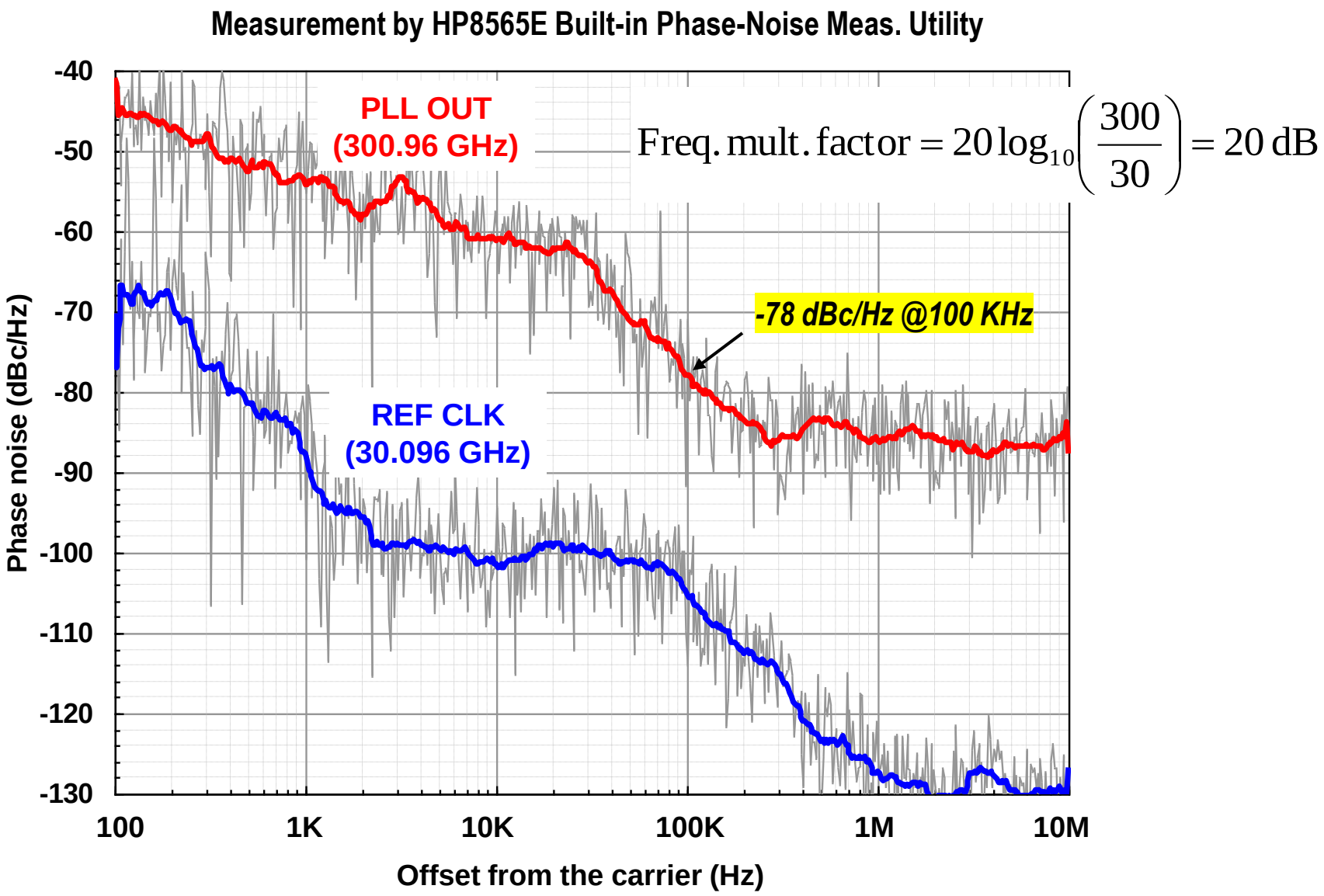




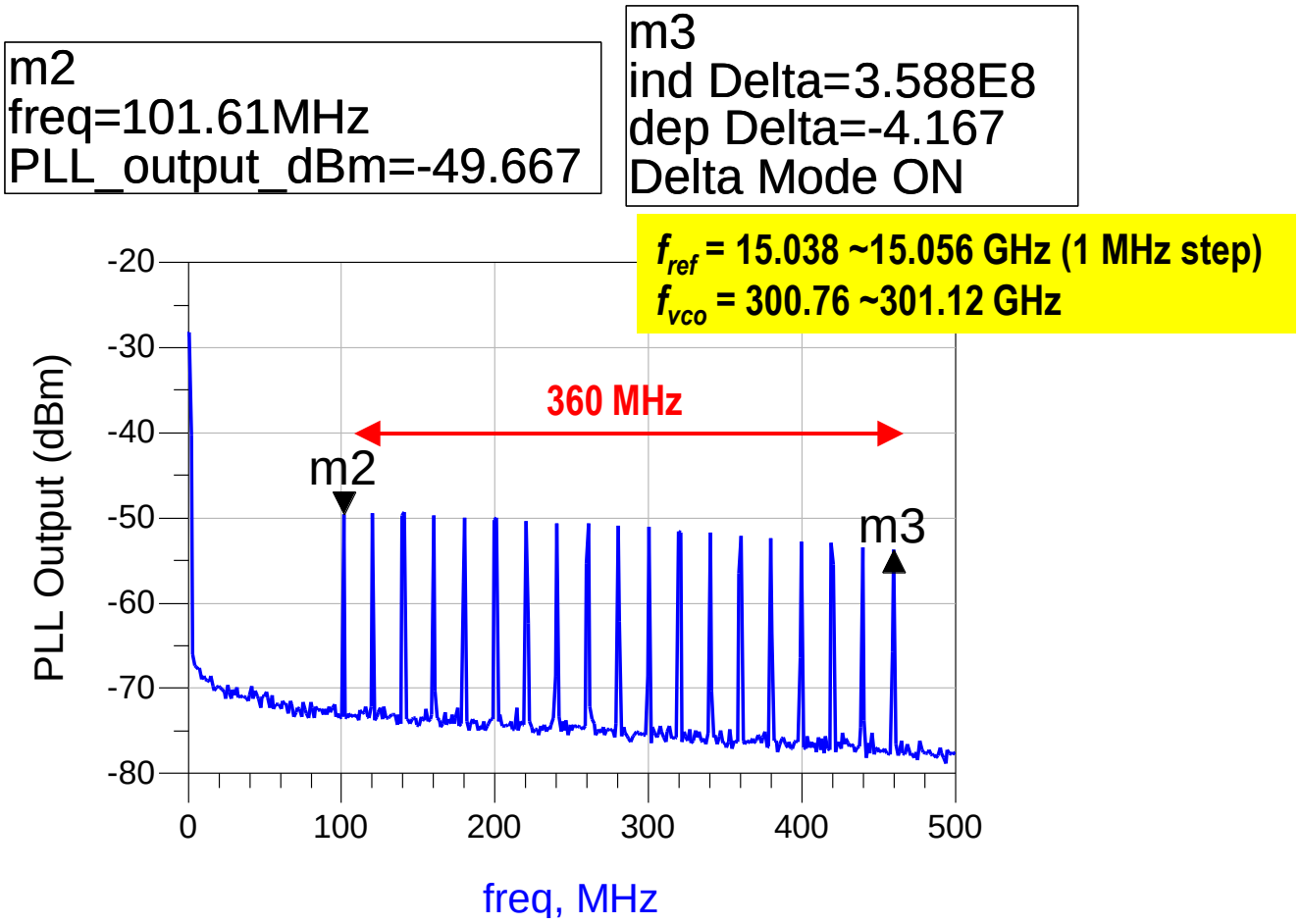


- **PLL output power = -23 dBm @ P_{DC}= 302 mW**
  - **Most of VCO output power goes to the dynamic frequency divider**

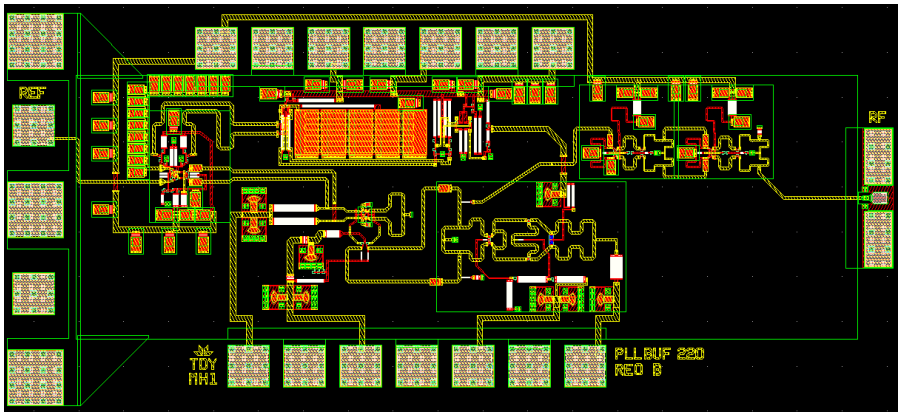
PLL: Measured Phase Noise

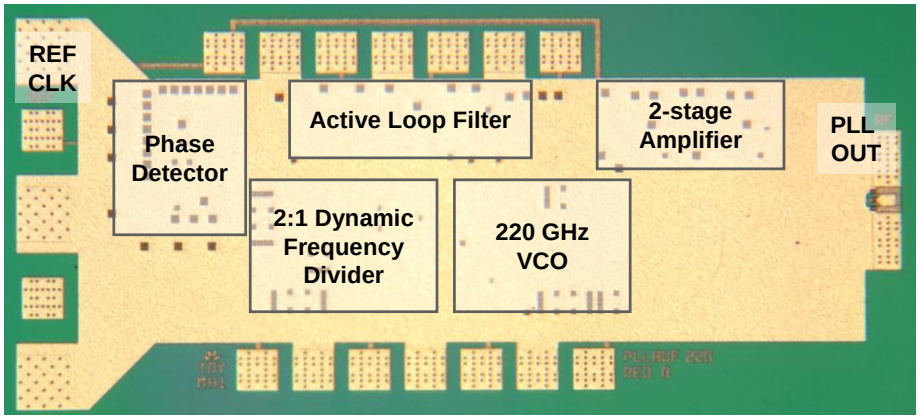


PLL: Measured Tuning Bandwidth

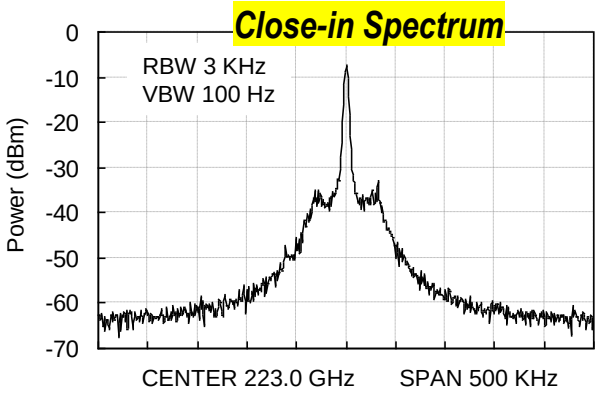


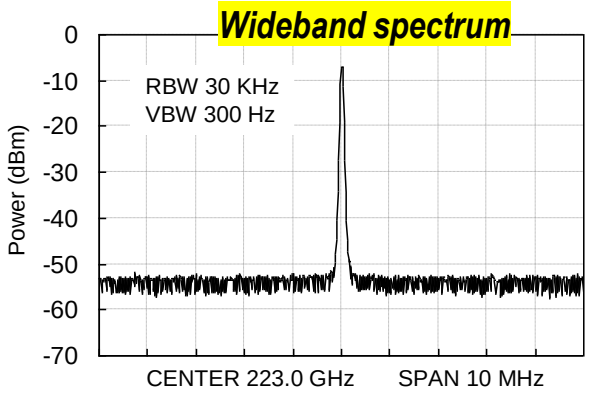
220 GHz PLL (CSICS-2011)

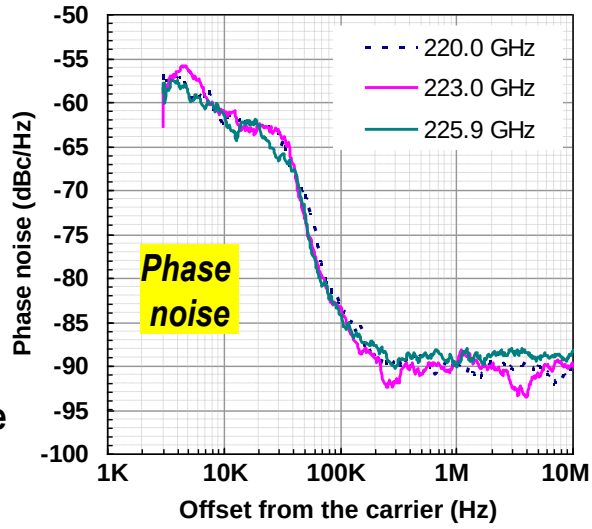




Size: 1,570×700 μm²







- **Improved locking range (increased loop filter gain) and output power (2-stage cascode output amplifier) compared to the previous 300 GHz PLL.**
- **Measured locking range: 220-225.9 GHz (BW = 5.9 GHz)**
- **PLL output power = -1 dBm (estimated) @ P_{DC}= 465 mW**
- **Phase noise: -83 dB/Hz @100 KHz**

PLL: Performance Comparison

Published mm-Wave PLLs beyond 70 GHz

	InP 300 GHz (IMS-2011)	InP 220 GHz (CSICS-2011)	RFIC-2010	JSSC-2007	ISSCC-2009	MTT-2006	JSSC-2008
Frequency [GHz]	**300.76–301.12**	**220-225.9**	162–164* 86–92 81–82	91.8–101* 45.9–50.5	95.1–96.5	79.4	73.4–73.72
Technology	**InP HBT**	**InP HBT**	0.13μm BiCMOS	0.13μm CMOS	65nm CMOS	SiGe	90nm CMOS
Divide ratio [f_{VCO}/f_{REF}]	**10**	**10**	16,32, 64,128	512	256	64	32
Phase noise @100KHz [dBc/Hz]	**-78**	**-83**	-78.9 @163GHz -93.8 @90GHz	-63.5 (50KHz offset)	-75.2 to -75.86 (1MHz offset)	-81	-88
Supply voltage [V]	**-4.3, -5.0**	**-4.3, -5.0**	1.8, 2.5, 3.3	1.5, 0.8	1.2, 1.3	5.5	1.45
P_{OUT} [dBm]	**-23**	**-1 (estimated)**	-25 @163GHz -3 @90GHz	-10 @50GHz -31 to -22 @100GHz	-	-	-
P_{DC} [mW]	**301.6**	**465.3**	1,150 to 1,250	57	43.7	-	88#
Chip area [mm^2]	**1.38×0.61**	**1.57×0.7**	1.1×1.7	1.16× 0.75	1× 0.7	-	1×0.8

***Using the second order harmonic** **# Excluding the output buffer**

References

S. Shahramian, A. Hart, A. Tomkins, A. C. Carusone, P. Garcia, P. Chevalier, and S. Voinigescu, "A D-band PLL covering the 81-82 GHz, 86-92 GHz and 162-164 GHz bands," *Proc. IEEE RFIC Symp.*, pp. 53-56, June 2010.

C. Cao, Y. Ding, and K. K. O, "A 50-GHz phase-locked loop in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, pp. 1649-1656, Aug. 2007.

K.-H. Tsai, and S.-I. Liu, "A 43.7 mW 96 GHz PLL in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 276-277, Feb. 2009.

C. Wagner, A. Stelzer, and H. Jager, "PLL architecture for 77-GHz FMCW radar systems with highly-linear ultra-wideband frequency sweeps," *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 399-402, Jun. 2006.

J. Lee, M. Liu, and H. Wang, "A 75-GHz phase-locked loop in 90-nm CMOS technology," *IEEE J. Solid-State Circuits*, pp. 1414-1426, Jun. 2008.

M. Seo, M. Urteaga, M. Rodwell and M. Choe, "A 300 GHz PLL in an InP HBT Technology," *IEEE MTT-S Int. Microwave Symp.*, Baltimore, June 2011.

M. Seo, A. Young, M. Urteaga, Z. Griffith, M. Choe, M. J. Field, and M. Rodwell, "A 220-225.9 GHz InP HBT single-chip PLL," *to be presented at IEEE Compound Semiconductor Integrated Circuit Symposium*, 2011.