InGaAs/InP DHBTs in a Dry-Etched Refractory Metal Emitter Process Demonstrating Simultaneous $f_\tau/f_{\max} \sim$ 430/800 GHz

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***Abstract*—We report an InP/$In_{0.53}Ga_{0.47}$As/InP double heterojunction bipolar transistor (DHBT) demonstrating simultaneous 430-GHz f_τ and 800-GHz $f_{\max}$. The devices were fabricated using a triple mesa process with dry-etched refractory metals for emitter contact formation. The devices incorporate a 30-nm-thick InP emitter semiconductor which enables a wet-etch emitter process demonstrating 270-nm-wide emitter–base junctions. At peak RF performance, the device is operating at 30 mW/μm^2 with $J_c = 18.4$ mA/μm^2 and $V_{\rm ce} = 1.64$ V. The devices show a peak DC common-emitter current gain (β) $\sim$ 20 and $V_{{\rm BR},CEO} = 2.5$ V.**

***Index Terms*—Heterojunction bipolar transistor (HBT), indium phosphide (InP).**

I. Introduction

LITHOGRAPHIC and epitaxial scaling of key DHBT dimensions is required for improved transistor performance enabling high speed digital logic and mixed signal circuits. This will enable submillimeter wave ICs for imaging, sensing, radio astronomy, and spectroscopy applications [1]–[5]. Specific challenges to increasing HBT performance include fabricating narrow emitter and base junctions, reducing emitter and base ohmic contact resistivities (ρ_c), and reliable operation of the transistors at high current density.

Improved transistor bandwidth is achieved by reducing transit delays and RC charging delays associated with the device. Reducing the base (T_B) and collector thicknesses (T_c) not only reduces transit delays and increases the current density J_c at the Kirk-effect limit $J_{\rm kirk} \sim T_c^{-2}$ but also increases the base–collector capacitance ($C_{\rm cb}$) per unit junction area. RC delays are reduced by reducing ohmic contact resistivities. Small-signal ($C_{\rm cb}kT/qI$) and logic ($C_{\rm cb}\Delta V/I$) delays are reduced by increasing J_c; junction lithographic dimensions are reduced partly to reduce the base spreading resistance but primarily to reduce device thermal resistance, accommodating the increased J_c.

To permit operation at high current density without electromigration or contact degradation [6], molybdenum (Mo)-based refractory emitter contacts were used in this work. Given highly stressed refractory contact metals, narrow emitter contacts readily lose adhesion to the emitter semiconductor, and fabrication yield in our laboratory for sub-200-nm emitters was nearly zero. A low stress W/$Ti_{0.1}W_{0.9}$ emitter stack and double sidewall process were, therefore, developed to permit fabrication of HBTs with sub-200-nm-width emitter contacts and junctions.

Prior to this work, InP DHBTs having 150-nm T_c and $\sim$800-GHz $f_{\max}$ have been reported [4], [7], [8] but with lower f_τ than this work. The HBTs here reported demonstrate a simultaneous 430-GHz f_τ and 800-GHz $f_{\max}$. These HBTs can be biased simultaneously at high current density and bias voltages, above 20 mW/μm^2 power density, an attribute as important as breakdown voltage in determining the useful voltage capability of a transistor [9].

II. Growth, Design, and Fabrication

The epitaxial structure (Table I) was grown on a 4″ semi-insulating InP substrate by IQE. DHBTs were fabricated using a wet-etch triple mesa process. The emitter design includes a 10-nm highly doped n-$In_{0.53}Ga_{0.47}$As cap ($N_d > 5 \times 10^{19}$ cm^{-3}) and 30-nm InP layer which enables a wet-etch process demonstrating 270-nm-wide emitter–base junctions. A TEM cross section of the emitter is depicted in Fig. 1. Wet etch of the thin InP emitter (30 nm) produces very small undercut below the emitter metal resulting in only $\sim$10-nm spacing between the emitter mesa and base contact. This greatly reduces the emitter–base gap resistance component of the base access resistance ($R_{\rm bb}$), thereby improving $f_{\max}$. The increased doping reduces the emitter depletion thickness from 40 in [7] to 15 nm under bias, reducing the calculated depletion-layer resistivity ($q^{-1}\mu^{-1}n^{-1}(x)$ integrated over the depletion region [2]) from 2.5 to < 0.5 Ω-μm^2; this will be reported separately. The InGaAs base is 30-nm thick ($9 - 5 \times 10^{19}$ cm^{-3} doping gradient), and T_c is 100 nm. The base–collector grade includes a 4.5-nm InGaAs setback and a 10.8-nm InGaAs/InAlAs submonolayer superlattice grade [10].

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TABLE I
DHBT EPITAXIAL DESIGN

T(nm)	Material	Doping (cm^{-3})	Description
10	$In_{0.53}Ga_{0.47}As$	> $5\cdot10^{19}$: Si	Emitter Cap
15	InP	$5\cdot10^{19}$: Si	Emitter
15	InP	$2\cdot10^{18}$: Si	Emitter
30	$In_{0.53}Ga_{0.47}As$	$9\text{-}5\cdot10^{19}$: C	Base
4.5	$In_{0.53}Ga_{0.47}As$	$9\cdot10^{16}$: Si	Setback
10.8	$In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$	$9\cdot10^{16}$: Si	B-C Grade
3	InP	$6\cdot10^{18}$: Si	Pulse doping
81.7	InP	$9\cdot10^{16}$: Si	Collector
7.5	InP	$1\cdot10^{19}$: Si	Sub Collector
7.5	$In_{0.53}Ga_{0.47}As$	$4\cdot10^{19}$: Si	Sub Collector
300	InP	$2\cdot10^{19}$: Si	Sub Collector
~625,000	InP	SI	Substrate

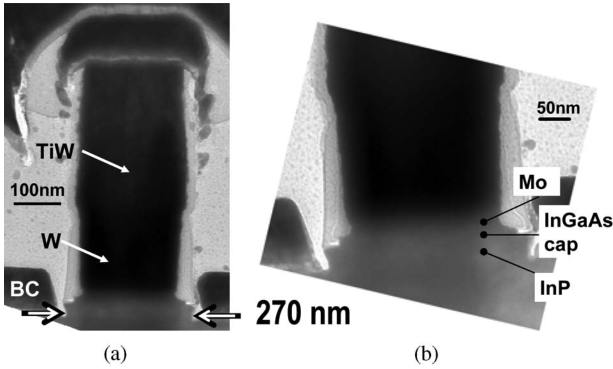

Fig. 1. (a) Cross-sectional TEM of the emitter mesa of DHBT showing the emitter profile, 270-nm emitter–base junction and (BC) base metal contact. (b) Magnified view of the emitter mesa depicting the Mo contact, InGaAs emitter cap, and InP emitter.

Emitter contacts were formed by blanket e-beam evaporation of 20-nm Mo. A $W/Ti_{0.1}W_{0.9}$ (200/300 nm) metal stack was then blanket sputter-deposited under conditions giving < 100 MPa stress. Emitter contact patterns were then defined by E-beam lithography, and the metal stack was etched by an SF_6/Ar ICP. A 30-nm SiN_x sidewall is deposited, the InGaAs cap is wet-etched, a second 30-nm SiN_x sidewall is formed, and the InP emitter is wet-etched. The vertical etch profile and the undercut at the W/TiW interface (Fig. 1) act as shadow mask for lifted-off base contacts deposited after the emitter mesa formation. The remainder of the process flow is as in [7]. HBTs with 110-nm emitter junction widths [11], as verified by TEM images, have been demonstrated in this process; here, we describe devices with greater $f_{\max}$.

III. Results

Transmission line model measurements show base $R_{\rm sh} = 620\ \Omega/\text{sq}$ and $\rho_c < 7\ \Omega\text{-}\mu\text{m}^2$ and collector $R_{\rm sh} = 11\ \Omega/\text{sq}$ and $\rho_c = 6\ \Omega\text{-}\mu\text{m}^2$. Total emitter access resistivity $\rho_{\rm ex} < 5\ \Omega\text{-}\mu\text{m}^2$ was extracted from the RF data. HBTs with an emitter area $A_{\rm je} = 0.27\ \times 3.5\ \mu\text{m}^2$ show peak DC common-emitter current gain $\beta = 20$, with common-emitter breakdown voltage $V_{\rm BR,CEO} = 2.5$ V ($J_c = 0.01$ mA/μm^2). Common-emitter current–voltage and Gummel characteristics are shown in Fig. 2.

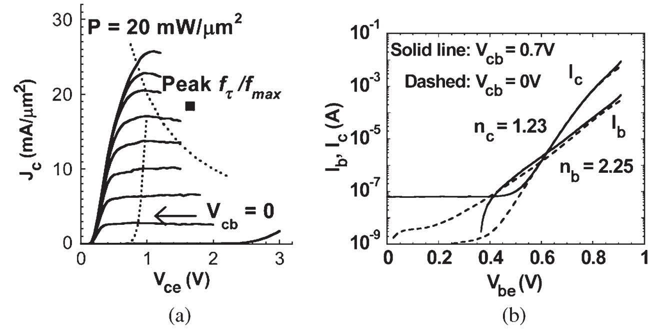

Fig. 2. (a) Common-emitter current–voltage characteristics ($I_{b,\rm step} = 200\ \mu$A) and (b) Gummel plot of a DHBT with $A_{\rm je} = 0.27\ \times 3.5\ \mu\text{m}^2$.

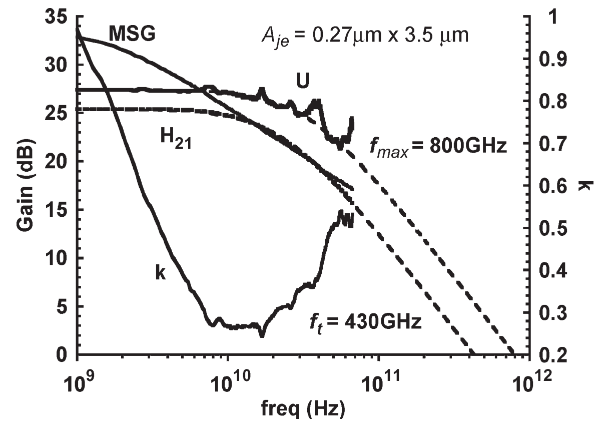

Fig. 3. Measured RF gains and stability factor (k) for the DHBT in 1–67-GHz band using off-wafer LRRM calibration in a lumped pad structure. The DHBT was biased at $I_c = 17.4$ mA, $V_{\rm ce} = 1.64$ V, and $V_{\rm cb} = 0.7$ V.

Measurements of 1–67-GHz range HBTs embedded in a ground-signal-ground pad structure were carried out after performing a standard line-reflect-reflect-match (LRRM) calibration on an Agilent E8361A PNA, bringing the reference planes to the probe tips. On wafer, short and open circuit pad structures identical to those used by the devices were measured after calibration to deembed associated transistor pad parasitics from device measurements [12]. For all measurements, Port1 and Port2 output powers were set at -37 dBm, and a power slope of 0.25 dB/GHz was used. Peak RF performance was obtained at $I_c = 17.4$ mA and $V_{\rm ce} = 1.64$ V ($V_{\rm cb} = 0.7$ V, $J_c = 18.4$ mA/μm^2, $P = 30.2$ mW/μm^2, and $C_{\rm cb}/I_c = 0.32$ psec/V). Extrapolations from single-pole least-squares fit to the measured current gain H_{21}, and Mason's unilateral gain U indicates cutoff frequencies $f_\tau \sim 430$ GHz and $f_{\max} \sim 800$ GHz (Fig. 3). Extrapolation at -20 dB/dec of U and H_{21} computed from 150–180 GHz S-parameter measurements of HBTs of identical geometry embedded in a thin-film microstrip on-wafer TRL calibration environment [13] yielded $f_\tau \sim 455$ GHz and $f_{\max} \sim 820$ GHz at the same bias conditions.

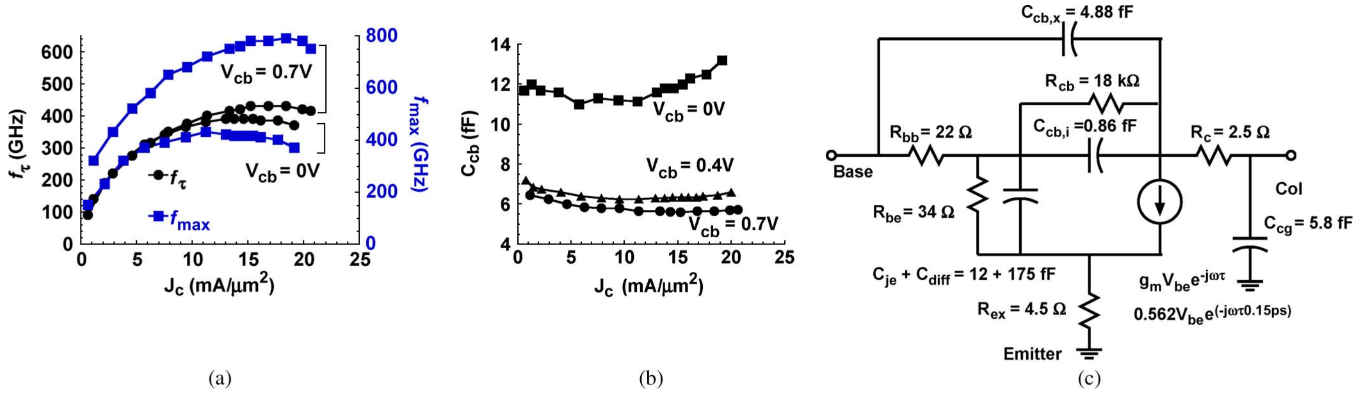

Fig. 4. (a) f_τ and $f_{\max}$. (b) $C_{\rm cb}$ dependence on $V_{\rm cb}$ and J_c for the reported DHBT. $C_{\rm cb}$ was extracted from Y_{12} at 5 GHz. (c) Hybrid-π equivalent circuit at peak RF performance from 1–67-GHz RF data extracted for the bias conditions: $I_c = 17.4$ mA, $V_{\rm ce} = 1.64$ V, and $V_{\rm cb} = 0.7$ V.

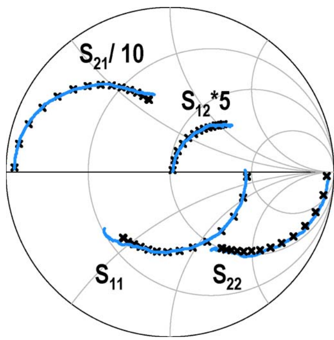

Fig. 5. Comparison of (Solid line) measured S-parameters of Fig. 3 and (x) simulated S-parameters from the model of Fig. 4(c) from 1–67 GHz.

Fig. 4(a) and (b) shows the variation in f_τ, $f_{\max}$ and extracted $C_{\rm cb}$ as a function of J_c and base–collector voltage ($V_{\rm cb}$). A small-signal hybrid-π equivalent circuit [14] extracted from the RF data is shown in Fig. 4(c). Fig. 5 compares the measured S-parameters of Fig. 3 to simulated S-parameters from hybrid-π model of Fig. 4(c). The Kirk effect is observed at $J_c = 21\ \mathrm{mA}/\mu\mathrm{m}^2$ ($V_{\rm ce} = 1.65$ V) when f_τ falls to 95% of its peak value.

IV. Conclusion

InP DHBTs having simultaneous 430-GHz $f_\tau$and 800-GHz $f_{\max}$ have been demonstrated. The thin emitter design and all wet-etch process results in small undercut below the contact metal, permitting fabrication of narrow emitter junctions. Comparing with other high $f_{\max}$ HBTs, reduced collector thickness (100 nm) and emitter access resistance have resulted in improved f_τ, while high $f_{\max}$ has been maintained through reduced $R_{\rm bb}$ by reduced spacing between the emitter mesa and the base contact. Reduction in $C_{\rm cb}$ by reducing the base contact width, emitter width, and sidewall thickness should lead to further improvement in device performance.

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