A Distributed Model for Border Traps in $Al_2O_3 - InGaAs$ MOS Devices

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***Abstract*—A distributed border trap model based on tunneling between the semiconductor surface and trap states in the gate dielectric film is formulated to account for the observed frequency dispersion in the capacitance and conductance of $Al_2O_3/InGaAs$ MOS devices biased in accumulation. The distributed circuit model is more physical and descriptive than previous lumped circuit border trap models in the literature. The distributed model correctly depicts the frequency dependence of both capacitance and conductance data in accumulation. A border trap volume density is extracted from the quantitative agreement with measured data.**

***Index Terms*—Border trap, MOS, tunneling, III-V.**

I. Introduction

RECENTLY, III-V compound semiconductor MOSFETs have been intensely investigated to replace silicon CMOS for high-performance digital applications. In many reports in the literature [1]–[5], frequency dispersion is commonly observed in the capacitance–voltage (C–V) and conductance–voltage (G–V) data in accumulation, as shown in the example of a $Pt/Al_2O_3/n\text{-}In_{0.53}Ga_{0.47}As$ MOS in Fig. 1. Such dispersion cannot be explained by the conventional interface states whose time constant in accumulation is far too short for the range of frequencies 1 kHz–1 MHz in typical measurements [6], [7]. On the other hand, trap states inside the gate insulator, called border traps or bulk traps, do have long time constants as they interact with the conduction band electrons via tunneling [8]. Moreover, the dispersion in the accumulation capacitance of such devices has been reported to be insensitive to temperature, consistent with a tunneling mechanism for charge trapping [4].

In previous publications, border traps are modeled by a lumped *RC* circuit [9], [10] which does not reflect the distributed nature of border trap capacitance over the depth of the gate insulator. In this paper, we develop a distributed circuit model for border traps based on tunneling mechanism. A differential equation is derived and solved numerically to yield frequency-dependent capacitance and conductance in close agreement with the $Pt/Al_2O_3/n\text{-}In_{0.53}Ga_{0.47}As$ MOS data in accumulation.

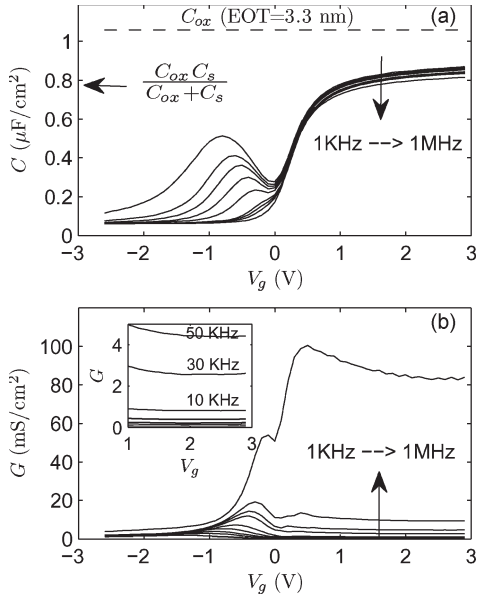

Fig. 1. Experimental (a) C-V and (b) G–V data of n-type InGaAs MOS. The inset in (b) magnifies the G–V data at low frequencies.

II. Distributed Circuit Model for Border Traps

In MOS devices, border traps in the gate dielectric film can exchange charge with mobile carriers in the semiconductor bands through tunneling. Fig. 2 shows schematically the tunneling process between border traps and conduction band in an n-type MOS device biased in accumulation. The time constant associated with charge exchange between border traps and semiconductor is governed by the tunneling mechanism which gives an exponential dependence on the trap distance x from the interface [8], [9]

$$\tau(x) = \tau_0 e^{2\kappa x}. \tag{1}$$

Here, τ_0 is inversely proportional to the carrier density at the semiconductor surface, and κ is the attenuation coefficient for

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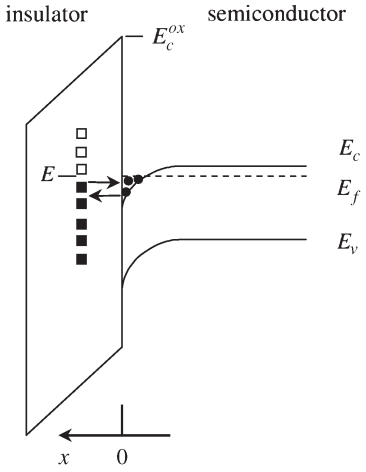

Fig. 2. Schematic diagram of tunneling between border traps in gate insulator and conduction band of semiconductor.

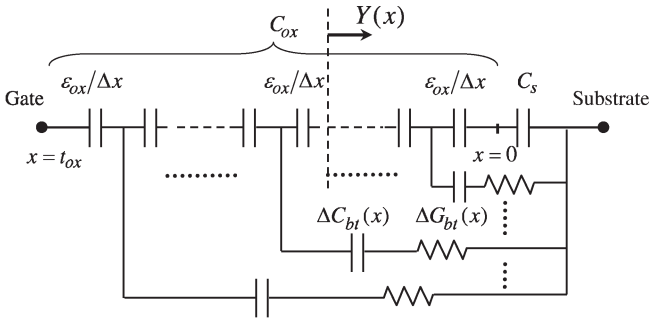

Fig. 3. *RC* equivalent circuit for border traps distributed over the depth of the insulator. The semiconductor capacitance is represented by C_s.

an electron wave function of energy E decaying under an energy barrier $E_C^{\rm ox} > E$:

$$\kappa = \sqrt{2m^*\left(E_C^{\rm ox} - E\right)}/\hbar. \tag{2}$$

m^* is electron effective mass in the dielectric and $E_C^{\rm ox}$ is the energy of the top of the dielectric barrier as indicated in Fig. 2.

For a given gate dc bias, only border traps at energy $E = E_f$ change occupancy in response to a small signal ac modulation. The effects of border traps at a specific depth on the small-signal MOS admittance can be modeled by a serial combination of capacitance and conductance. With a continuous distribution of border traps throughout the oxide thickness, the equivalent circuit of the MOS device is of a distributed form shown in Fig. 3. The border traps within an incremental depth Δx at x are represented by an incremental capacitance $\Delta C_{\rm bt}(x)$ and an incremental conductance $\Delta G_{\rm bt}(x)$ connected in series. If the volume and energy density of border traps at $E = E_f$ is $N_{\rm bt}(x)$ in units of cm^{-3}Joule^{-1}, then

$$\Delta C_{\rm bt}(x) = q^2 N_{\rm bt}\Delta x. \tag{3}$$

$\Delta G_{\rm bt}(x)$ and $\Delta C_{\rm bt}(x)$ are related by the time constant $\tau(x)$:

$$\Delta C_{\rm bt}(x)/\Delta G_{\rm bt}(x) = \tau(x) = \tau_0 e^{2\kappa x}. \tag{4}$$

In Fig. 3, $\epsilon_{\rm ox}$ is the permittivity of the insulator and C_s is the semiconductor capacitance.

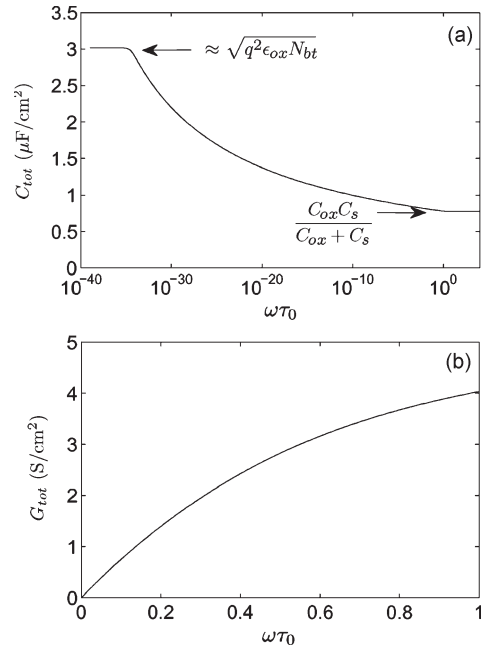

Fig. 4. Example of numerical solution to (6): Real and imaginary parts of $Y(x = t_{\rm ox})$ versus $\omega\tau_0$ with $\tau_0 = 1.6 \times 10^{-9}$ s.

If we define $Y(x)$ to be the equivalent admittance at a point x looking into the semiconductor in Fig. 3, the recursive nature of the distributed circuit gives the admittance of the next point $x + \Delta x$ as

$$Y(x+\Delta x) = \frac{1}{\frac{1}{j\omega\Delta C_{\rm bt}(x)} + \frac{1}{\Delta G_{\rm bt}(x)}} + \frac{1}{\frac{\Delta x}{j\omega\epsilon_{\rm ox}} + \frac{1}{Y(x)}}. \tag{5}$$

Substituting (3), (4) for $\Delta C_{\rm bt}(x)$ and $\Delta G_{\rm bt}(x)$, the first-order terms in Δx then yields a differential equation for $Y(x)$

$$\frac{dY}{dx} = -\frac{Y^2}{j\omega\epsilon_{\rm ox}} + \frac{j\omega q^2 N_{\rm bt}}{1 + j\omega\tau_0 e^{2\kappa x}}. \tag{6}$$

The boundary condition is $Y(x = 0) = j\omega C_s$. If the border trap density $N_{\rm bt}$ is a constant, (6) can be transformed to a hypergeometric differential equation, whose solution is a Gaussian hypergeometric function [11].

In general, (6) needs to be solved numerically to obtain the total admittance seen by the gate

$$Y(x = t_{\rm ox}) \equiv G_{\rm tot} + j\omega C_{\rm tot}. \tag{7}$$

A typical example of the solutions $C_{\rm tot}$ versus $\ln\omega$ and $G_{\rm tot}$ versus ω is given in Fig. 4. In the high-frequency limit $\omega\tau_0 \geq 1$, none of the border traps respond to the ac signal and $C_{\rm tot}$ equals $C_{\rm ox}$ in series with C_s as expected. For the measurement frequencies of 1 kHz–1 MHz, $10^{-5} < \omega\tau_0 < 10^{-2}$, $C_{\rm tot}$ varies linearly with $\ln(1/\omega)$, and $G_{\rm tot}$ linearly with ω, i.e., $G_{\rm tot}/\omega \approx constant$. Both are consistent with the data trends in Fig. 1. The constant $G_{\rm tot}/\omega$ reflects the fact that, at any given gate bias, border trap response spans a wide spectrum of frequencies due to their depth distribution—a clear distinction from conventional interface traps [6].

For $\omega = 0$ or dc, Fig. 3 becomes a purely capacitive circuit and (6) is reduced to a real equation for $Im[Y(x)]$ that can

be solved analytically. If $2qt_{\rm ox}\sqrt{N_{\rm bt}/\epsilon_{\rm ox}} \gg 1$, then $C_{\rm tot}(\omega = 0) \approx \sqrt{q^2\epsilon_{\rm ox}N_{\rm bt}}$ [left plateau in Fig. 4(a)], insensitive to C_s. Note that $\sqrt{q^2\epsilon_{\rm ox}N_{\rm bt}}$ can be larger than both C_s and $C_{\rm ox}$—a result that fundamentally differs from those of lumped circuit models.

III. Results and Discussion

The multiple frequency C–V and G–V data in Fig. 1 are measured from a $Pt/Al_2O_3/n\text{-}In_{0.53}Ga_{0.47}As$ MOS device fabricated under similar processing procedures as in [12]. The semiconductor layer structure is 1 μm 2×10^{16} cm^{-3} doped n-$In_{0.53}Ga_{0.47}As$ on 100 nm 5×10^{18} cm^{-3} doped n-$In_{0.53}Ga_{0.47}As$ on n^+ InP substrate. The Al_2O_3 film is prepared by 50 cycles of atomic layer deposition with trimethyl aluminum precursor and water vapor oxidant. The sample is then annealed in forming gas for 30 min at 400 °C. The dashed line in Fig. 1(a) indicates the oxide capacitance $C_{\rm ox}$ determined by matching the accumulation capacitance measured at 1 MHz, which is least affected by border traps, to that of an ideal simulated InGaAs MOS with quantum-mechanical and nonparabolic band effects.

It has been reported that parasitic resistance in series with the MOS capacitor could make the apparent $C_{\rm tot}$ lower at high frequencies, e.g., 1 MHz. We rule this out as the cause of the dispersion in the measured C–V because the dispersion persists to as low frequencies as a few kilohertz [see Fig. 5(a)], where the series resistance plays no role. Moreover, the estimated spreading resistance in the substrate for the 100 μm dot size is less than a few ohms—several orders of magnitude smaller than the capacitive reactance at 1 MHz.

The experimentally measured capacitance and conductance versus frequency at $V_g = 2.9$ V are compared to model calculations in Fig. 5. For model parameters, the semiconductor capacitance C_s is based on the numerically simulated value at V_g, somewhat lower than 2.9 V to account for stretch-out of the experimental C–V. The serial combination of $C_{\rm ox}$ and C_s gives a $C_{\rm tot}$ [labeled in Fig. 1(a)] slightly below the measured 1-MHz capacitance at $V_g = 2.9$ V. κ is calculated from (2) with $m^* = 0.5m_0$ and $E_C^{\rm ox} - E = 1.91$ eV. Both the slopes of $C_{\rm tot}$ versus $\ln(1/\omega)$ and $G_{\rm tot}$ versus ω are sensitive to the border trap density $N_{\rm bt}$. By choosing a single fitting parameter $N_{\rm bt} = 4.5 \times 10^{19}$cm^{-3}eV^{-1}, good agreement is achieved between the model and the measured $C_{\rm tot}$, $G_{\rm tot}$ data over 1 kHz–1 MHz in Fig. 5(a) and (b). The parameter τ_0 has little effect on the $C_{\rm tot}$, $G_{\rm tot}$ slopes until $\omega\tau_0 \to 1$ [Fig. 4(b)] which is much beyond 1 MHz.

In conclusion, a distributed border trap model based on tunneling between the semiconductor and trap states in the gate insulator is developed. It differs fundamentally from the conventional interface state model in that there is a wide frequency spectrum of border trap response at a given gate bias. The model explains the experimentally observed C–V and G–V dispersion in $Pt/Al_2O_3/n\text{-}In_{0.53}Ga_{0.47}As$ MOS devices. Unlike surface states which are in units of areal density, border traps are characterized by a volume density, extracted from the fitting of capacitance and conductance data.

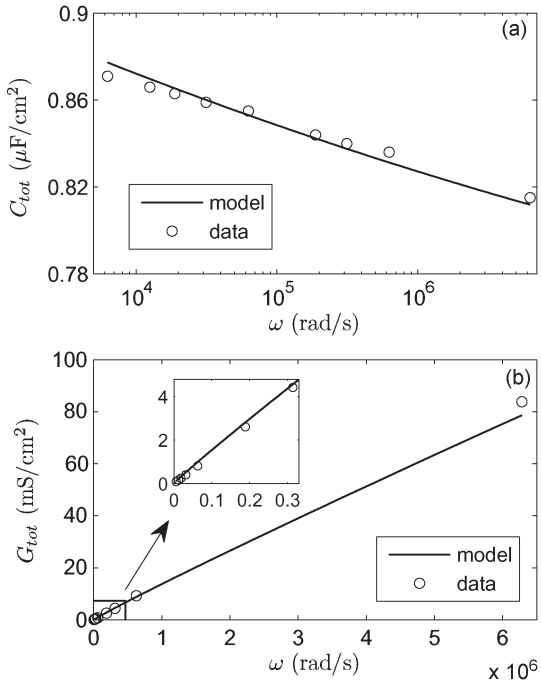

Fig. 5. Experimental (a) $C_{\rm tot}(\omega)$ and (b) $G_{\rm tot}(\omega)$ dispersion data (open circles) at $V_g = 2.9$ V in Fig. 1 compared to those calculated from the distributed border trap model (solid lines). A single border trap density $N_{\rm bt} = 4.5 \times 10^{19}$ cm^{-3}eV^{-1} is assumed in both $C_{\rm tot}(\omega)$ and $G_{\rm tot}(\omega)$ calculations. The rest of the model parameters are $C_{\rm ox} = 1.06$ μF/cm^2, $t_{\rm ox} = 5$ nm, $C_s = 2.8$ μF/cm^2, $\kappa = 5$ nm^{-1}, and $\tau_0 = 2.8 \times 10^{-10}$ s.

References

[1] M. Passlack, R. Droopad, and G. Brammertz, "Suitability study of oxide/gallium arsenide interfaces for MOSFET applications," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 2944–2956, Nov. 2010.

[2] Y. Xuan, Y. Q. Wu, T. Shen, T. Yang, and P. D. Ye, "High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al_2O_3, HfO_2 and HfAlO as gate dielectrics," in *IEDM Tech. Dig.*, 2007, pp. 637–640.

[3] N. Goel, P. Majhi, C. O. Chui, W. Tsai, D. Choi, and J. S. Harris, "InGaAs metal-oxide-semiconductor capacitors with HfO_2 gate dielectric grown by atomic-layer deposition," *Appl. Phys. Lett.*, vol. 89, no. 16, p. 163 517, Oct. 2006.

[4] E. J. Kim, E. Chagarov, J. Cagnon, Y. Yuan, A. C. Kummel, P. M. Asbeck, S. Stemmer, K. C. Saraswat, and P. C. McIntyre, "Atomically abrupt and unpinned $Al_2O_3/In_{0.53}Ga_{0.47}As$ interfaces: Experiment and simulation," *J. Appl. Phys.*, vol. 106, no. 12, p. 124 508, Dec. 2009.

[5] G. Brammertz, K. Martens, S. Sioncke, A. Delabie, M. Caymax, M. Meuris, and M. Heyns, "Characteristic trapping lifetime and capacitance-voltage measurements of GaAs metal-oxide-semiconductor structures," *Appl. Phys. Lett.*, vol. 91, no. 13, p. 133 510, Sep. 2007.

[6] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: Wiley, 1982.

[7] W. Shockley and W. T. Read, Jr., "Statistics of the recombinations of holes and electrons," *Phys. Rev.*, vol. 87, no. 5, pp. 835–842, Sep. 1952.

[8] F. P. Heiman and G. Warfield, "The effects of oxide traps on the MOS capacitance," *IEEE Trans. Electron Devices*, vol. ED-12, no. 4, pp. 167–178, Apr. 1965.

[9] H. Preier, "Contribution of surface states to MOS impedance," *Appl. Phys. Lett.*, vol. 10, no. 12, pp. 361–363, Jun. 1967.

[10] D. S. L. Mui, J. Reed, D. Biswas, and H. Morkoç, "A new circuit model for tunneling related trapping at insulator-semiconductor interfaces in accumulation," *J. Appl. Phys.*, vol. 72, no. 2, pp. 553–558, Jul. 1992.

[11] A. D. Polyanin and V. F. Zaitsev, *Handbook of Exact Solutions for Ordinary Differential Equations*. Boca Raton, FL: CRC Press, 2003.

[12] E. J. Kim, L. Wang, P. M. Asbeck, K. C. Saraswat, and P. C. McIntyre, "Border traps in $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) gate stacks and their passivation by hydrogen anneals," *Appl. Phys. Lett.*, vol. 96, no. 1, p. 012906, Jan. 2010.