InGaAs/InP DHBTs in a planarized, etch-back technology for base contacts

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High performance InP DHBTs are required for developing high speed digital logic and mixed signal circuits which will enable sub-mm wave ICs for imaging, sensing, radio astronomy and spectroscopy applications [1]. Lithographic and epitaxial scaling of key DHBT dimensions to reduce transit and RC charging delays is critical for improved transistor bandwidth. Transit delays can be decreased by reducing the base (T_b) and collector (T_c) thicknesses. However, typical base contact metals - Pd, Ti or Pt diffuse into the base under thermal stress [2], increasing contact resistivity (ρ_c) and thus limiting minimum T_b [3-4]. Hence further base scaling requires non-diffusive metal contacts - W, Mo or Ir which form low ρ_c contacts to highly doped p-InGaAs [5-6]. These metals are blanket deposited by e-beam evaporation and require planarization and etch-back process to prevent any emitter-base short. In this work, for the first time, we have fabricated InP DHBTs using Pd/W base contact metals in a planarized, etch-back process having simultaneous f_τ/f_{max} ~ 410/690 GHz at 220nm wide emitter junction.

For the DHBTs reported here, the InP emitter, InGaAs base and InP collector are 30, 30 and 100 nm thick respectively. Process details for the emitter metal stack and mesa formation are described in [7]. After emitter definition, a thin Pd layer (1.5nm) is blanket deposited by e-beam evaporation followed by a 20 nm sputtered W deposition to form the base contact. The W deposition is conformal, hence to prevent base-emitter short-circuits, W is etched from the sides of the emitter using a photo-resist planarization and etch-back technique [8]. Ti/Au pads for the base were lifted-off to reduce base metal resistance. Devices are isolated by dry etching Pd and W in the field using a SiN_x hard mask. Remainder of the process is as in [7].

Emitter access resistance ρ_{ex} = 6 Ω-μm^2 was extracted from RF data. HBTs with an emitter area A_{je} = 0.22 × 5.7 μm^2, have peak β = 26, with common emitter breakdown voltage $V_{BR,CEO}$ = 2.4 V (J_e = 10 μA/cm^2). Kirk effect is observed at J_e = 21 mA/μm^2 where the f_τ falls to 95% of its peak value. 1-67 GHz measurements of HBTs were carried out after performing a standard line-reflect-reflect-match (LRRM) calibration on an Agilent E8361A PNA, bringing the reference planes to the probe tips. On wafer, short and open circuit pad structures identical to those used by the devices were measured after calibration to de-embed associated transistor pad parasitics from device measurements. Peak RF performance was obtained at I_c = 22.4 mA and V_{ce} = 1.67 V (J_e = 17.9 mA/μm^2, P = 29.9 mW/μm^2). Extrapolations from single pole fit indicate f_τ = 410 GHz and f_{max} = 690 GHz.

In this process, we have used Pd/W contacts for achieving low ρ_c. However, the technique is readily extended to incorporate any low resistivity, refractory base ohmic in a DHBT process flow. This will lead to further improvement in transistor performance.

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T(nm)	Material	Doping (cm^{-3})	Description
10	$In_{0.53}Ga_{0.47}As$	> $5\cdot10^{19}$: Si	Emitter Cap
15	InP	$5\cdot10^{19}$: Si	Emitter
15	InP	$2\cdot10^{18}$: Si	Emitter
30	InGaAs	$9\text{-}5\cdot10^{19}$: C	Base
4.5	$In_{0.53}Ga_{0.47}$ As	$9\cdot10^{16}$: Si	Setback
10.8	$In_{0.53}Ga_{0.47}As$ / $In_{0.52}Al_{0.48}As$	$9\cdot10^{16}$: Si	B-C Grade
3	InP	$6\cdot10^{18}$: Si	Pulse doping
81.7	InP	$9\cdot10^{16}$: Si	Collector
7.5	InP	$1\cdot10^{19}$: Si	Sub Collector
7.5	$In_{0.53}Ga_{0.47}$ As	$4\cdot10^{19}$: Si	Sub Collector
300	InP	$2\cdot10^{19}$: Si	Sub Collector
~625,000	InP	SI	Substrate

Table 1. DHBT layer structure

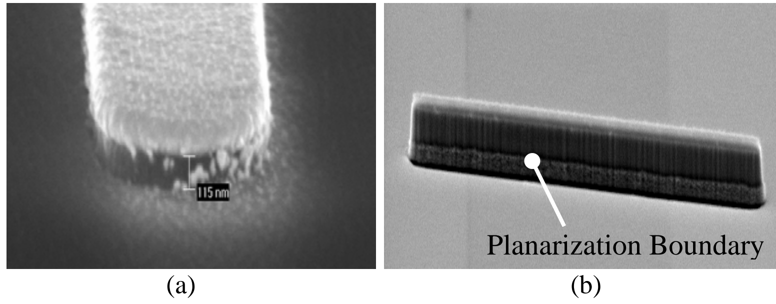

Fig 1. SEMs of the emitter during planarization and etch-back steps (a) Emitter projecting from PR during planarization; (b) Emitter after W etch back showing the planarization boundary

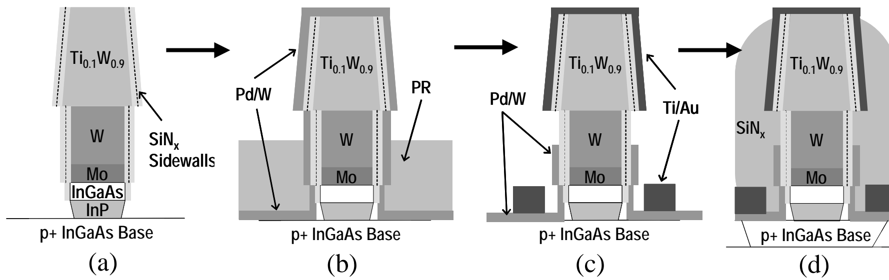

Fig 2. Base process flow - (a) Emitter metal stack and mesa formation; (b) Blanket Pd/W deposition, PR planarization; (c) W etch from the sides of emitter and Ti/Au pad lift-off; (d) Base mesa formed by dry etching Pd/W in the field and wet etch of base semiconductor using SiN_x hard mask

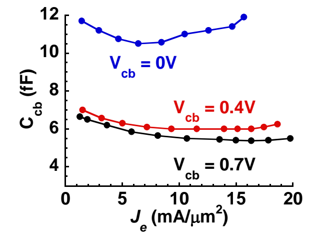

Fig 3. Variation in C_{cb} with V_{cb} and J_e; C_{cb} is extracted from Y_{12} at 5 GHz

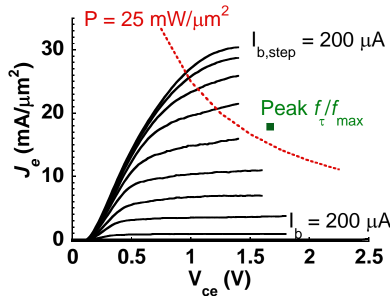

Fig 4. DHBT Common-Emitter *I-V* characteristics; $A_{je} = 0.22 \times 5.7\ \mu m^2$

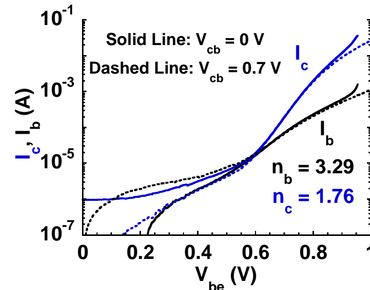

Fig 5. Gummel Plot of DHBT with $A_{je} = 0.22 \times 5.7\ \mu m^2$

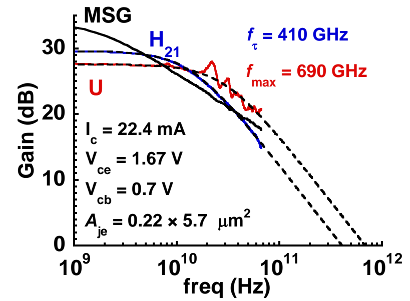

Fig 6. Measured RF gains for the DHBT in 1 - 67 GHz band

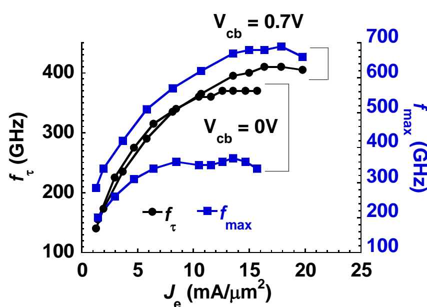

Fig 7. f_τ/f_{max} dependence on V_{cb} and J_e

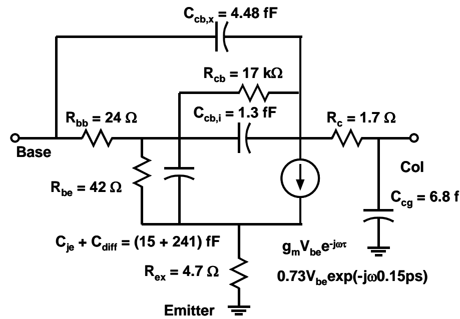

Fig 8. Hybrid-π equivalent circuit at peak RF performance derived from 1 – 67 GHz RF data

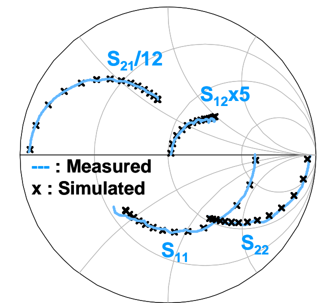

Fig 9. 1 - 67 GHz measured and simulated S-Parameters from equivalent circuit model in Fig 8