InGaAs/InP DHBTs demonstrating simultaneous f_τ/f_{max} ~ 460/850 GHz in a refractory emitter process

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Abstract

We report InP/$In_{0.53}Ga_{0.47}As$/InP double heterojunction bipolar transistors (DHBTs) demonstrating simultaneous 460 GHz f_τ and 850 GHz f_{max}. The devices were fabricated using a triple mesa process with dry-etched, refractory metals for emitter contact formation. The devices incorporate a 35 nm thick InP emitter which enables a wet etch emitter process demonstrating 220 nm wide emitter-base junctions with less than 10 nm undercut in the emitter semiconductor below emitter metal. This reduces the gap between base metal contact and emitter semiconductor causing significant reduction in emitter-base gap resistance (R_{gap}) component of the total base access resistance (R_{bb}), leading to an increase in observed f_{max}. At peak RF performance, the device is operating at 32 mW/μm^2 with J_e = 19.4 mA/μm^2 and V_{ce} = 1.66 V. The devices show a DC common emitter current gain (β) ~ 20 and $V_{BR,CEO}$ = 3.7 V.

I. Introduction

High bandwidth DHBTs have potential applications in 0.3-1.0 THz ICs for imaging, sensing, radio astronomy and spectroscopy, in high-resolution 2-20 GHz mixed-signal ICs, and in 100-500 GHz digital logic [1]-[4]. Lithographic and epitaxial scaling of critical DHBT dimensions is required for improved device performance. Specific challenges that exist in addition to scaling device junction areas include reduction in emitter and base contact resistivity and reliable operation of transistors at high current density set by the Kirk-effect limit.

HBT bandwidth is increased by thinning the base (T_b) and collector layers (T_c) to reduce transit times, and by decreasing junction widths and ohmic contact resistivities to reduce RC charging times. Reduction in T_c also increases the current density J_e at the Kirk-effect limit $J_{kirk} \sim T_c^{-2}$; increasing the device transconductance (g_m) and reducing the small-signal ($C_{cb}kT/qI$) and logic ($C_{cb}\Delta V/I$) delays. Reduction in device dimensions also helps in reducing the base spreading resistance and the device thermal resistance, accommodating the increased J_e.

In this work, we have used molybdenum (Mo) based refractory ohmic contacts to permit device operation at high current density without problems of electromigration or contact degradation [5]. Given highly stressed refractory contact metal layers used for emitter metal stack, narrow emitter contacts readily lose adhesion to the emitter semiconductor during processing, resulting in zero fabrication yield for sub-200 nm features. A W/TiW emitter metal stack optimized for low stress and a double sidewall process were used in this work, which permits fabrication of HBTs having 220 nm wide emitter-base junctions.

Prior to this work, InP DHBTs having greater than 800 GHz f_{max} have been reported [6]-[8] but with lower f_τ than this work. The HBTs here reported demonstrate a simultaneous 460 GHz f_τ and 850 GHz f_{max}.

II. Growth, Design and Fabrication

The epitaxial structure (Table I) was grown on a 4" semi-insulating InP substrate by IQE. The emitter design includes a 10 nm highly doped n-$In_{0.53}Ga_{0.47}As$ cap (N_d > 5 × 10^{19} cm^{-3}), 20 nm 5 × 10^{19} cm^{-3} doped InP layer and 15 nm 2 × 10^{18} cm^{-3} doped InP depletion layer. The InGaAs base is 30 nm thick having a 9 – 5 × 10^{19} cm^{-3} doping gradient. InP collector is 100 nm thick and doped at 5 × 10^{16} cm^{-3}. The base-collector grade includes a 13.5 nm InGaAs setback, a 16.5 nm InGaAs/InAlAs chirped-superlattice grade [9] and an InP pulse doping.

DHBTs were fabricated using a wet-etch triple mesa process. Emitter contacts were formed by blanket e-beam evaporation of 20 nm Mo. Sample surface preparation techniques prior to emitter metal deposition for obtaining low contact resistivity are described in [10]. A W/TiW (10% Ti by weight) metal stack ~ 200/300 nm thick was then blanket sputter deposited using Ar plasma under conditions giving < 100 MPa stress. Emitter contact patterns were then defined by E-beam lithography and the metal stack was etched in an SF_6/Ar ICP using Cr etch mask. The etch conditions were optimized to obtain an almost vertical emitter profile with undercut at the W/TiW interface which acted as the shadow mask for lifted-off base contacts. A 20 nm SiN_x sidewall is deposited, the InGaAs cap wet-etched and a second 30 nm SiN_x sidewall formed. The InP emitter is then wet-etched in a selective chemistry to stop on the InGaAs base. Wet etch of the thin InP

T (nm)	Material	Doping (cm^{-3})	Description
10	$In_{0.53}Ga_{0.47}As$	>5·10¹⁹:Si	Emitter Cap
20	InP	5·10¹⁹:Si	Emitter
15	InP	2 ·10¹⁸:Si	Emitter
30	InGaAs	9-5 ·10¹⁹:C	Base
13.5	$In_{0.53}Ga_{0.47}As$	5 ·10¹⁶:Si	SetBack
16.5	$In_{0.53}Ga_{0.47}As$/ $In_{0.52}Al_{0.48}As$	5 ·10¹⁶:Si	B-C Grade
3	InP	3.6·10¹⁸:Si	Pulse Doping
67	InP	5 ·10¹⁶:Si	Collector
7.5	InP	2 ·10¹⁹:Si	Sub-Collector
5	$In_{0.53}Ga_{0.47}As$	4 ·10¹⁹:Si	Sub-Collector
300	InP	2 ·10¹⁹:Si	Sub-Collector
Substrate	InP	SI	

Table 1. DHBT layer structure

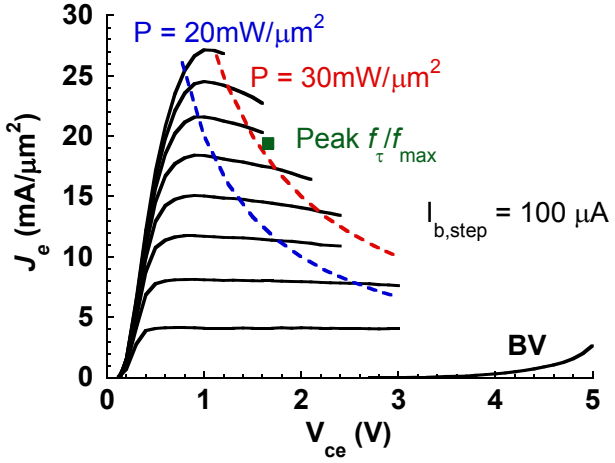

Figure 1. Common-Emitter current-voltage (J_e-V) characteristics of a DHBT with A_{je} = 0.22 × 2.7 μm²

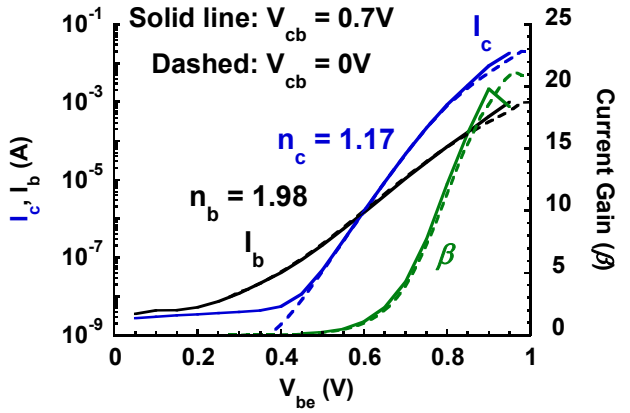

Figure 2. Gummel plot of a DHBT with A_{je} = 0.22 × 3.7 μm²

emitter (35 nm) produces very small undercut below the emitter metal resulting in only ~ 10 nm spacing between the emitter mesa and base contact. This greatly reduces the emitter-base gap resistance (R_{gap}) component of the base access resistance (R_{bb}), thereby improving f_{max}. Base and collector contacts are formed by metal lift-off – Pt/Ti/Pd/Au for base and Ti/Pd/Au for collector contact. Selective wet etches are employed for base and collector mesa definitions and for device isolation. Devices are passivated with benzocyclobutene (BCB) and planarized for contact to metal pads for measurements.

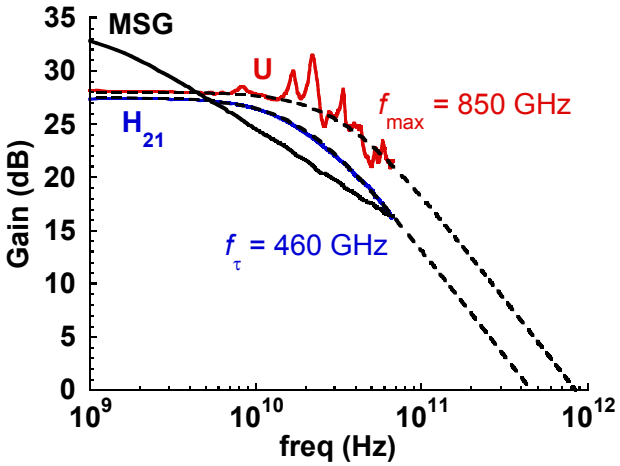

Figure 3. Measured RF gains for peak f_τ / f_{max} for the DHBT in 1 - 67 GHz band using off-wafer LRRM in a lumped pad structure. The DHBT was biased at I_c = 11.5 mA, V_{ce} = 1.66 V, V_{cb} = 0.7 V

III. Measurements and Results

Transmission line model (TLM) measurements show base R_{sh} = 710 Ω/sq and ρ_c < 5 Ω-μm² and collector R_{sh} = 15 Ω/sq and ρ_c = 22 Ω-μm². Higher than expected R_{sh} and ρ_c for the collector has been observed compared to previous designs [7] presumably due to thinner InGaAs subcollector layer. Total emitter access resistivity ρ_{ex} < 4 Ω-μm² was extracted from RF data. HBTs with an emitter base junction width of 220 nm show peak DC common emitter current gain β = 20, with common emitter breakdown voltage $V_{BR,CEO}$ = 3.7 V (J_e = 0.1 mA/μm²). Common emitter current-voltage curves and Gummel characteristics of the HBTs are shown in Fig 1 and Fig 2 respectively.

1-67 GHz measurements of HBTs embedded in a ground-signal-ground pad structure were carried out after performing a standard line-reflect-reflect-match (LRRM) calibration on an Agilent E8361A PNA, bringing the reference planes to the probe tips. On wafer, short and open circuit pad structures identical to those used by the devices were measured after calibration to de-embed associated transistor pad parasitics from device measurements [11]. Peak RF performance was obtained at I_c = 11.5 mA and V_{ce} = 1.66 V (V_{cb} = 0.7 V, J_c = 19.4 mA/μm², P = 32 mW/μm², C_{cb}/I_c = 0.38 psec/V). Extrapolations from single-pole fit to the measured current gain H_{21} and Mason's Unilateral gain U indicate cut off frequencies f_τ = 460 GHz and f_{max} = 850 GHz (Fig 3).

Variations in f_τ, f_{max} and extracted C_{cb} with J_e and base-collector voltage (V_{cb}) are shown in Figs 4, 5 and 6. A small-signal hybrid-pi equivalent circuit [12] extracted from the RF data of Fig 3 is shown in Fig 7. Fig 8 compares the measured S-parameters of Fig 3 to simulated

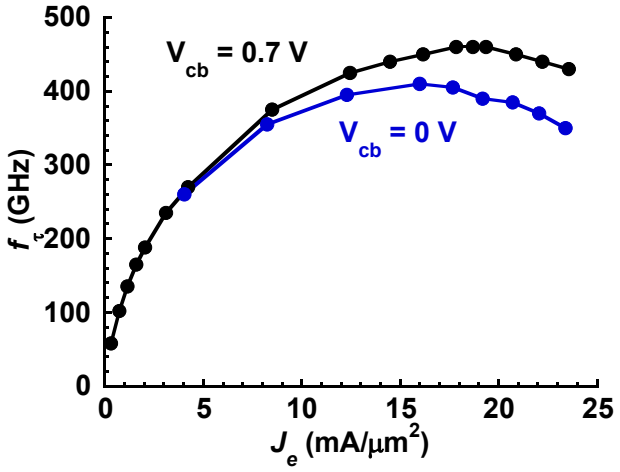

Figure 4. f_τ dependence on V_{cb} and J_e for the reported DHBT

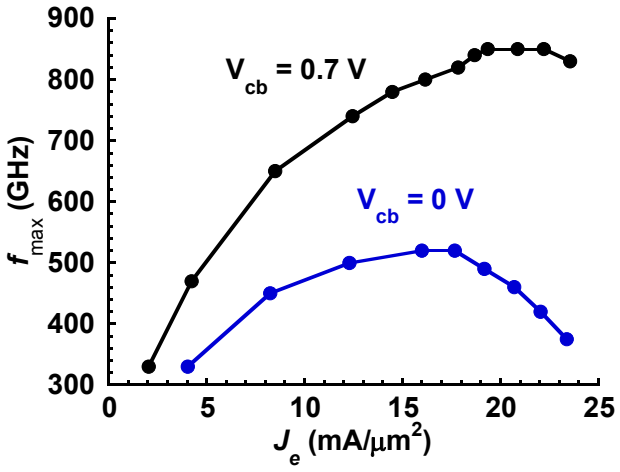

Figure 5. f_{max} dependence on V_{cb} and J_e for the reported DHBT

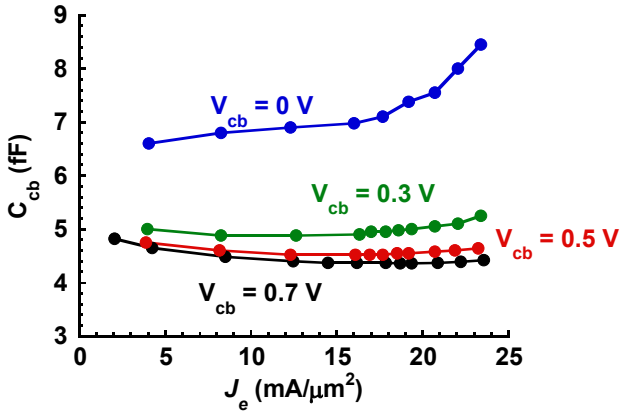

Figure 6. C_{cb} dependence on V_{cb} and J_e for the reported DHBT. C_{cb} was extracted from Y_{12} at 5 GHz

S-parameters from hybrid-π model of Fig 7. The Kirk effect is observed at J_e = 23 mA/μm^2 (V_{cb} = 0.7 V) when f_τ falls to 95% of its peak value.

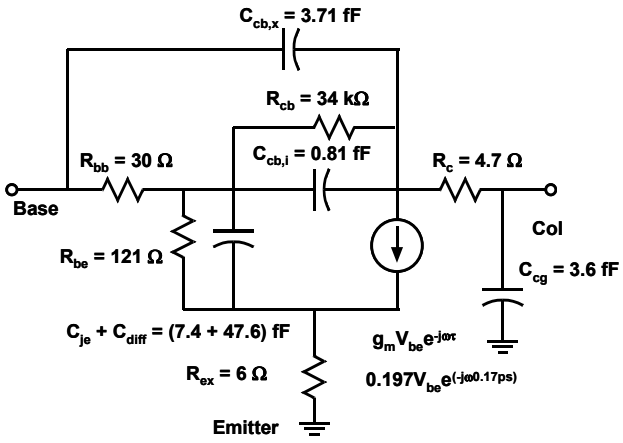

Figure 7. Hybrid-π equivalent circuit at peak RF performance of Fig 3

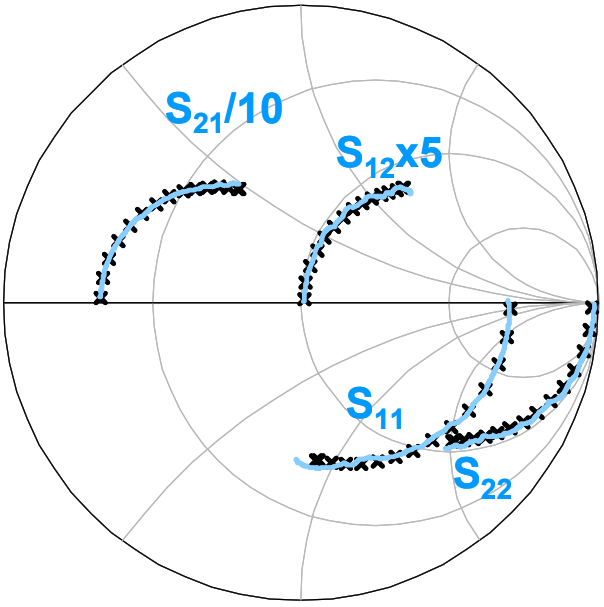

Figure 8. Comparison of measured S-parameters of Fig. 3 (Solid line) and simulated S-parameters (x) from model of Fig. 7 from 1-67 GHz

IV. Conclusion

InP DHBTs having simultaneous 460 GHz f_τ and 850 GHz f_{max} have been demonstrated. The thin emitter design and all wet-etch process results in small undercut below the contact metal, permitting fabrication of narrow emitter junctions. High f_{max} has been achieved through reduced R_{bb} by reduced spacing between the emitter mesa and base contact. Reduced junction sizes and emitter access resistivity have resulted in improved f_τ. Further reduction in emitter and base access resistances and reduction in C_{cb} by decreasing the base contact width, emitter width and sidewall thickness should lead to improvement in device performance.

Acknowledgements

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