Gate first $In_{0.53}Ga_{0.47}As/Al_2O_3$ MOSFETs with in-situ channel surface cleaning

Andrew D. Carter, Jeremy J. M. Law, William Mitchell, Gregory J. Burek,
Brian J. Thibeault, Arthur C. Gossard, Mark. J. W. Rodwell

As scaling of critical dimensions in VLSI becomes difficult, alternatives to silicon are being examined. III-V MOSFETs may provide larger drive currents than silicon at the same equivalent dielectric thickness [1], absent dielectric interfacial defect densities, D_{it}, which degrade subthreshold slope and drive current. While low D_{it} for HfO_2 on InGaAs has been reported [2], this result used an arsenic cap to protect the semiconductor surface from oxidation during the transfer between the wafer growth system and the dielectric deposition tool. We have demonstrated D_{it} similar to [2] cleaning the InGaAs surface with hydrogen and trimethylaluminum (TMA) before Al_2O_3 deposition [3]. This could eliminate the need for an arsenic cap. Here we report first MOSFET results using such channel surface cleaning techniques.

An ~5.5 nm Al_2O_3 film was grown in an FlexAL ALD at 300 °C using TMA and deionized water as reactants. We performed an in-situ surface preparation on air exposed samples with iterative cycles of hydrogen plasma and TMA. Hydrogen removes native oxides on the channel surface [4]. Interface quality was measured by capacitance-voltage (CV) on 300 nm, 1E17 cm^{-3} Si-doped n-type InGaAs surfaces. Gate stack deposition may degrade semiconductor-oxide interface properties [5]. Measurements were done on not annealed and annealed tungsten CV dots to determine damage done by gate metal and SiO_2 deposition.

Transistor material was grown lattice matched on InP by MBE with the following layer structure: semi-insulating InP substrate, 400 nm undoped InAlAs, 3 nm InAlAs (1E19 cm^{-3} and 3E19 cm^{-3} Si doped n-type), and 10 nm undoped InGaAs. Blanket depositions of W/Cr/SiO2/Cr and subsequent photolithography define a gate stack that is etched by RIE, followed by PECVD SiN_x sidewall deposition and quasi-MEE InAs source-drain regrowth [6]. Finally, devices were metallized using lifted-off Ti/Pd/Au and wet etch mesa isolated.

The performance of the depletion mode device (3E19 cm^{-3} doping) was comparable to the previous enhancement mode result [6] which utilized arsenic capped material to prevent surface oxidation. The enhancement mode device (1E19 cm^{-3} doping) has a reduced current density and transconductance which are due to large series access resistance underneath the sidewalls. For the depletion mode device, series access resistance to the channel does not explain the poor extrinsic transconductance. Future work will include smaller gate lengths and thinner sidewalls.

[1] M.J.W. Rodwell et al, Device Research Conference 2010.
[2] R. Engel-Herbert et al, J. Appl. Phys. **108**, 124101 (2010).
[3] A.D. Carter et al, Appl. Phys. Express, to be submitted.
[4] E. J. Petit et al, J. Vac. Sci. Technol. B **12**, 547 (1994).
[5] X. Cao et al, J. Vac. Sci. Technol. B **23**, 3138 (2005).
[6] U. Singisetti et al, IEEE Electron Device Lett. **30**, 1128–1130 (2009).

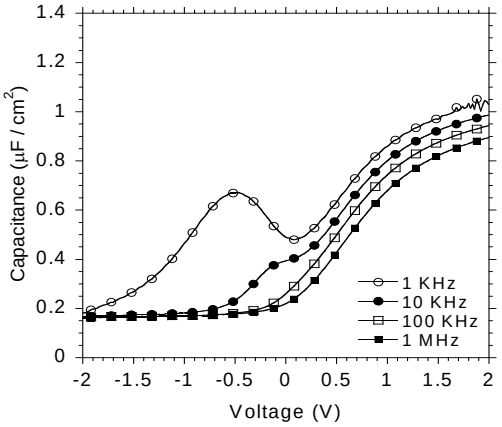

Figure 1: CV curve of not annealed Al_2O_3 with a thermally evaporated nickel contact.

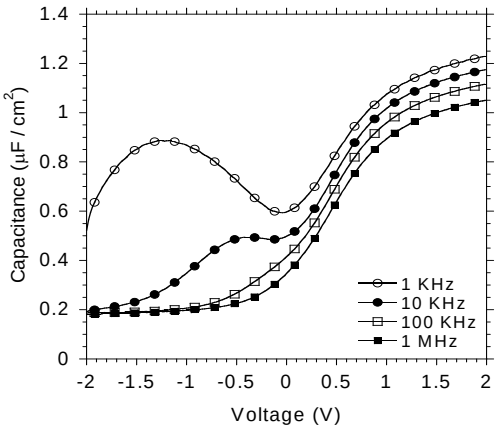

Figure 2: CV curve of not annealed Al_2O_3 with a sputtered tungsten contact.

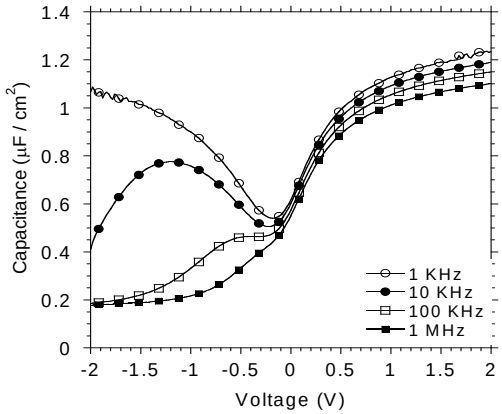

Figure 3: CV curve of 500 °C annealed Al_2O_3 with a sputtered tungsten contact. The sample was coated in SiO_2 prior to annealing.

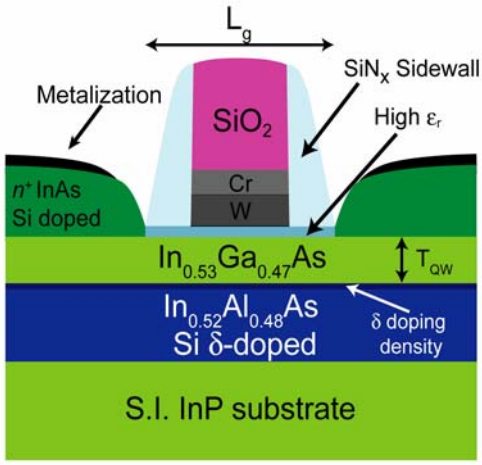

Figure 4: Cartoon schematic of transistor in cross section.

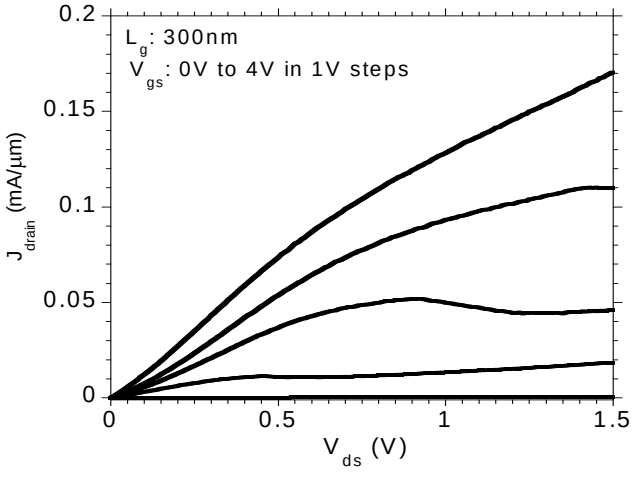

Figure 5: Drain current versus gate voltage for the enhancement mode device. Apparent negative resistance due to poorly controlled RF impedance termination.

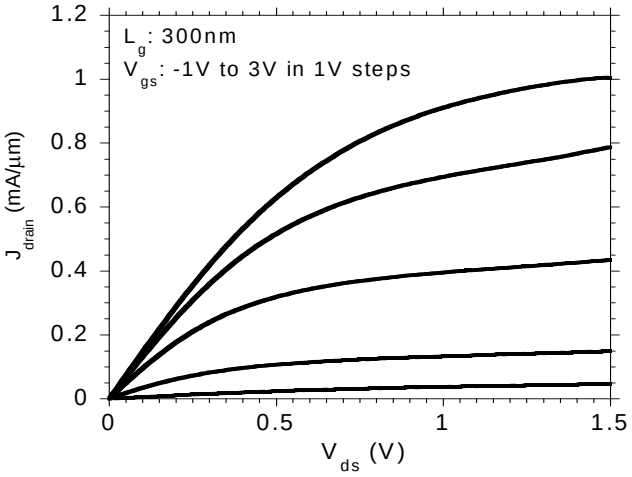

Figure 6: Drain current versus gate voltage for the depletion mode device.