Gate first $In_{0.53}Ga_{0.47}As/Al_2O_3$ MOSFETs with in-situ channel surface cleaning

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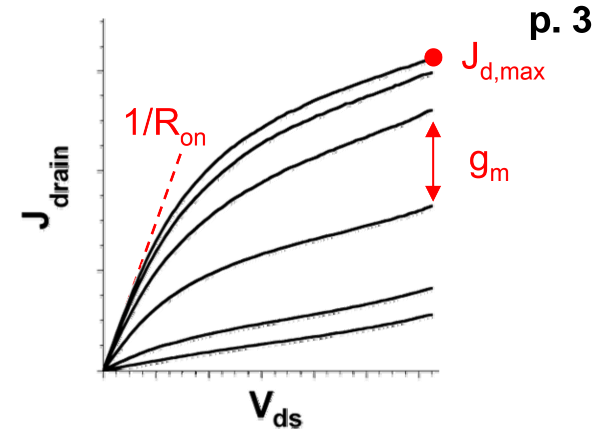
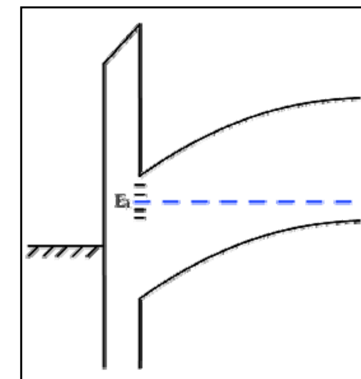
Overview

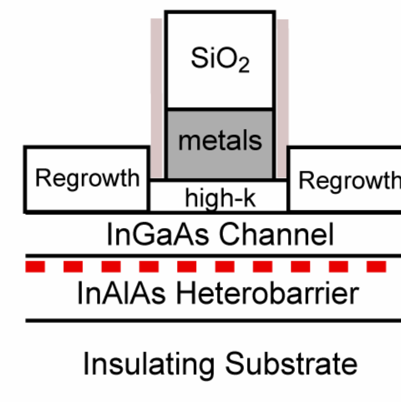
- Why III-V MOSFETs?
- Device Physics
- Device Processing
  - ALD Al_2O_3 with D_{it} passivation
  - Transistor processing
- Measurements
- Conclusions

Why III-V VLSI?

- Higher electron velocities than Si MOS
  - For short L_g FETs, $J_{drain} = q \cdot n_{s,channel} \cdot v_{sat}$
  - Transconductance, $g_m = C_{effective} \cdot v_{sat}$
  - J_d and g_m are key figures of merit in VLSI
- However:
  - J_d and g_m degraded by source large R_{access}
  - J_d and g_m degraded by interface trap density, D_{it}
- **Therefore, we must develop:**
  - **Low access resistance source/drain contacts**
  - **Thin, high-k, low D_{it} dielectrics on InGaAs**
  - **Fully self-aligned process modules**







*MOSFETs have been, and always will be, a **materials challenge**.*

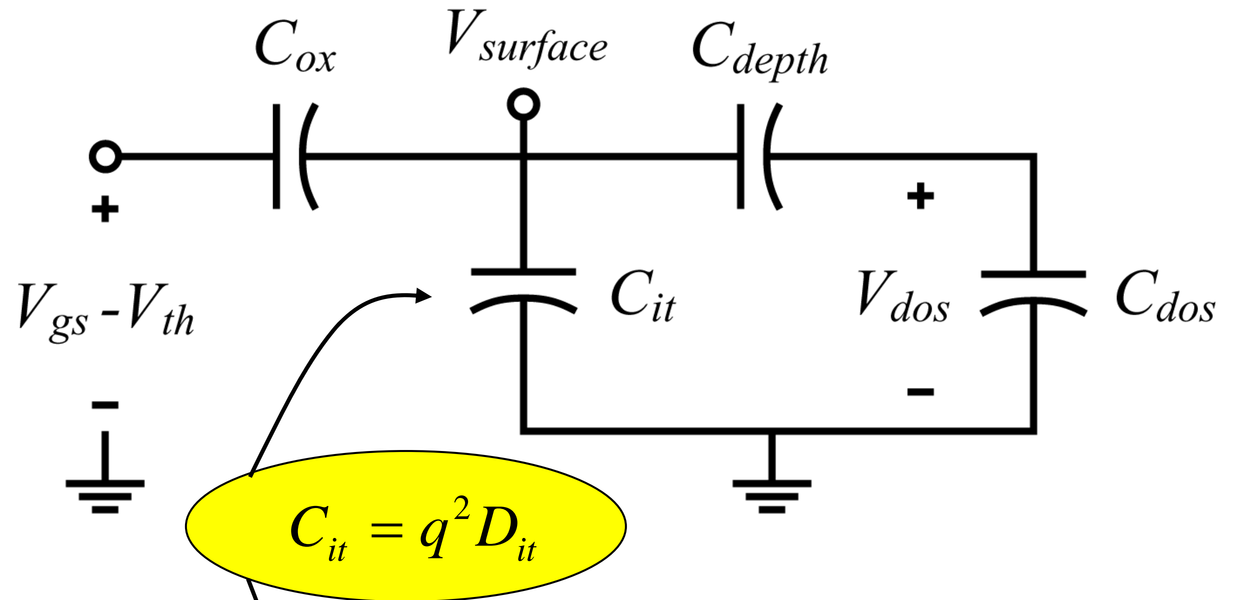
FET Device Physics

$$C_{ox} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}}$$

$$C_{depth} \approx \frac{\varepsilon_o \varepsilon_{channel}}{t_{channel}/2}$$

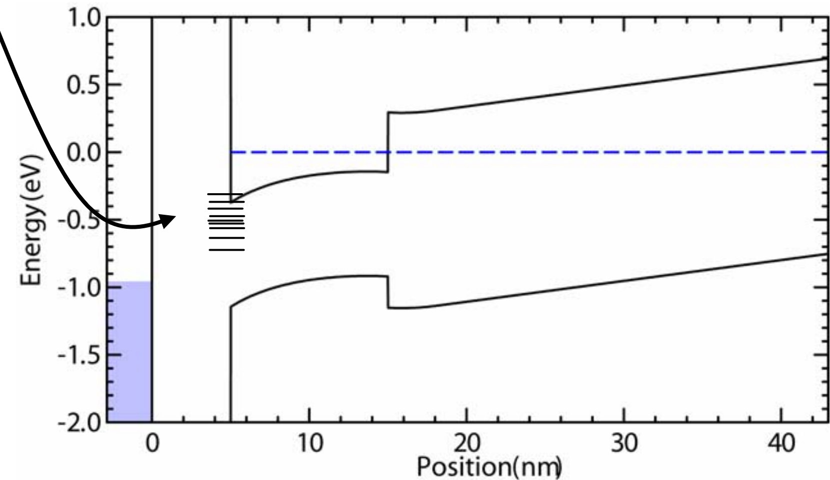
$$C_{dos} = \frac{q^2 g m^*}{\pi \hbar^2}$$

$$n_{channel} = \frac{C_{dos}}{q}(V_{dos})$$



D_{it} problem

- $\uparrow C_{it}$, $\downarrow V_{surface}$
- $V_{surface}$ also supplies C_{dos}
- $\downarrow V_{surface} = \downarrow n_{chan}$ in C_{dos}



Electron band diagram of a quantum well FET

III-V D_{it} Passivation

- Multiple ways to passivate the D_{it} on compound semiconductors
  - Sulfur passivation, e.g. $(NH_4)_2S$ [1]
  - GdGaO based dielectrics [2]
  - *In-situ* dielectric growth after epitaxial growth [3]
  - Arsenic capping for *ex-situ* dielectric growth [4]
- However, these techniques restrict process flow choices
  - Wet treatment → *ex-situ* surface oxide formation
  - *In-situ* deposition → gate first process flow only
  - Lack of portability to higher-k dielectrics for scaling

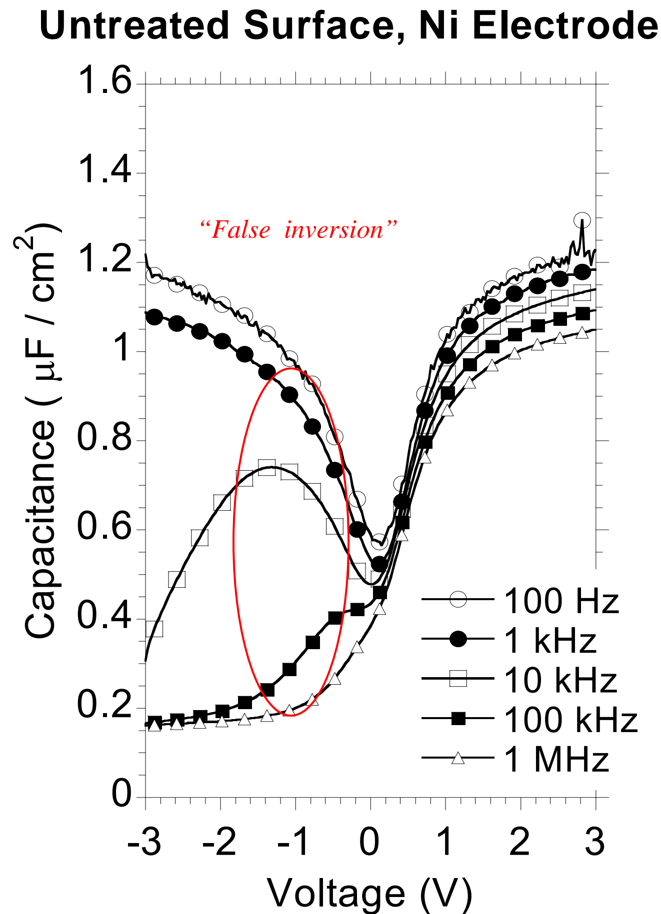
[1] Y.Q. Wu et. al, IEDM 2009
[2] *M.*Passlack et al, JVST B 2005
[3] Cheng et al, APL 2010
[4] Y. Hwang et al, APL 2011

III-V D_{it} Passivation

Cyclic hydrogen plasma / TMA treatments before dielectric growth

→ D_{it} passivation immediately prior to Al_2O_3 growth under vacuum

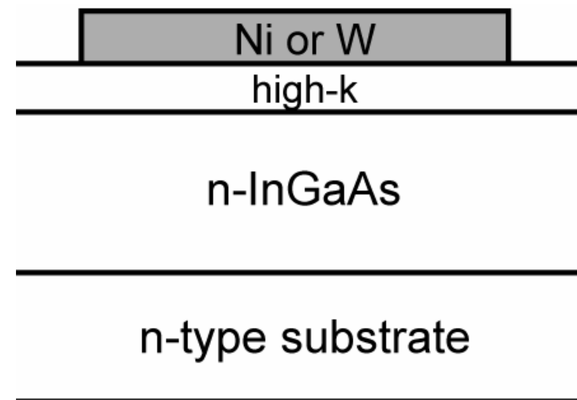
→ Gate first or gate last process flow compatibility



"False inversion" peak at negative bias

→ Surface trap response

Quantitative D_{it} information can be calculated from the conductance method*



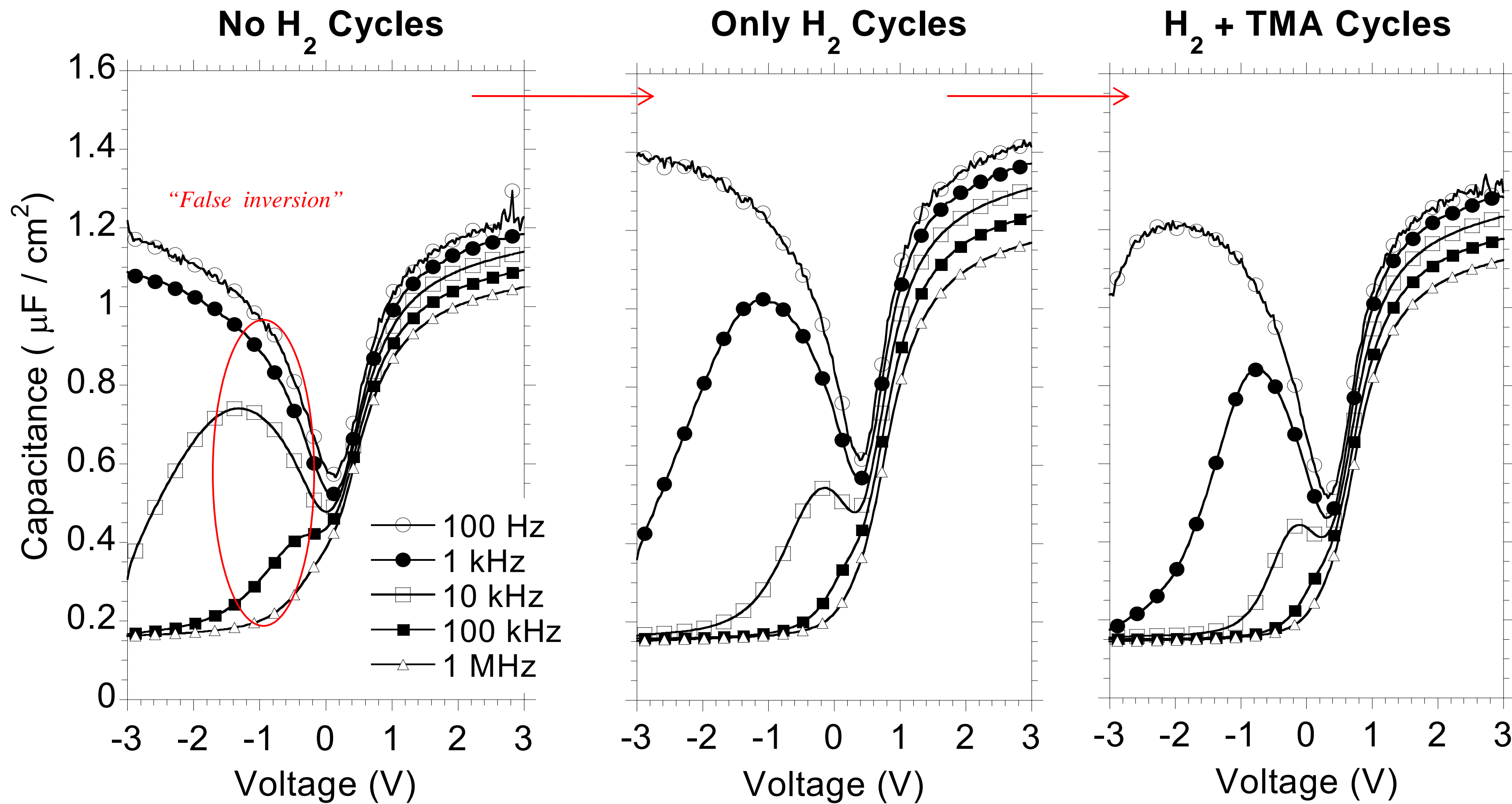
MOSCAP Structure

A.D. Carter et al, APEX, Submitted.

* R. Engel-Herbert et al *JAP 2010.*

III-V D_{it} Passivation

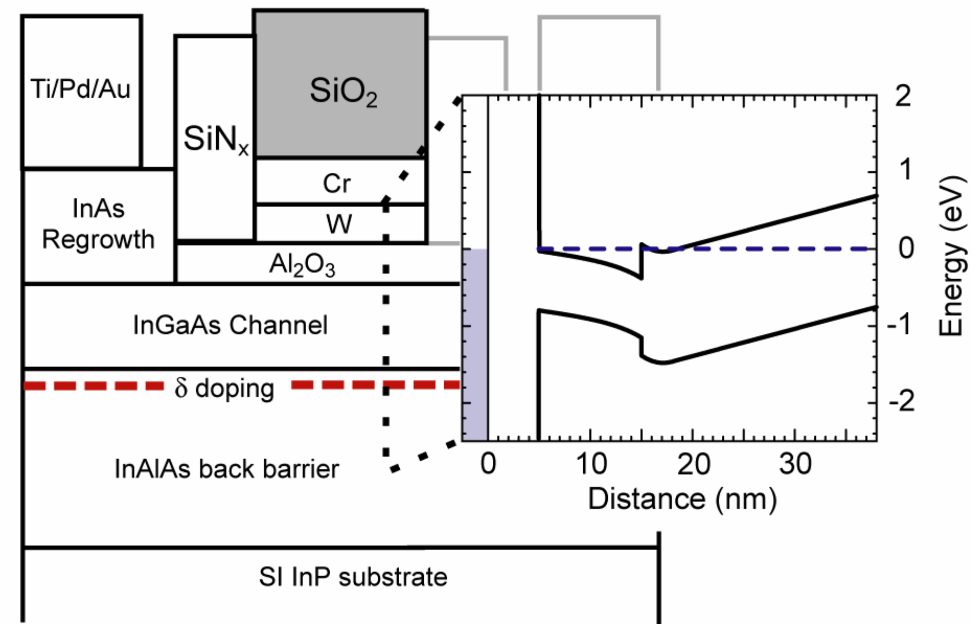
Cyclic hydrogen plasma / TMA treatments before dielectric growth
→ 50 cycle (~5 nm Al_2O_3) growth, 400°C anneal, Ni metallization



A.D. Carter et al, APEX, Submitted.

Gate First FET Process Flow

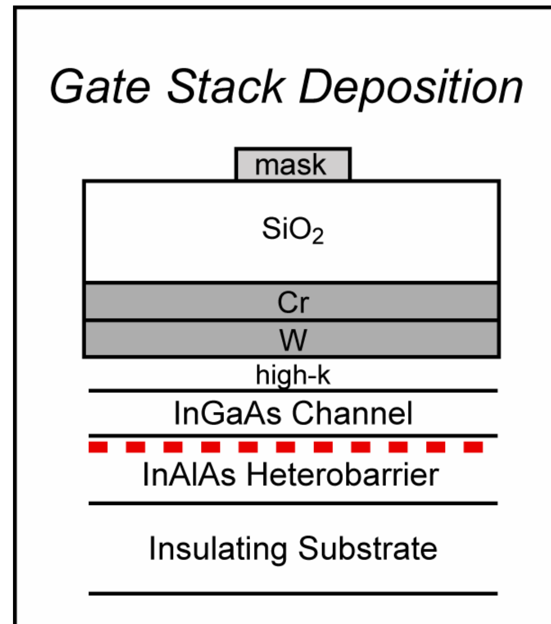
- Thick channel
  - Process damage mitigation
- Heavy δ doping
  - Prevents ungated sidewall current choke
  - Depletion mode: $9x10^{12}$ cm^{-2} Si doping
  - Enhancement mode: $3x10^{12}$ cm^{-2} Si doping
- $In_{0.52}Al_{0.48}As$ heterobarrier
  - Carrier confinement
- Semi-insulating InP
  - Device isolation

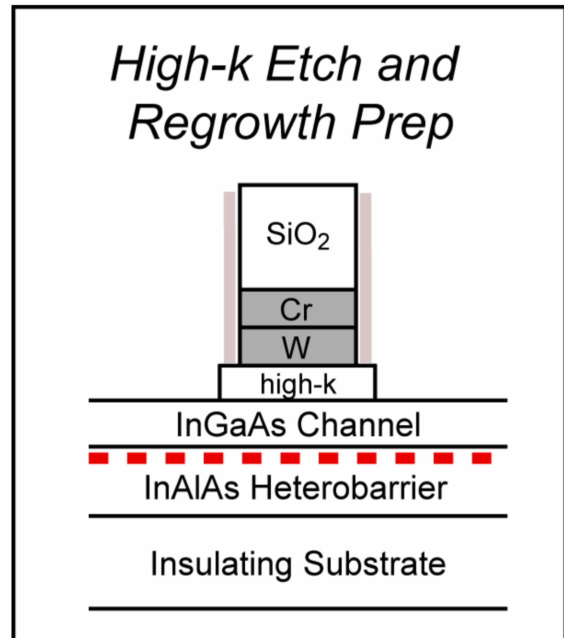


Gate First FET Process Flow

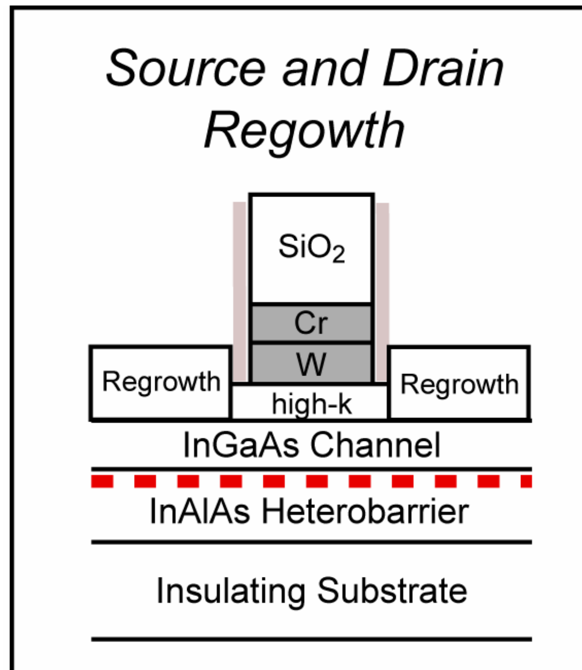
Gate Stack Definition

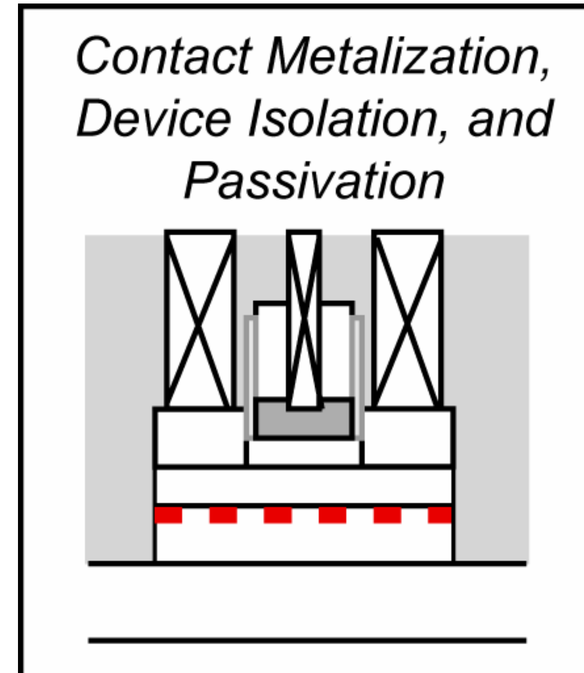
- Hydrogen plasma / TMA treatment before Al_2O_3
- Optical gate lithography + hard mask
- Bi-layer gate
  - Sputtered W + evaporated Cr
  - High selectivity, low power dry etch
- Sidewall Deposition
  - Protects S/D short circuit to gate
- Sidewall etch
- High-k etch
- Surface preparation for regrowth
  - UV O_3 exposure to partially oxide channel
  - Removed *ex-situ* before MBE load



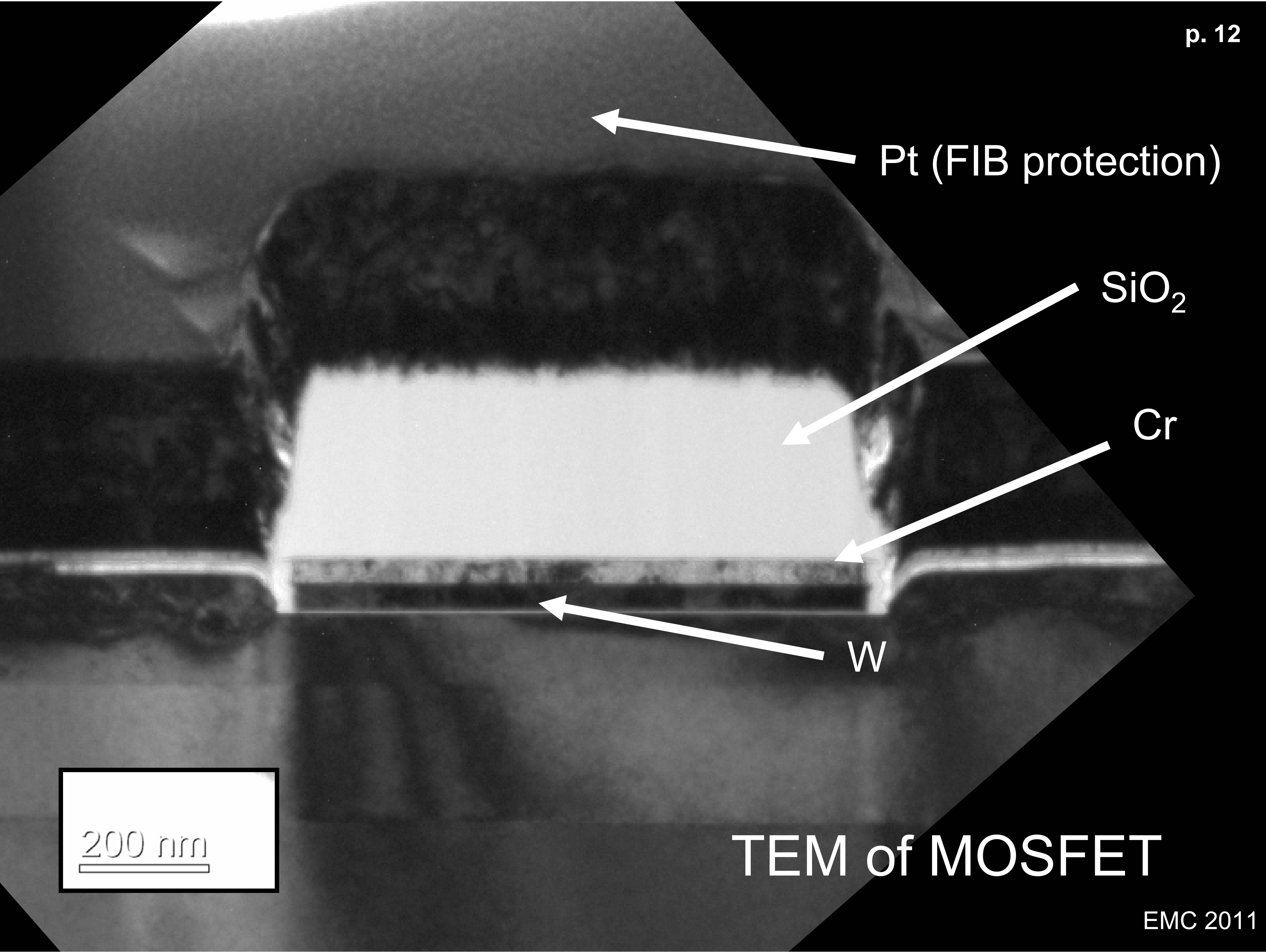


Gate First FET Process Flow

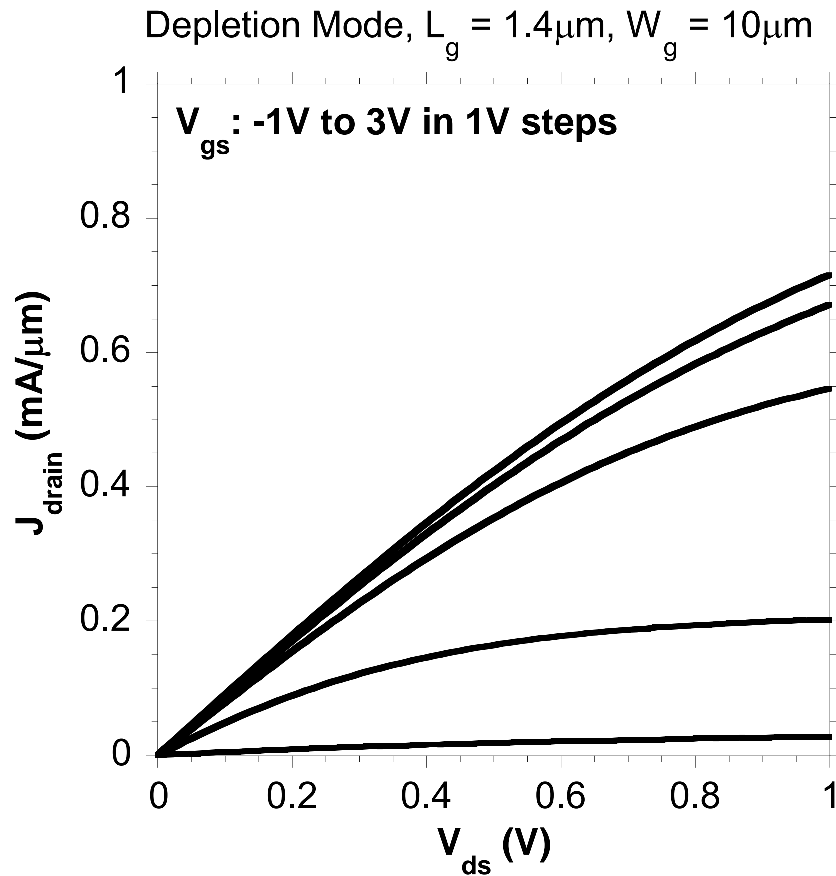


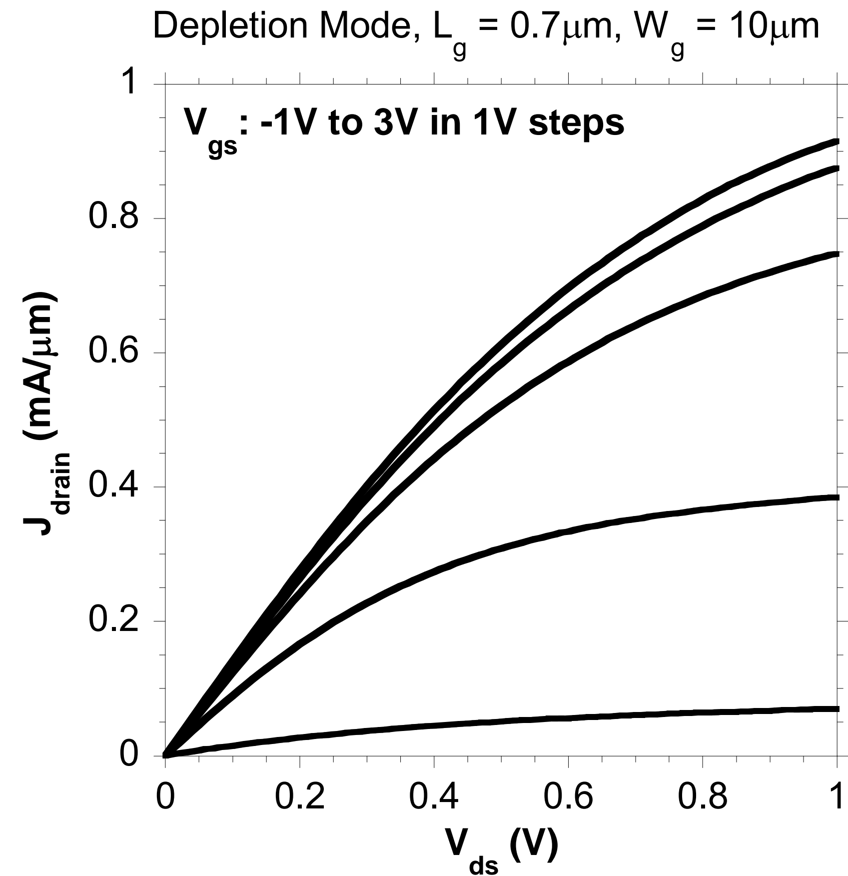


- Regrowth and Back End
  - MBE InAs Regrowth
    - 500°C, low arsenic flux, high temperature → near gate fill in
  - Metallization and Mesa Isolation
    - Ti/Pd/Au liftoff, *in-situ* Mo in MBE optional


Pt (FIB protection)
SiO_2
Cr
W
200 nm
TEM of MOSFET

Gate First D-Mode FET Results

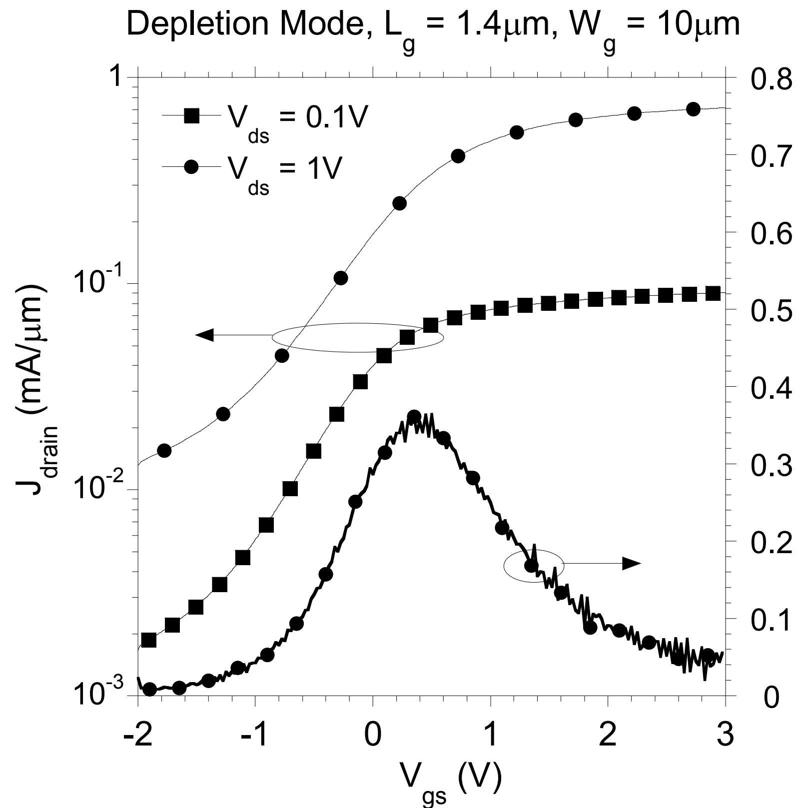


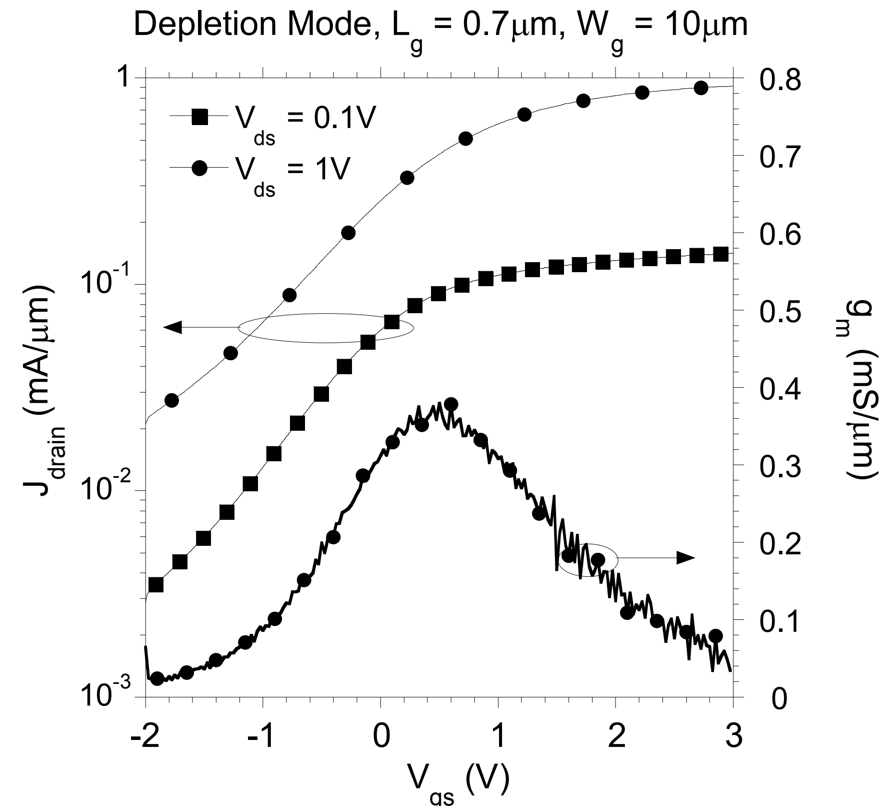


High J_{drain} (~1mA/μm)

Low access resistance from high δ doping

Gate First D-Mode FET Results



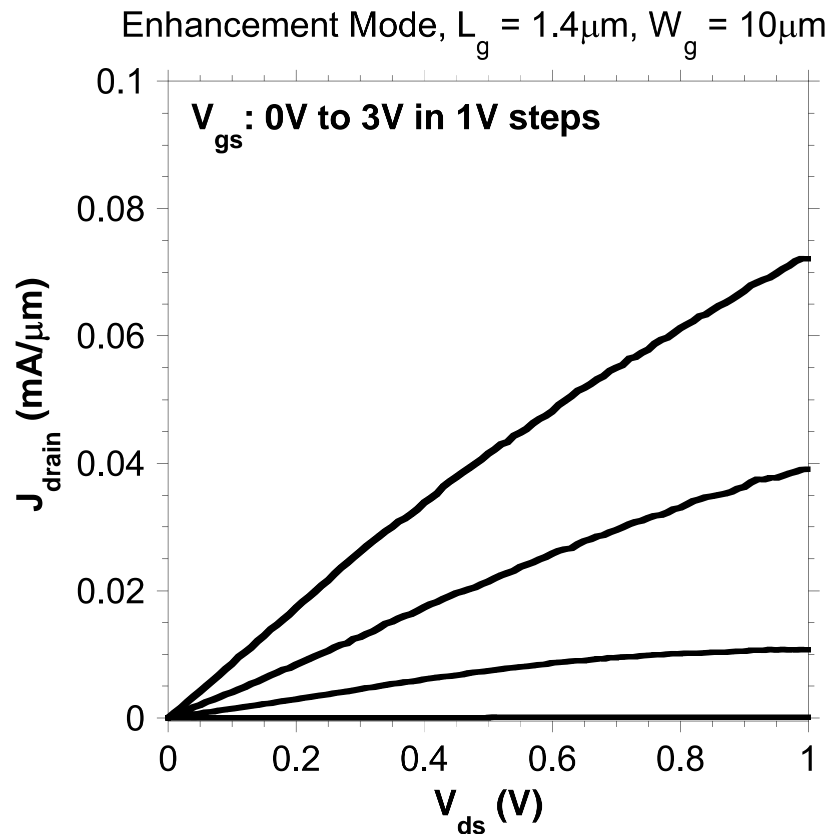


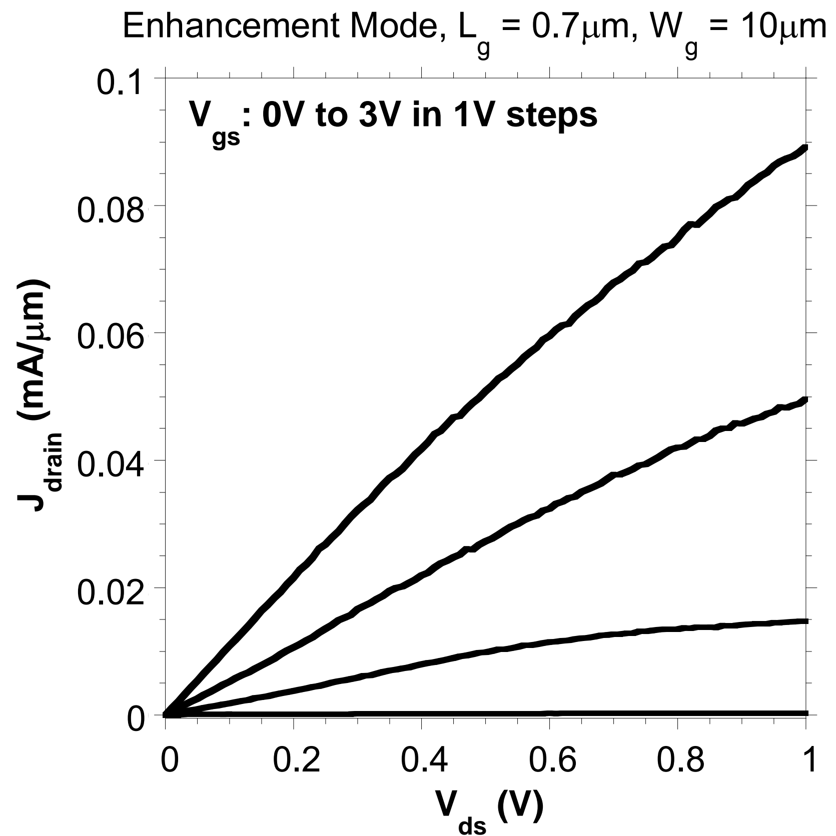
Large DIBL → heavy delta doping

Moderate transconductance (~0.35 mS/μm)

→ Not explained by $$g_{m,extrinsic} = \frac{g_{m,\text{intrinsic}}}{1 + g_{m,\text{intrinsic}} R_s}$$

Gate First E-Mode FET Results

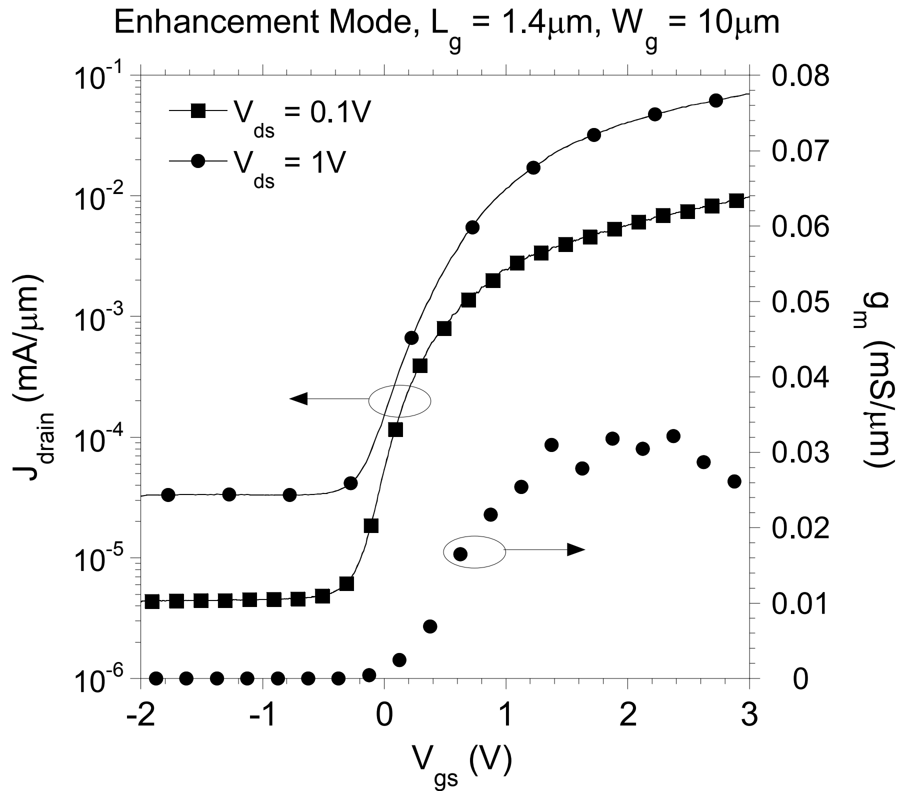


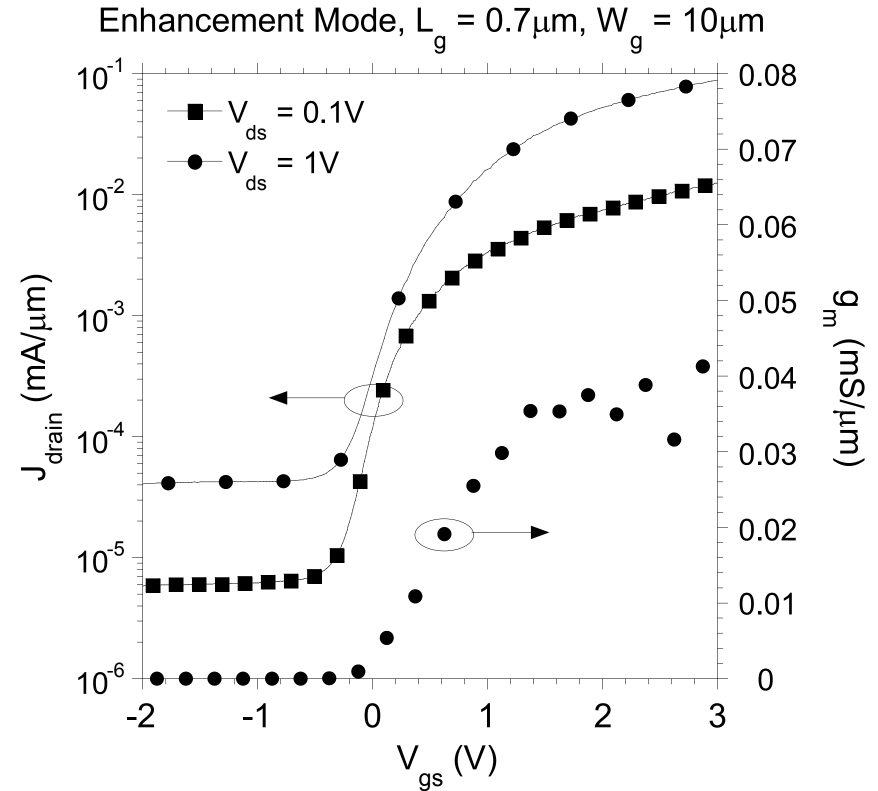


Poor on-state current density

→ Ungated/undoped access regions

Gate First E-Mode FET Results



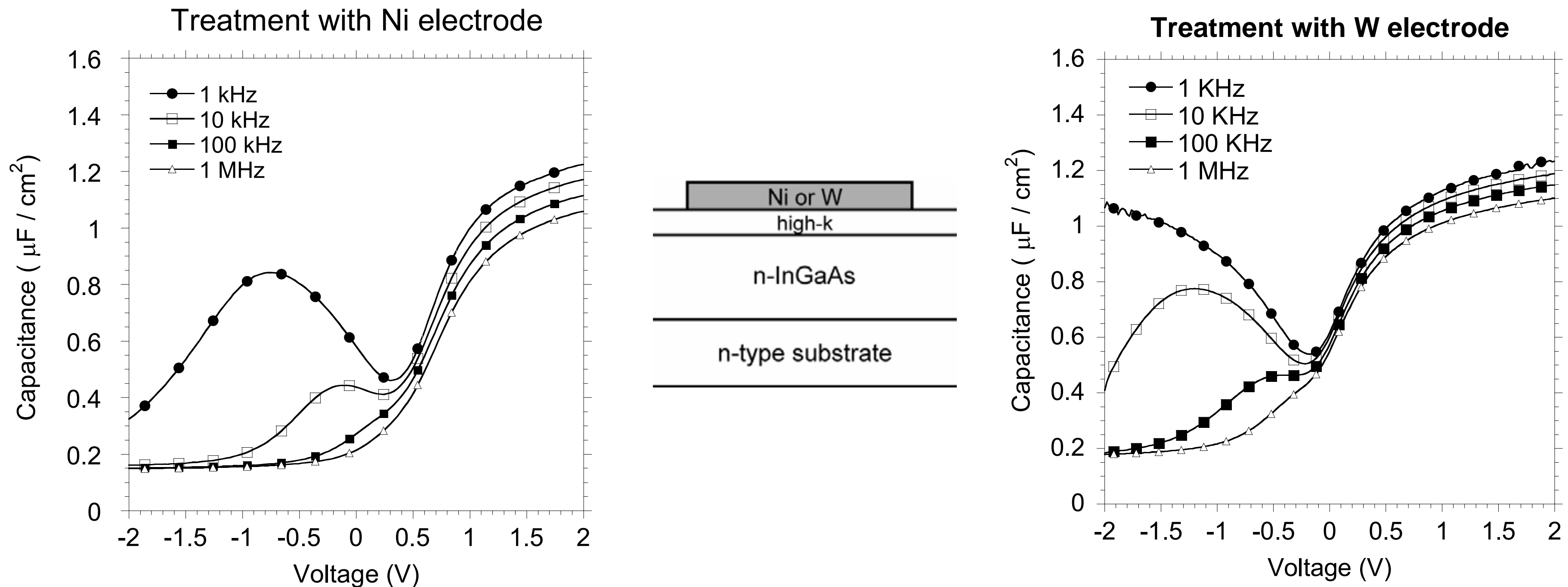


Less DIBL

→ Less delta doping

Gate First FET: Issues

Process-induced CV dispersion



Ni electrode: Thermally deposited, no overcoat, 400°C

W electrode: Sputter deposited, SiO_2 overcoat, 500°C anneal
→ mimics FET processing, regrowth thermal cycle

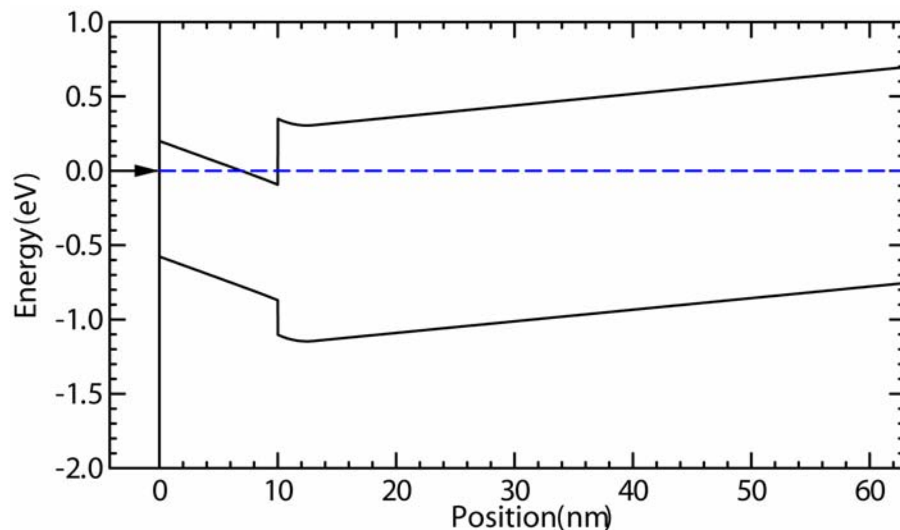
Increased D_{it} hinders device performance

Gate First FET: Issues

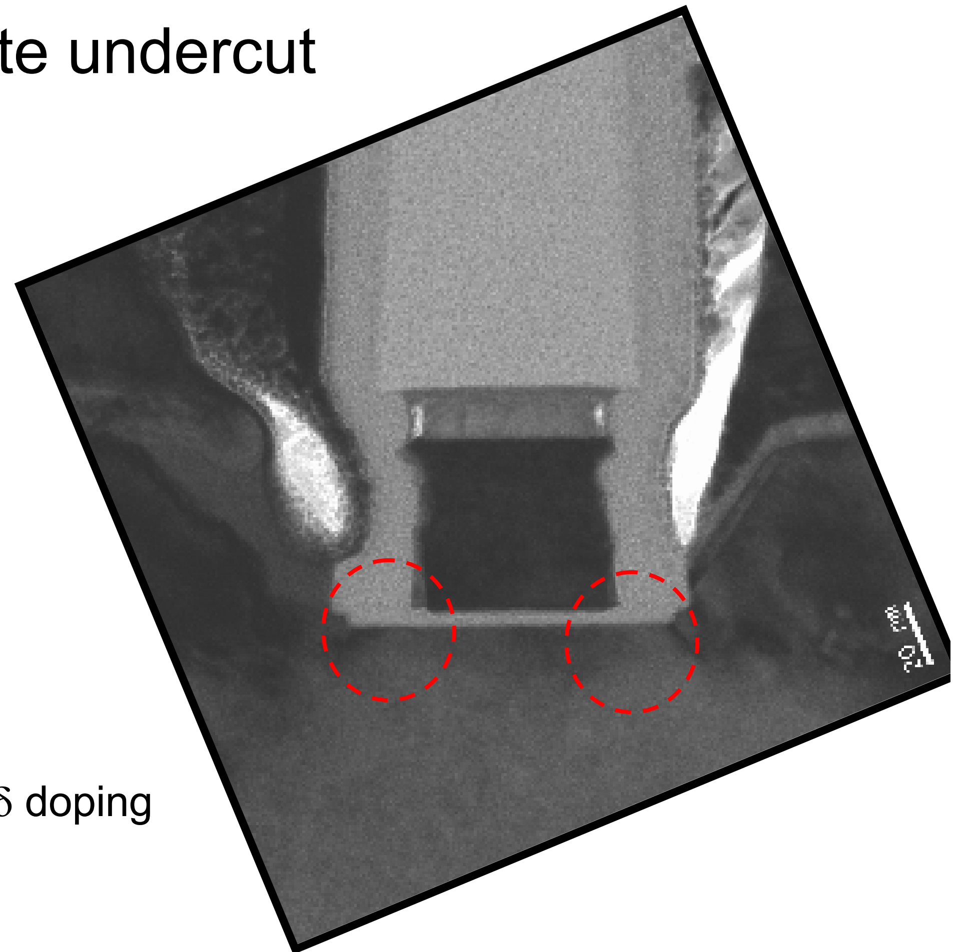
Ungated region → Current choke

Thinner sidewall can help…

… but hard to control with gate undercut



EBD of channel underneath sidewall, 3×10^{12} cm^{-2} δ doping



A.D. Carter DRC 2011.

Conclusions

- D_{it} passivation techniques for III-V MOS devices
- Process flow for gate first Al_2O_3/InGaAs MOSFETs
- Self-aligned process flow for scaled III-V VLSI
- Continued research areas
  - Minimizing ungated regions
  - Thinner dielectrics
  - D_{it} passivation techniques

Thanks for your time!
Questions?

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