60 nm gate length Al_2O_3 / $In_{0.53}Ga_{0.47}As$ gate-first MOSFETs using InAs raised source-drain regrowth

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Given adequately low source/drain (S/D) access resistivity and dielectric interface trap density ($R_{access} < 50$ Ω–μm,[1] and $D_{it} < 2\cdot10^{12}$ cm^{-2} eV^{-1},[2] respectively), InGaAs MOSFETs will provide greater on-state current than silicon MOSFETs at the same effective oxide thickness (EOT). The access resistance must be obtained in a self-aligned structure with a contacted gate pitch ~4 times the physical gate length (L_g), e.g. 116 nm at 32 nm L_g,[3] while control of short channel effects demands that the S/D region depth be only a fraction of gate length; low-resistance, ultra-shallow fully self-aligned III-V MOS processes must therefore be developed. Here we report a 60 nm L_g $In_{0.53}Ga_{0.47}As$ MOSFET fabricated in a gate-first process with self-aligned raised InAs S/D access regions formed by MBE regrowth. The devices have a peak drive current of 1.36 mA/μm at V_{ds} = 1.25 V and V_{gs} = 3 V and an R_{on} = 341 ohm-μm. To our knowledge this is the lowest R_{on} and smallest L_g reported to date for $In_{0.53}Ga_{0.47}As$ surface channel MOSFETs.[4]

The epitaxial layer structure, grown by molecular beam epitaxy (MBE), has a semi-insulating Fe doped InP substrate, 300 nm not intentionally doped (NID) $In_{0.52}Al_{0.48}As$, 3 nm $In_{0.52}Al_{0.48}As$ n-type Si-doped at $3\cdot10^{19}$ cm^{-3}, and 10nm NID $In_{0.53}Ga_{0.47}As$. Prior to atomic layer deposition (ALD) growth of the ~5 nm Al_2O_3 gate dielectric, the surface was treated by repeated hydrogen plasma / trimethylaluminum (TMA) cycles. A 60 nm sputtered W/15 nm electron beam evaporated Cr/400 nm PECVD SiO_2/15 nm electron beam evaporated Cr gate stack was blanket-deposited. Gate lengths between 60 nm to 1.3 μm were defined by patterning the upper Cr layer with a combination of electron beam and optical lithography. A high power inductively coupled (ICP) plasma SF_6/Ar etch defined vertical pillars in the SiO_2 layer. Cl_2/O_2 ICP etched the Cr, and a SF_6/Ar ICP etched the W gate. Etch undercuts in the W and Cr layers are less than 10 nm. 25nm SiN_x was deposited by PECVD and etched in a CF_4/O_2 ICP, defining gate sidewalls. After gate oxide removal in AZ400K, the semiconductor surface was oxidized by exposure to UV ozone and a subsequent removal of this oxide by a 10:1 DI H_2O:HCl etch prior to MBE loading. Regrowth of ~50 nm InAs n-type Si-doped at $\sim1\cdot10^{20}$ cm^{-3} ($\sim5\cdot10^{19}$ cm^{-3} active doping) was done as outlined in ref. [5]. 20 nm Ti / 60 nm Pd/120 nm Au was lifted off for source-drain metallization, and devices were isolated in a 1:1:25 H_3PO_4:H_2O_2:DI H_2O solution.

Devices were characterized using an Agilent 4155C semiconductor parameter analyzer. A 60 nm L_g / 9 μm W_g device has a peak drain current density of 1.36 mA/μm at V_{ds} = 1.25 V and V_{gs} = 3 V and an R_{on} = 341 ohm-μm. Extrapolated source and drain resistances R_S=R_D = 153 ohm-μm for these devices. Short channel effects and large delta doping underneath the channel prevent complete channel depletion. Heavy pulse doping ($\sim1\cdot10^{13}$ cm^{-2}) was used to overcome D_{it}-induced channel depletion underneath the ungated sidewall regions, which in turn increased device source to drain leakage. The ~60 nm L_g device has a DC transconductance g_m of 0.3 mS/μm at a V_{GS} = 0.7 V. Gate leakage current is < 20 nA/μm at all gate biases. The extracted R_S=(6.5 mS/μm)$^{-1}$ is too low to explain the measured g_m =0.3 mS/μm; suggesting that the transconductance is instead limited by the thick oxide and large D_{it}.. In conclusion, we have shown a 60 nm L_g Al_2O_3/InGaAs MOSFET with low R_{on} and low access resistance. Future work will include scaling the gate dielectric EOT, reducing process-damage-induced[6] D_{it} , and reduced width and increased carrier concentration in the sidewall regions surrounding the gate.

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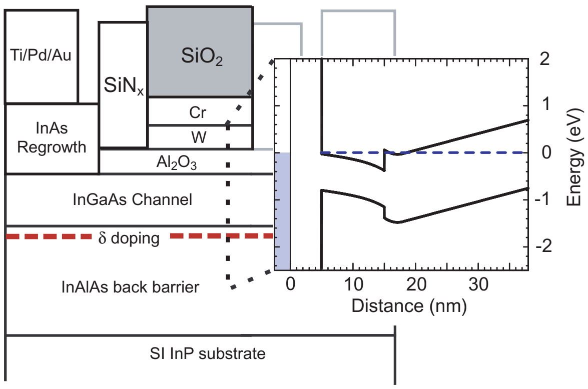

Figure 1: Schematic cross section of the gate first MOSFET. Inset: Energy band diagram across the gated channel region of the device.

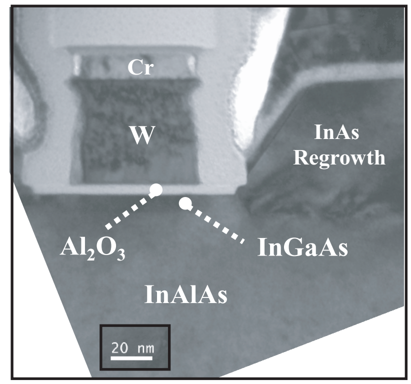

Figure 2: TEM cross section of a gate first MOSFET.

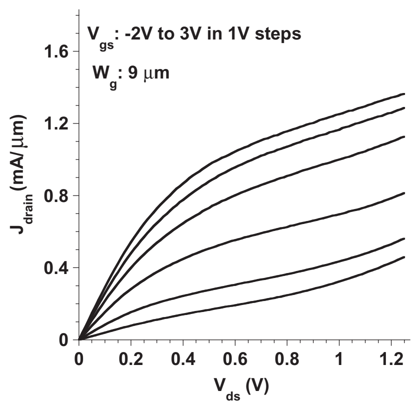

Figure 3: J_{drain} versus V_{ds} for 60 nm L_g depletion mode device.

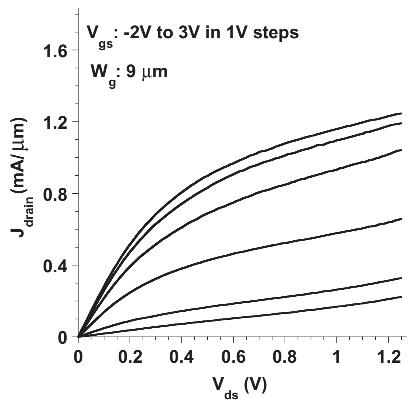

Figure 4: J_{drain} versus V_{ds} for 115 nm L_g depletion mode device.

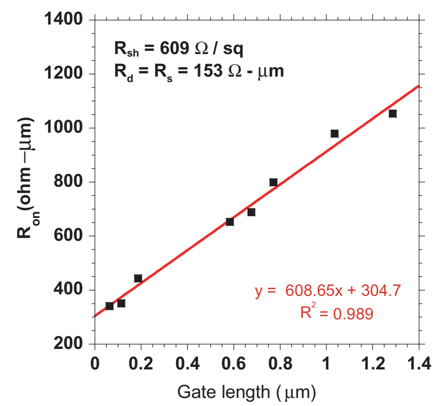

Figure 5: R_{on} as a function of gate length for 9 µm gate width devices, measured at V_{gs} = 3 V, V_{ds} = 0 to 0.1 V.

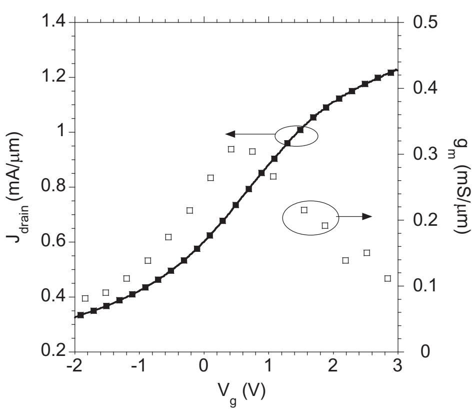

Figure 6: Measured J_{drain} versus V_{gs} (V_{ds} = 1 V) and DC transconductance for the 60 nm gate length device. Transconductance data is 5% weighting smoothed from raw data.

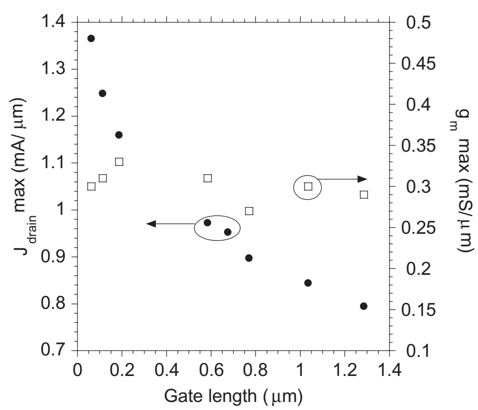

Figure 7: Maximum drain current density and DC transconductance versus gate length for 9µm gate width devices.

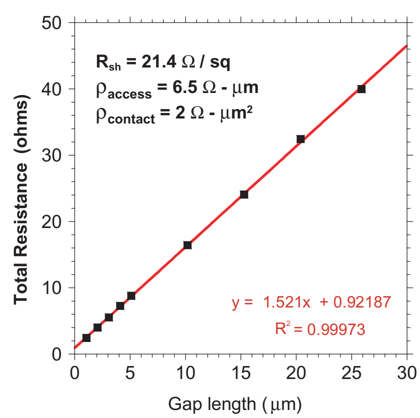

Figure 8: Transmission line measurement for 14 µm gap width of source-drain metalization and InAs regrowth.