



## 1.0-THz $f_{\max}$ InP DHBTs in a refractory emitter and self-aligned base process for reduced base access resistance

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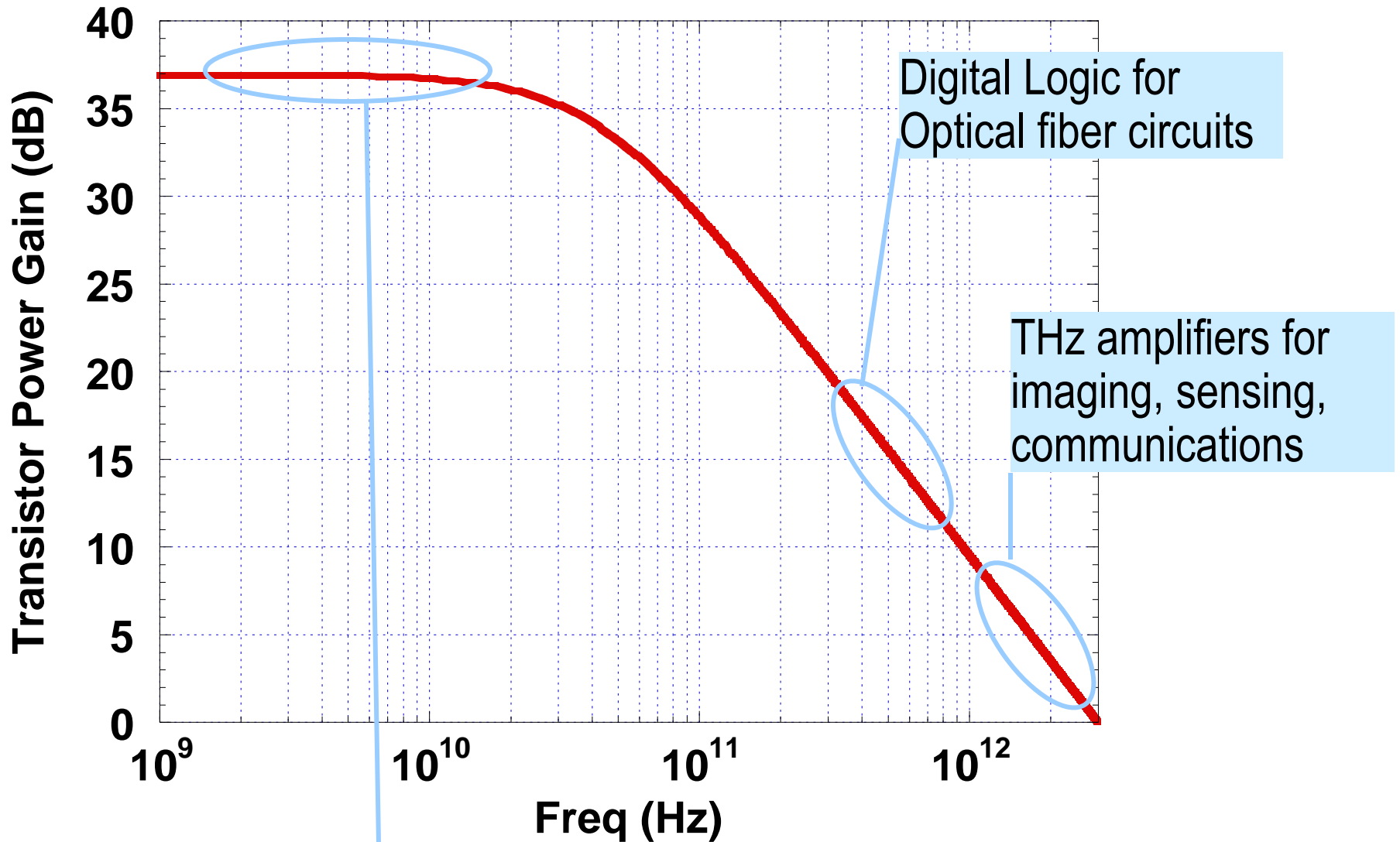
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# Outline

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- Need for high speed HBTs
- Fabrication
  - Challenges
  - Process Development
- DHBT
  - Epitaxial Design
  - Results
- Summary

# Why THz Transistors?



High gain at microwave frequencies → precision analog design, high resolution ADC & DAC, high performance receivers

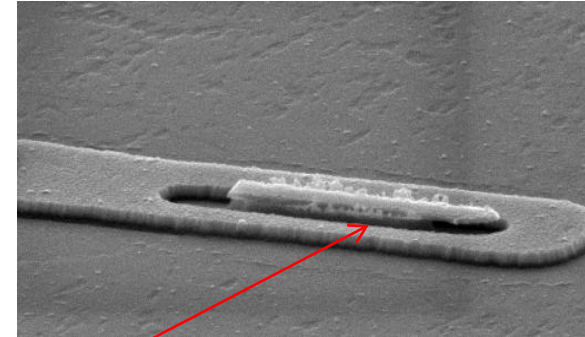
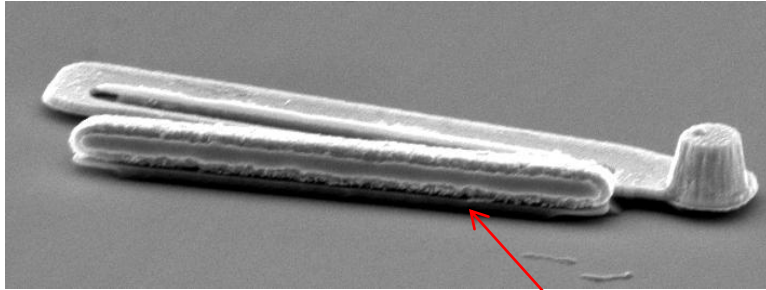
# HBT process requirements

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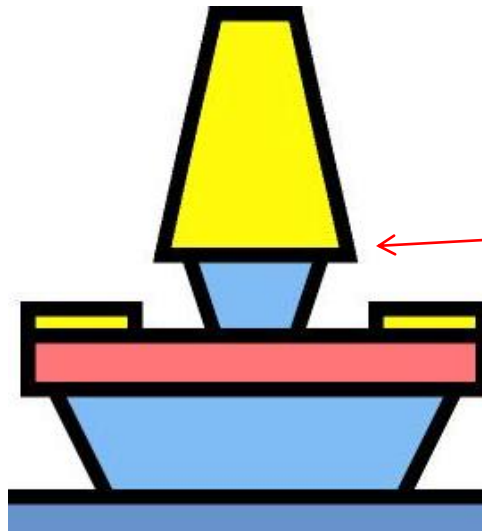
- **Refractory emitter contact and metal stack**
  - To sustain high current density operation
- **Low stress emitters**
  - For high yield
- **Low base access resistance**
  - For improved device  $f_{\max}$
- **Thin emitter semiconductor**
  - To enable a wet etched emitter process for reliability and scalability

# Fabrication Challenges – Stable refractory emitters

Emitter yield drops during base contact, subsequent lift-off steps



Fallen emitters



High stress in emitter metal stack

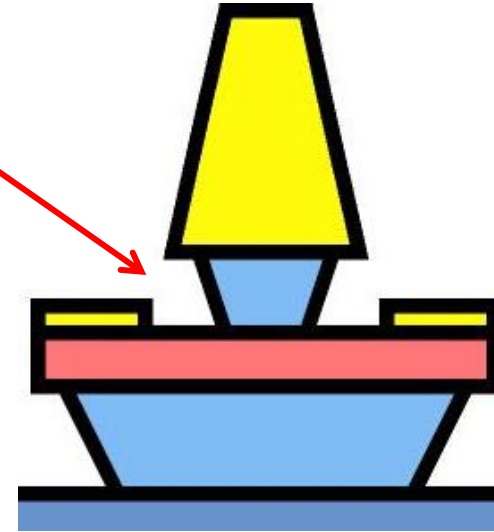
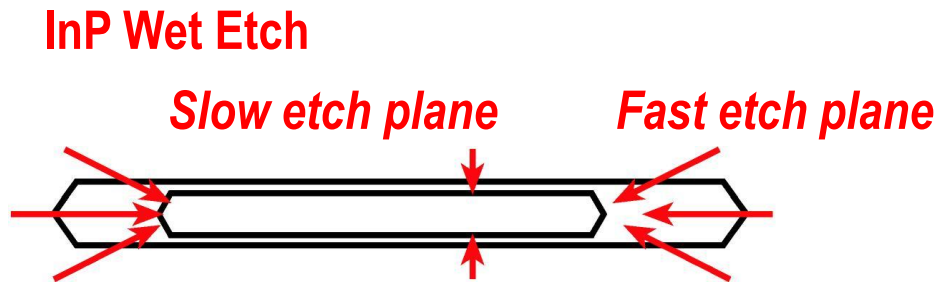
Poor metal adhesion to InGaAs

*Need for low stress, high yield emitters*

# Fabrication Challenges – Base-Emitter Short

Undercut in thick emitter semiconductor

Helps in Self Aligned Base Liftoff



For controlled semiconductor undercut

→ Thin semiconductor

To prevent base – emitter short

→ Vertical emitter profile and line of sight metal deposition

→ Shadowing effect due to high emitter aspect ratio

# Fabrication Challenges – Base Access Resistance

$$f_{\max} = \sqrt{\frac{f_{\tau}}{8\pi R_{bb} C_{cb}}}$$

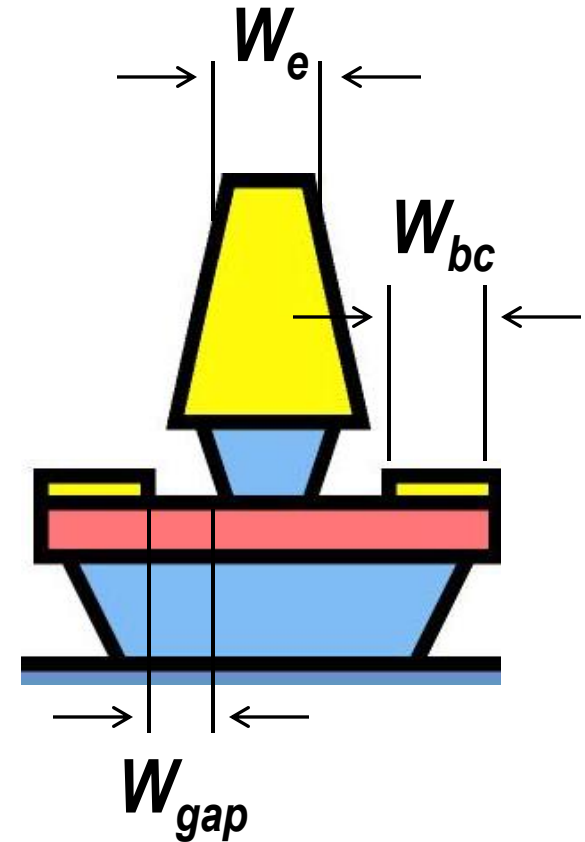
$$R_{bb} = \rho_{sh,e} \cdot \frac{W_e}{12L_e} + \rho_{sh,bc} \cdot \frac{W_{bc}}{6L_e} + \rho_{sh,gap} \cdot \frac{W_{gap}}{2L_e} + \frac{\rho_{contact}}{A_{contacts}}$$

$$\rho_{sh,gap} \gg \rho_{sh,e}, \rho_{sh,bc}$$

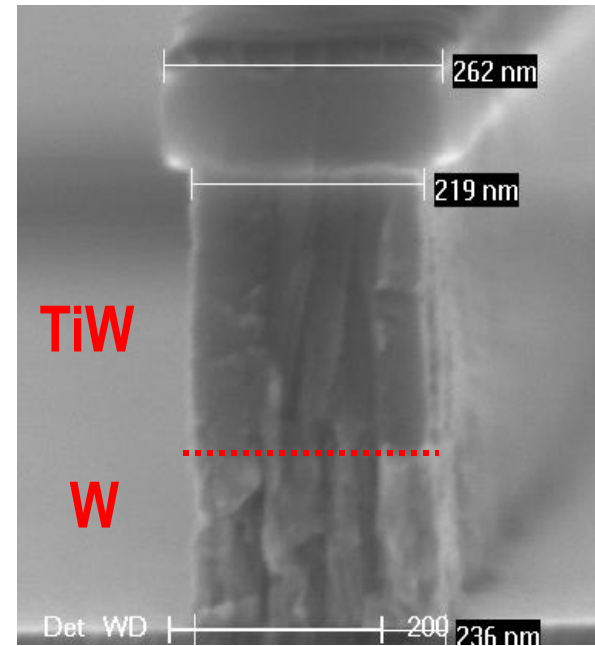
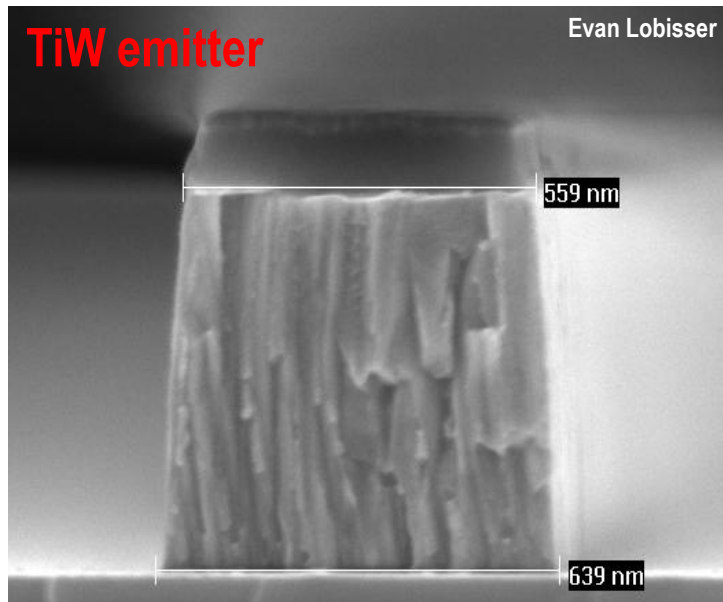
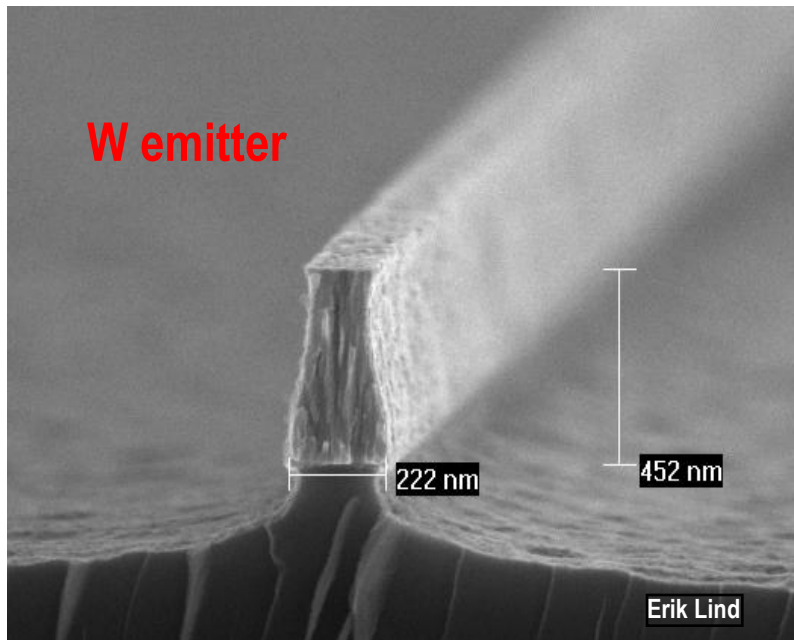
- Surface Depletion
- Process Damage

→ Need for very small  $W_{gap}$

- Small undercut in InP emitter
- Self-aligned base contact

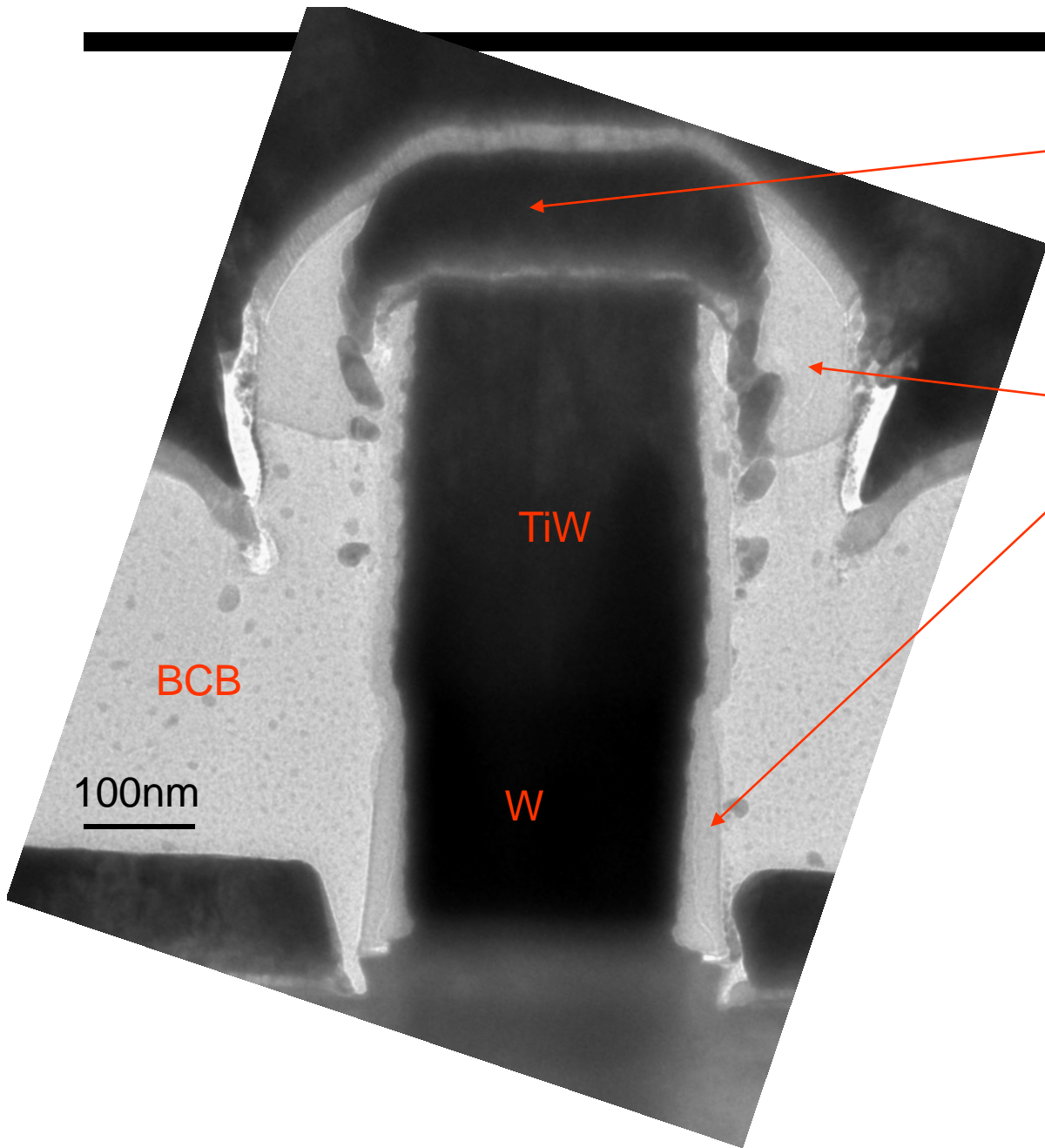


# Composite Emitter Metal Stack



- W/TiW metal stack
- Low stress
- Refractory metal emitters
- Vertical dry etch profile





Base  
Metal

SiN<sub>x</sub>

TiW

BCB

100nm

W

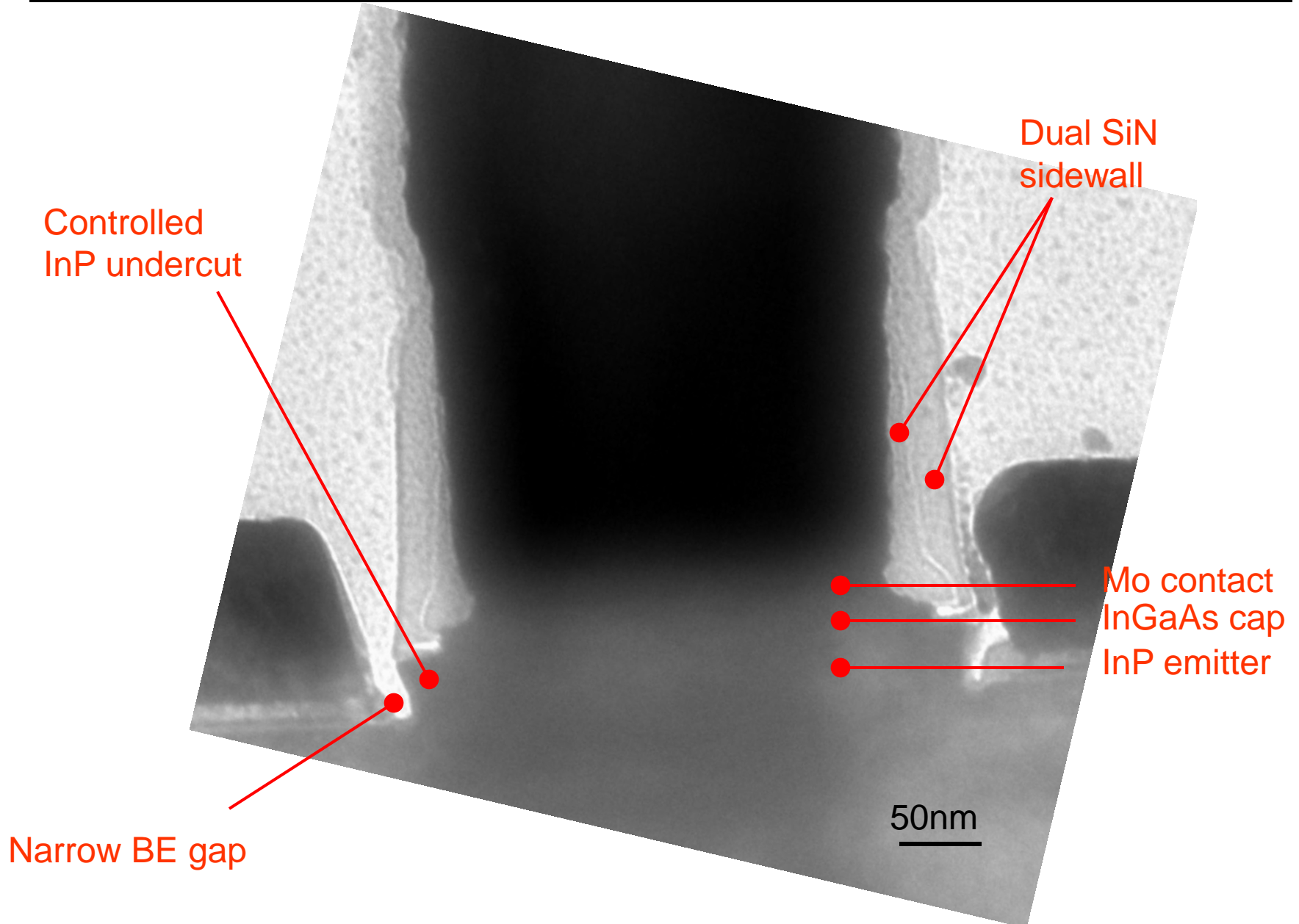
**Vertical etch profile**

**Low stress**

**High emitter yield**

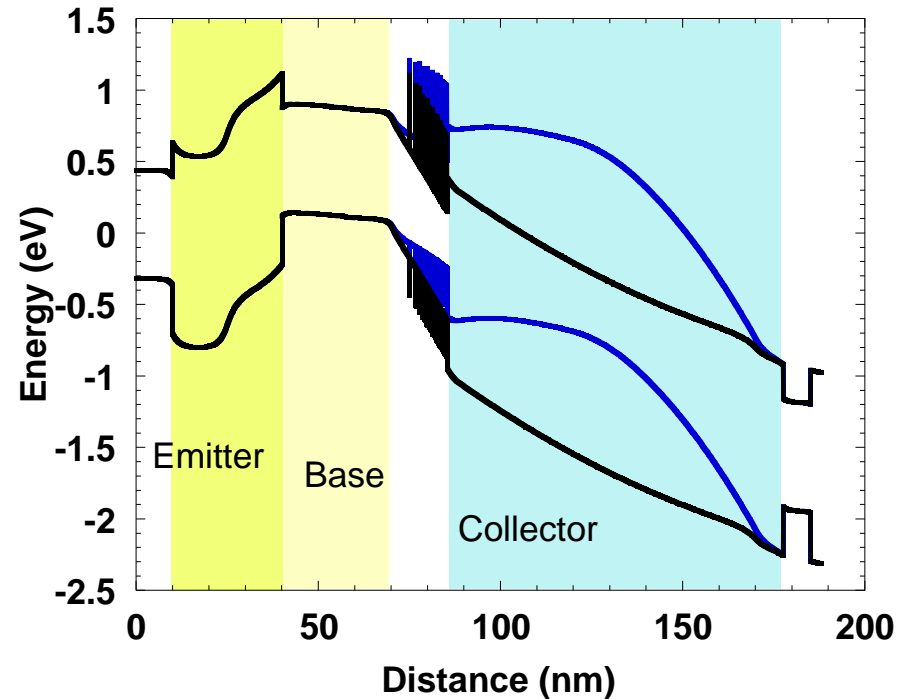
**Scalable emitter process**

# Narrow Emitter Undercut



# Epitaxial Design

T(nm)	Material	Doping (cm <sup>-3</sup> )	Description
10	In <sub>0.53</sub> Ga <sub>0.47</sub> As	8·10 <sup>19</sup> : Si	Emitter Cap
20	InP	5·10 <sup>19</sup> : Si	Emitter
15	InP	2·10 <sup>18</sup> : Si	Emitter
30	InGaAs	9-5·10 <sup>19</sup> : C	Base
13.5	In <sub>0.53</sub> Ga <sub>0.47</sub> As	5·10 <sup>16</sup> : Si	Setback
16.5	InGaAs / InAlAs	5·10 <sup>16</sup> : Si	B-C Grade
3	InP	3.6 ·10 <sup>18</sup> : Si	Pulse doping
67	InP	5·10 <sup>16</sup> : Si	Collector
7.5	InP	1·10 <sup>19</sup> : Si	Sub Collector
5	In <sub>0.53</sub> Ga <sub>0.47</sub> As	4·10 <sup>19</sup> : Si	Sub Collector
300	InP	2·10 <sup>19</sup> : Si	Sub Collector
Substrate	SI : InP		



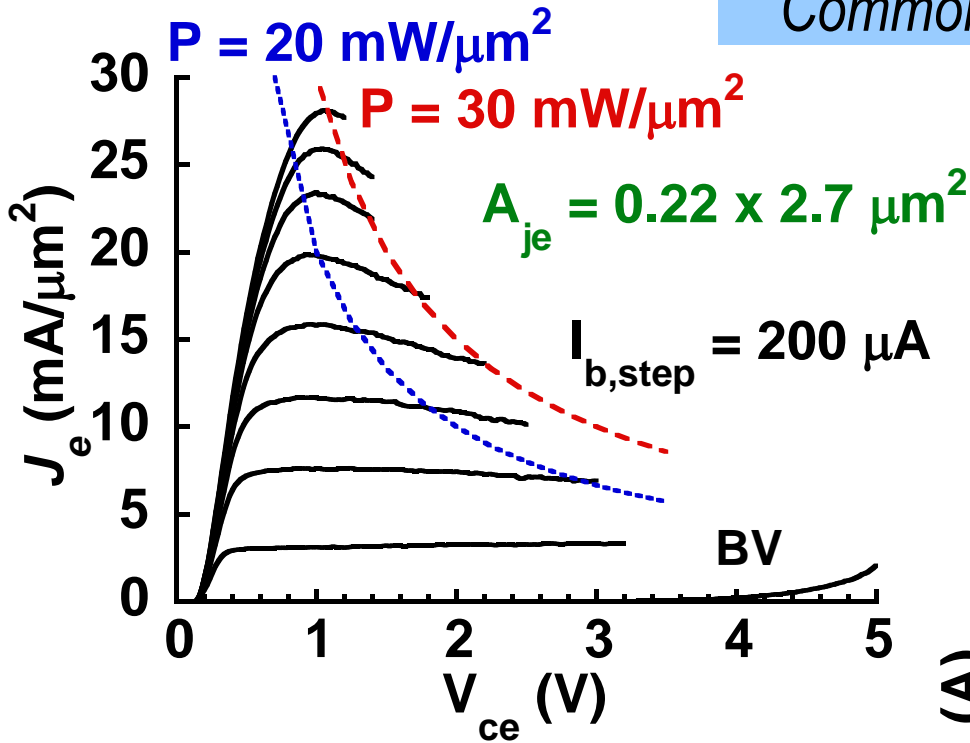
$$V_{be} = 1 \text{ V}, V_{cb} = 0.7 \text{ V}, J_e = 24 \text{ mA}/\mu\text{m}^2$$

Thin emitter semiconductor

→ Enables wet etching

# Results - DC Measurements

## Common emitter I-V



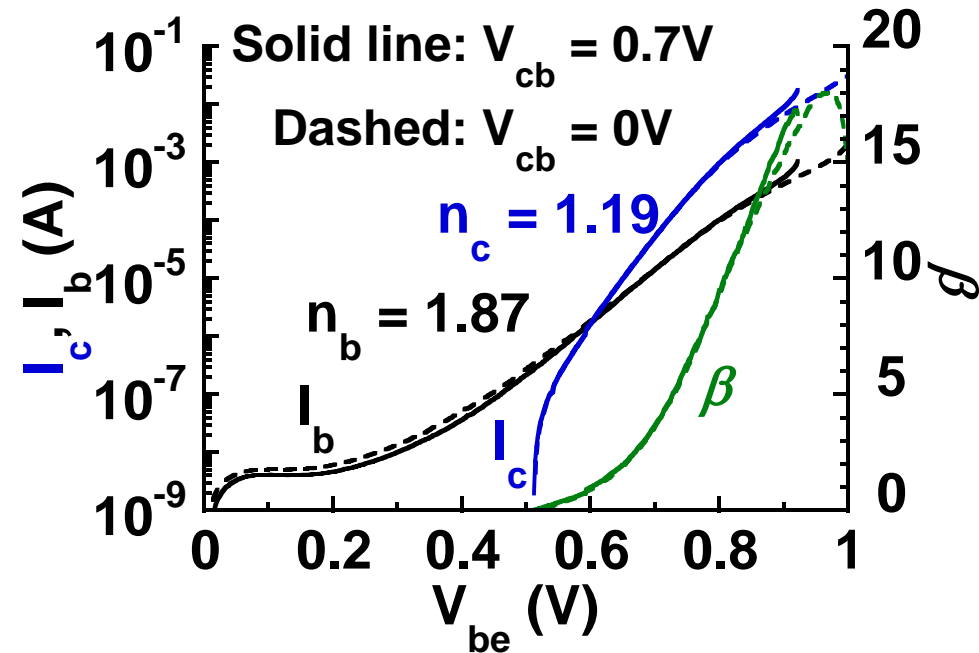
@Peak  $f_\tau, f_{max}$

$J_e = 20.4 \text{ mA}/\mu\text{m}^2$

$P = 33.5 \text{ mW}/\mu\text{m}^2$

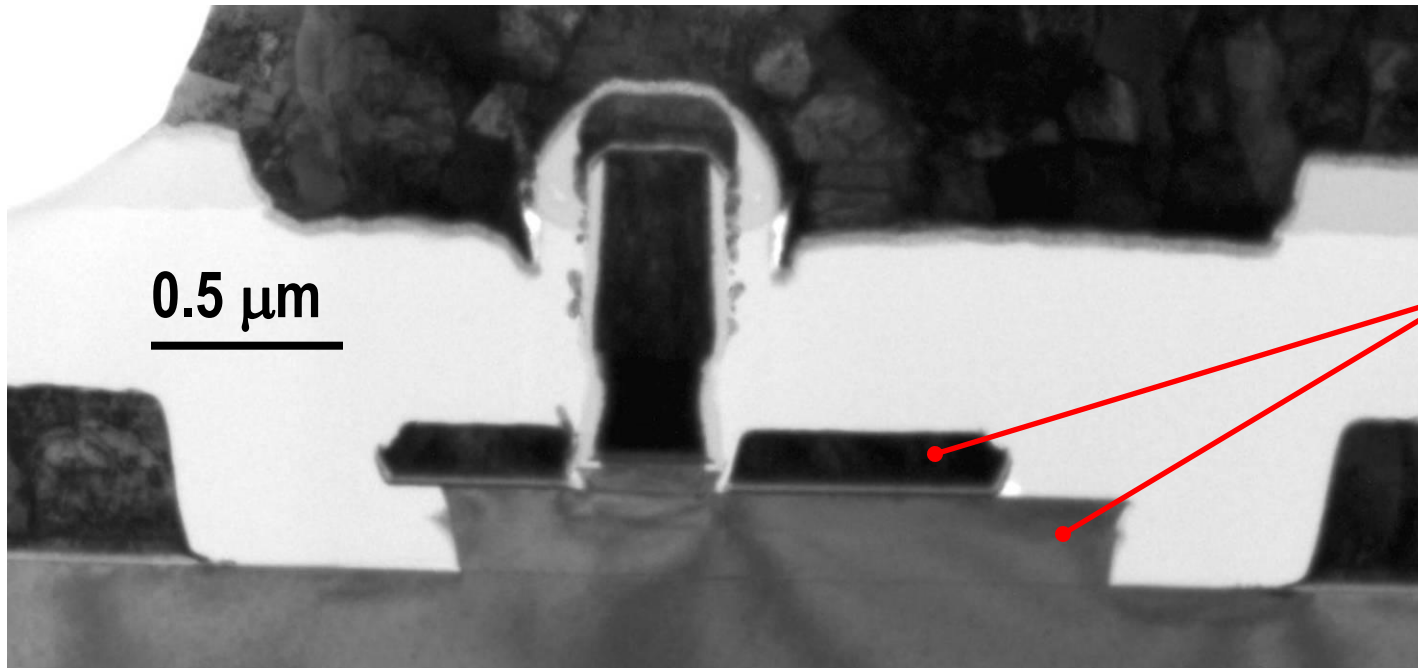
$BV_{ceo} = 3.7 \text{ V} @ J_e = 0.1 \text{ mA}/\text{cm}^2$

$\beta = 17$



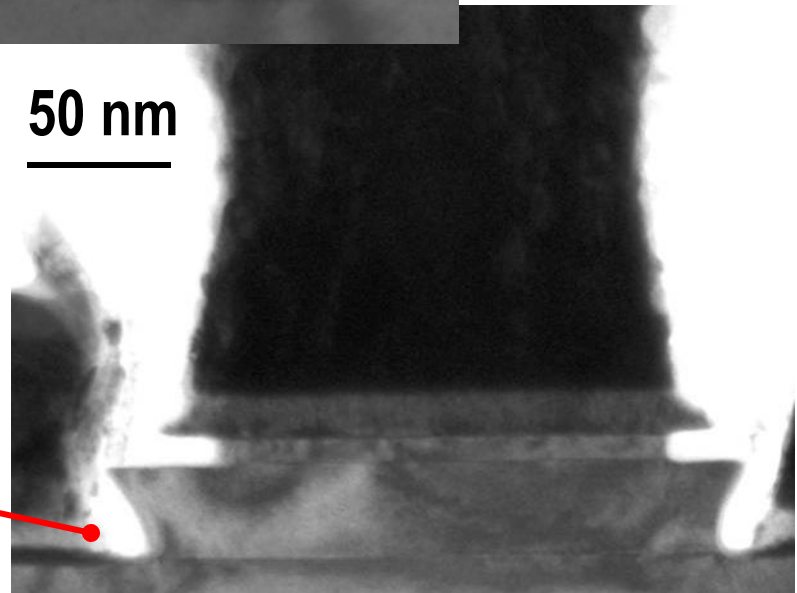
Gummel plot

# TEM – Wide, misaligned base mesa



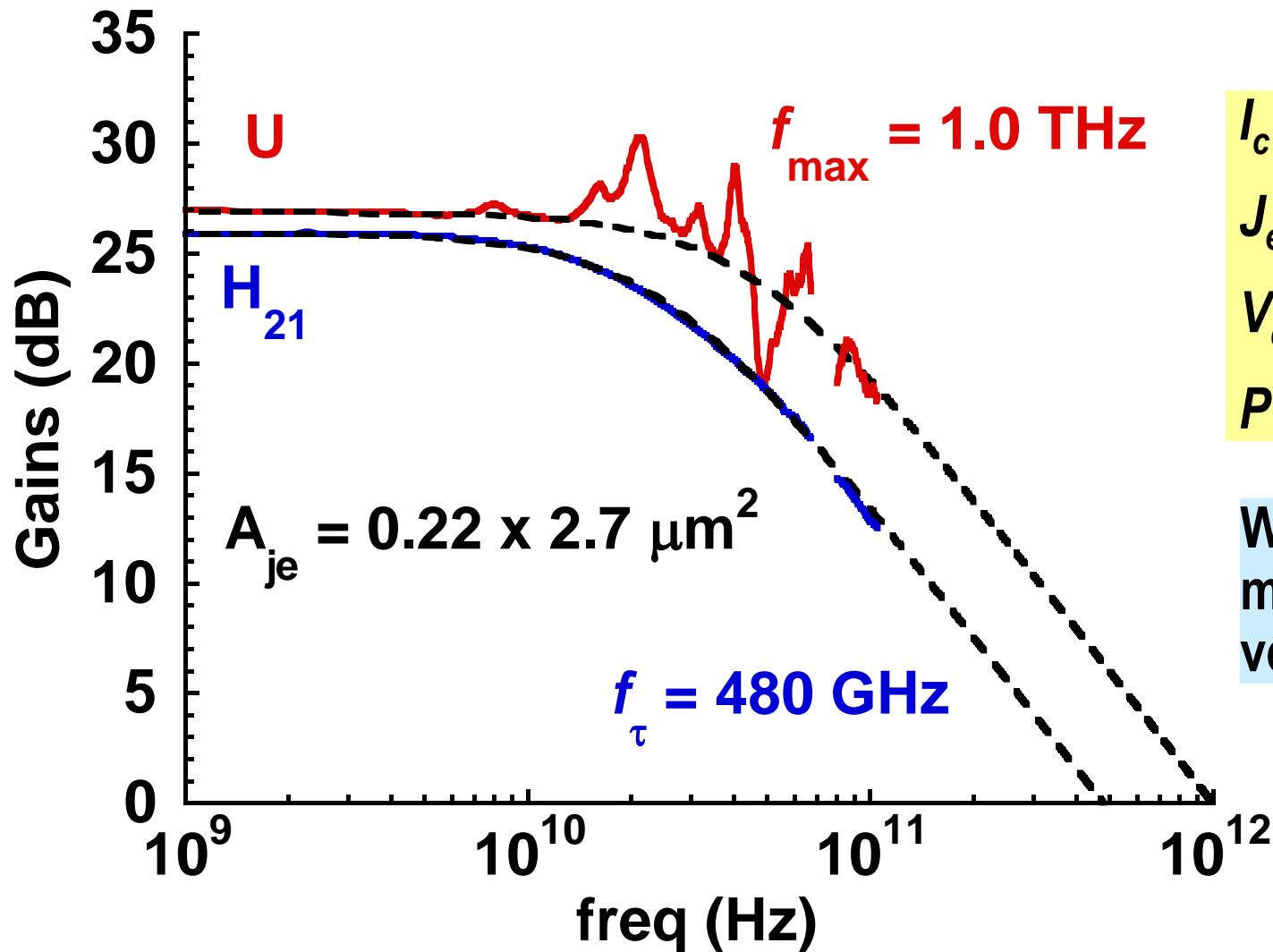
Misalignment

- 220 nm emitter-base junction
- 1.1  $\mu\text{m}$  wide base-collector mesa



Small EB gap

# RF Data



$I_c = 12.1 \text{ mA}$   
 $J_e = 20.4 \text{ mA}/\mu\text{m}^2$   
 $V_{cb} = 0.7 \text{ V}$   
 $P = 33.5 \text{ mW}/\mu\text{m}^2$

W-Band  
measurements to  
verify  $f_{\tau}/f_{\max}$

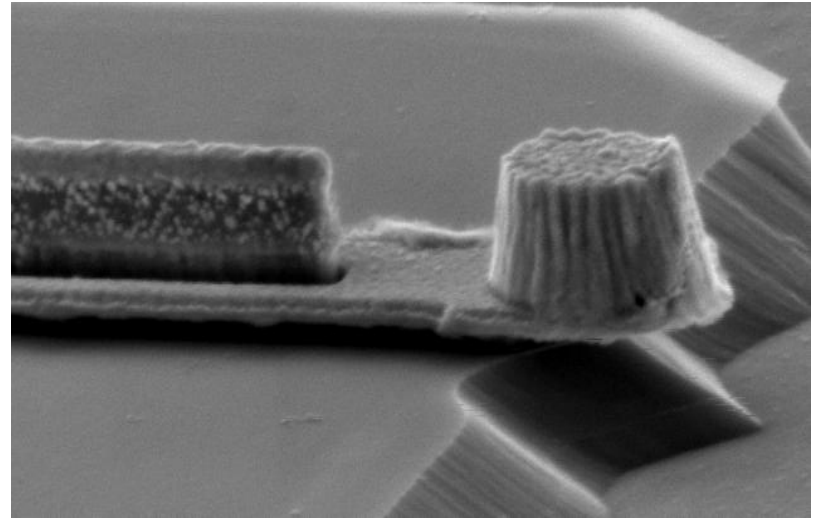
# Base Post Cap

$$C_{cb,post} = \frac{\epsilon_0 \epsilon_r \cdot A_{post}}{T_c}$$

$C_{cb,post}$  does not scale with  $L_e$

→ Adversely effects  $f_{max}$  as  $L_e \downarrow$

→ Need to minimize the  $C_{cb,post}$  value



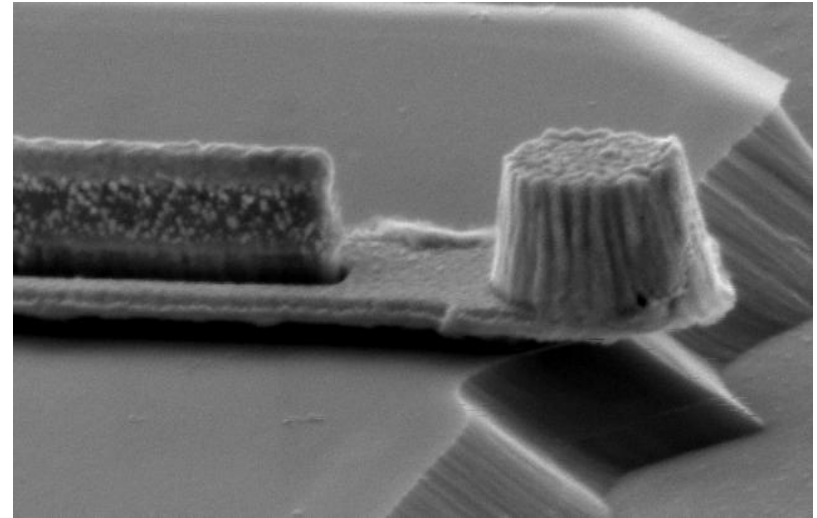
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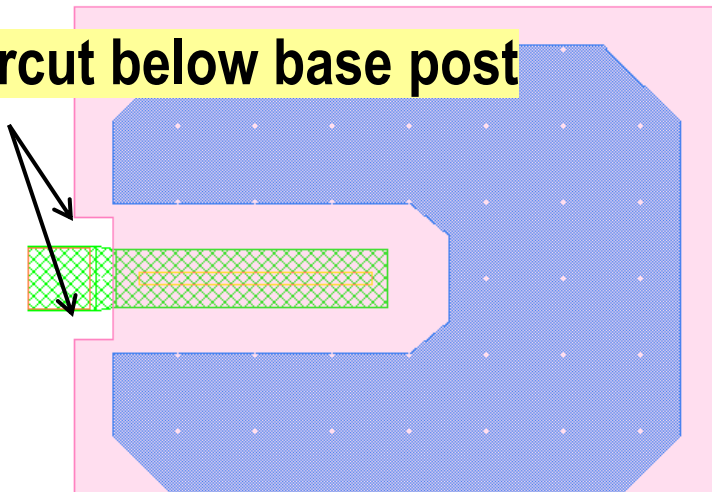
$C_{cb,post}$  does not scale with  $L_e$

→ Adversely effects  $f_{max}$  as  $L_e \downarrow$

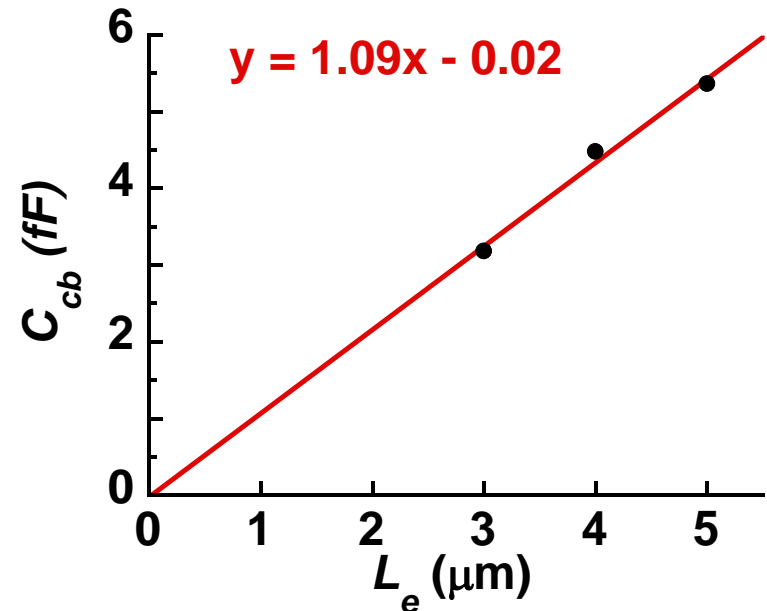
→ Need to minimize the  $C_{cb,post}$  value



Undercut below base post



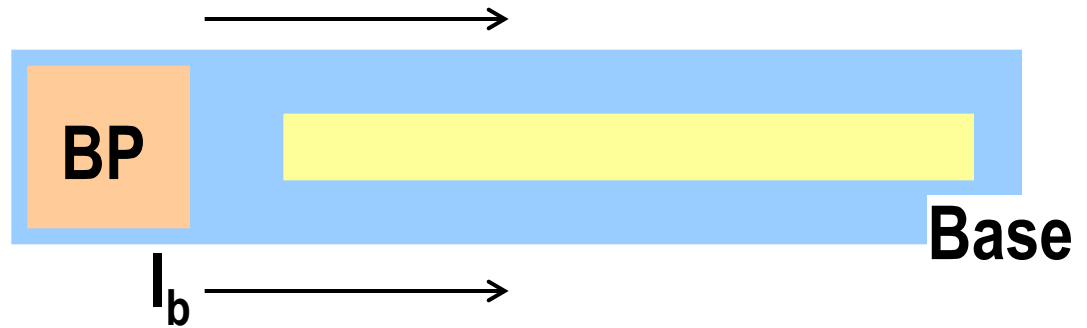
No contribution of Base post to  $C_{cb}$





# Base Metal Resistance

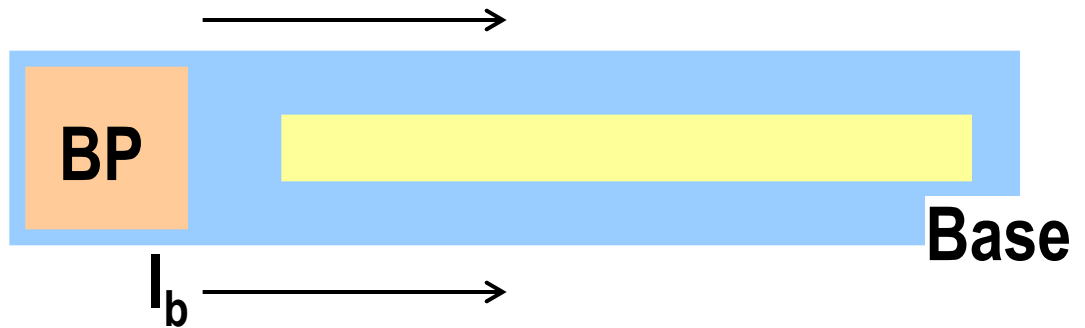
$$R_{bb,metal} = \rho_{sh,metal} \cdot \frac{L_e}{6W_{bc}}$$



- $R_{bb,metal}$  increases with emitter length
- $f_{max}$  decreases with increase in emitter length

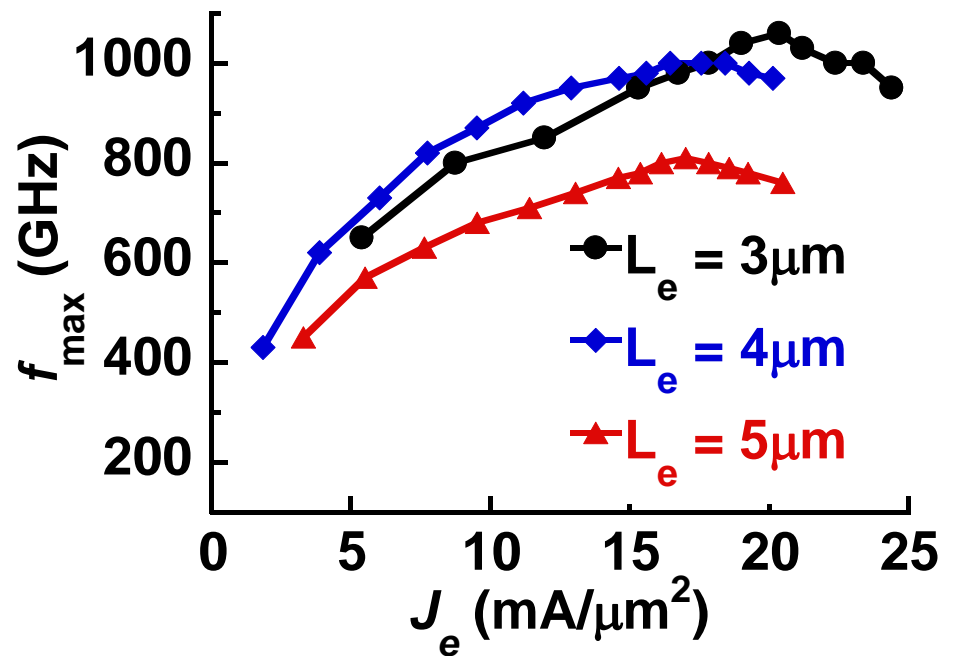
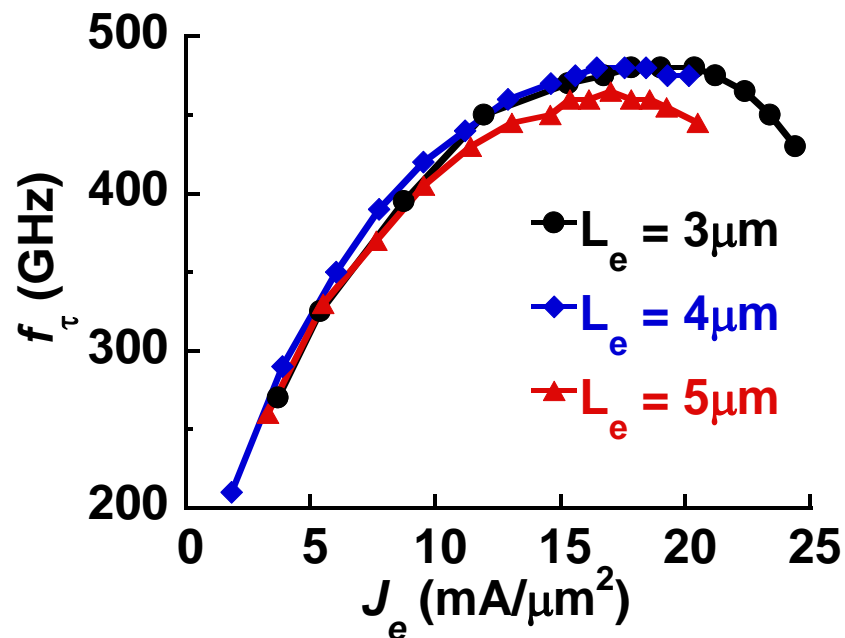
# Base Metal Resistance

$$R_{bb,metal} = \rho_{sh,metal} \cdot \frac{L_e}{6W_{bc}}$$

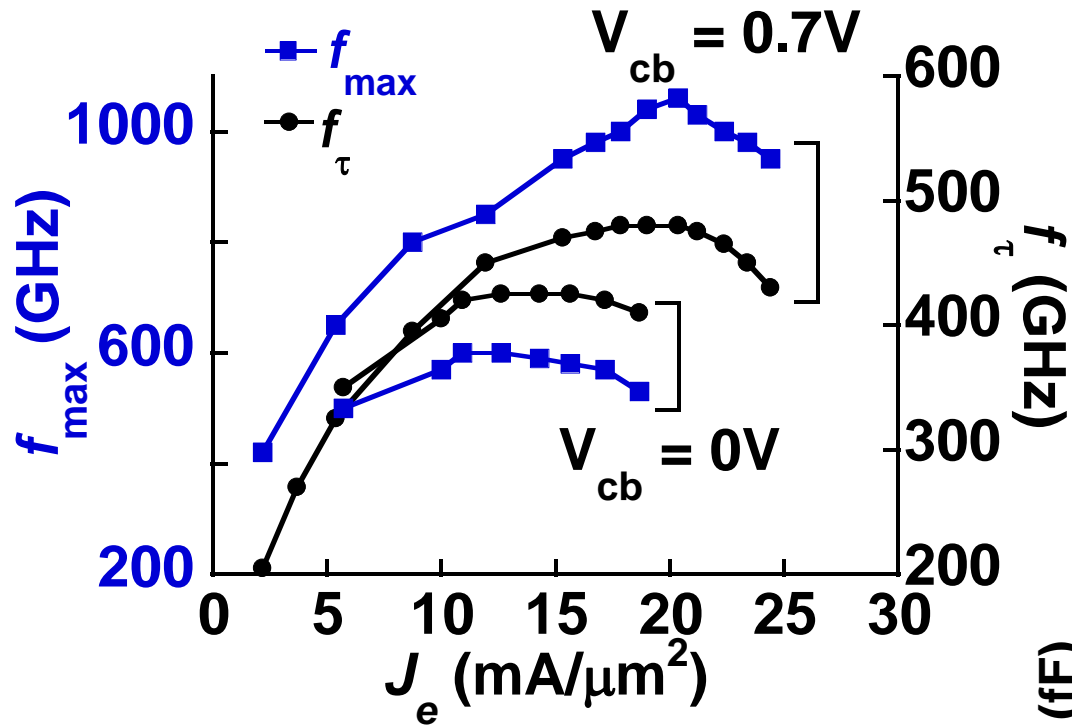


•  $R_{bb,metal}$  increases with emitter length

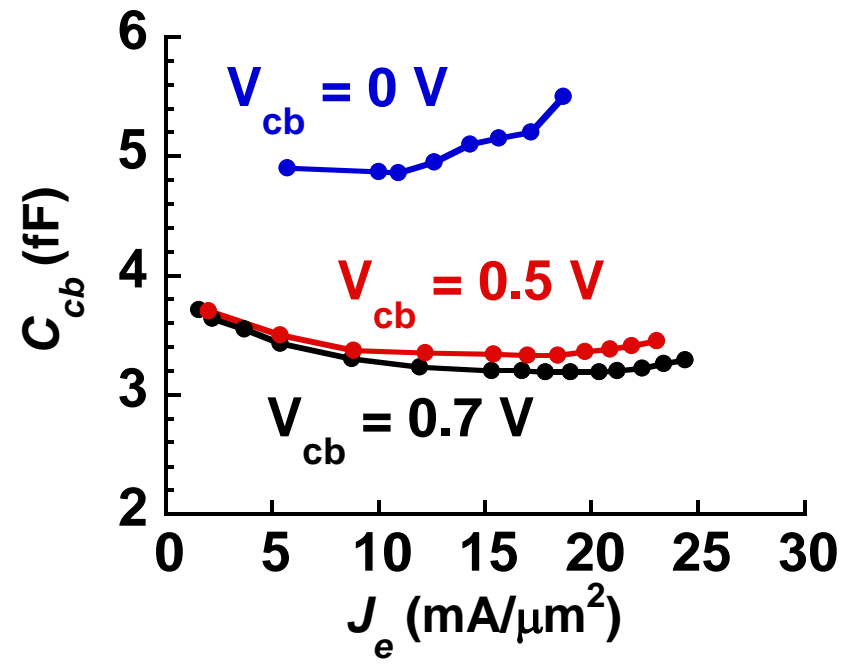
➔  $f_{max}$  decreases with increase in emitter length



# Parameter Extraction

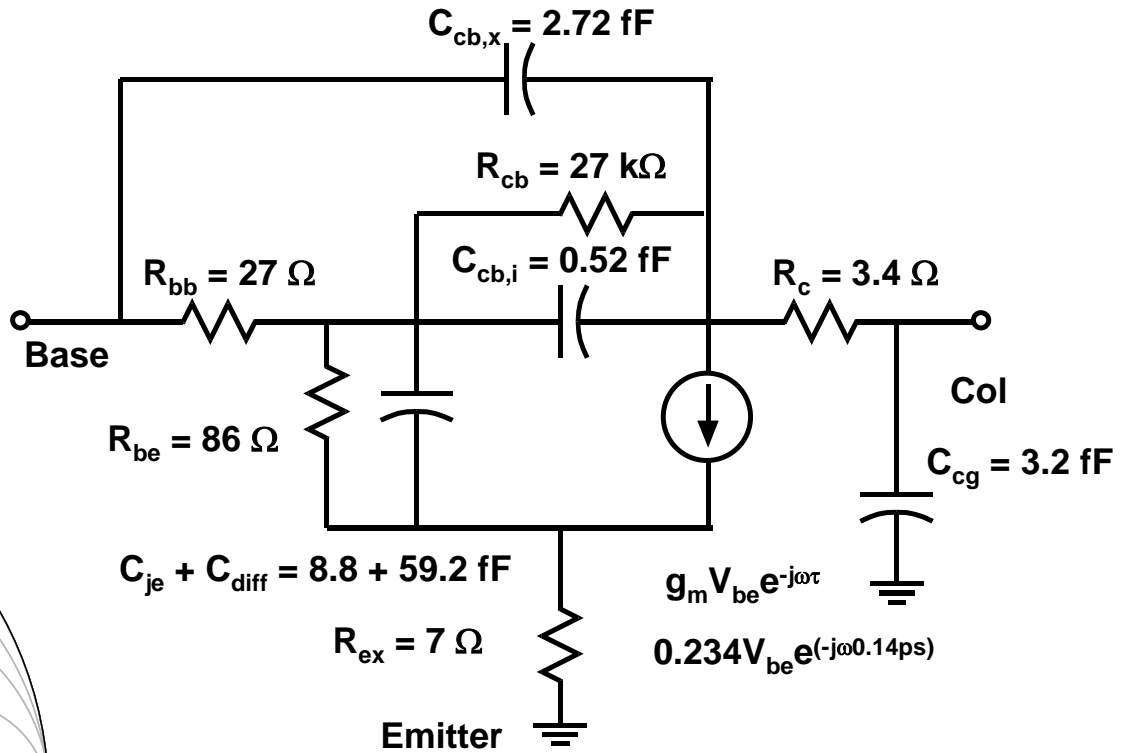
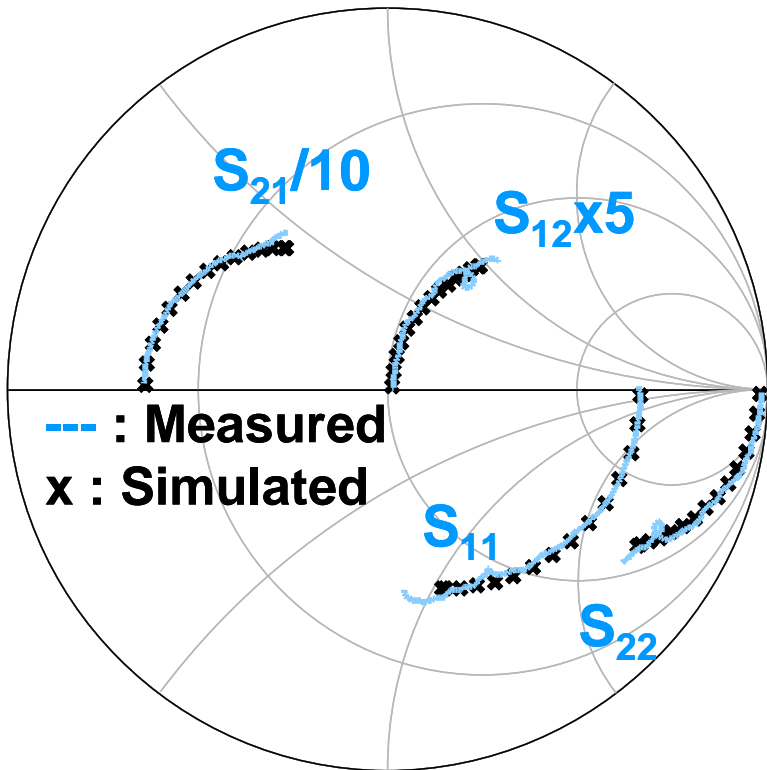


$J_{\text{kirk}} = 23\text{ mA}/\mu\text{m}^2$  (@  $V_{\text{cb}} = 0.7\text{V}$ )



# Equivalent Circuit

$R_{ex} \sim 4.2 \Omega \cdot \mu m^2$

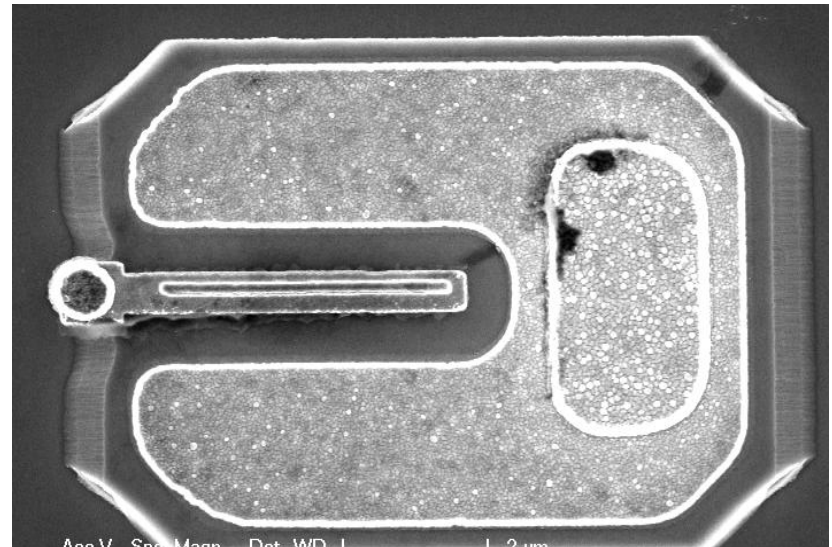
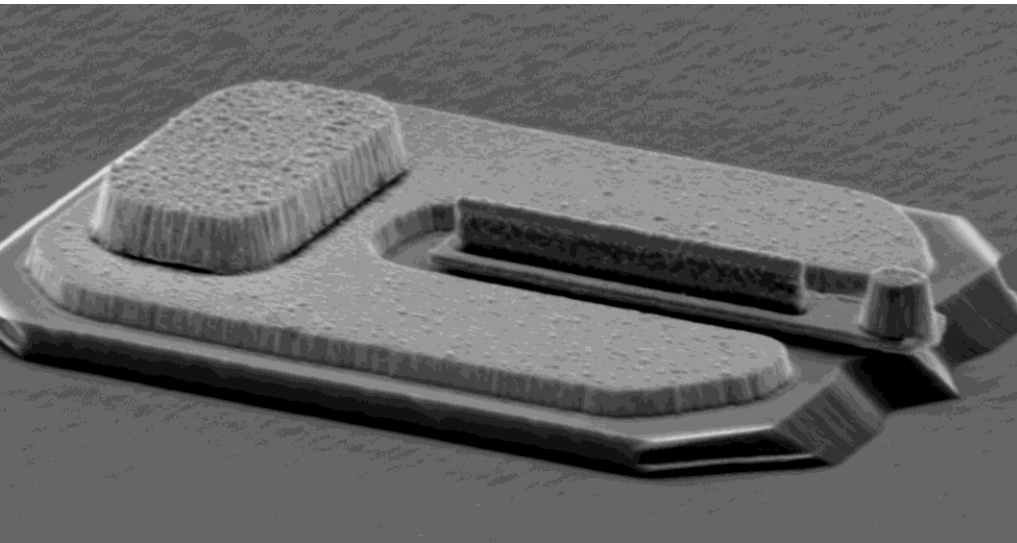


Hybrid- $\pi$  equivalent circuit from measured RF data

# Summary

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- Demonstrated DHBTs with peak  $f_{\tau} / f_{\max} = 480/1000$  GHz
- Small  $W_{\text{gap}}$  for reduced base access resistance  $\rightarrow$  High  $f_{\max}$
- Undercut below the base post to reduce  $C_{cb}$
- Narrow sidewalls, smaller base mesa and better base ohmics needed to enable higher bandwidth devices



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# Thank You

## Questions?

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