

## Al<sub>2</sub>O<sub>3</sub> Growth on (100) In<sub>0.53</sub>Ga<sub>0.47</sub>As Initiated by Cyclic Trimethylaluminum and Hydrogen Plasma Exposures

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The influence of hydrogen plasma treatment before atomic layer deposition of aluminum oxide on In<sub>0.53</sub>Ga<sub>0.47</sub>As is investigated. Experiments on untreated, trimethylaluminum-treated, hydrogen-plasma treated, and iterative hydrogen plasma/trimethylaluminum-treated samples are compared in the context of interface trap density,  $D_{it}$ . Through the conductance method, it was found that five cycles of two s, 20 mT, 100 W hydrogen plasma alternating with 40 ms of trimethylaluminum dose prior to dielectric growth resulted in a reduction of interface trap density (0.2 eV below the conduction band edge) from  $4.6 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$  for untreated samples to  $1.7 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$  for treated samples.

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**M**etal-oxide-semiconductor field-effect transistors (MOSFETs) with In<sub>x</sub>Ga<sub>1-x</sub>As channels are being investigated as an alternative to silicon FETs due to the potential for higher drive currents at the same equivalent oxide thickness.<sup>1-6</sup> High on-state currents and low-off state currents will, however, only be obtained given adequately low source/drain access resistances, and adequately low trap densities,  $D_{it}$ , at the dielectric/semiconductor interface.<sup>7</sup> Large trap densities both decrease the on-state drive current and degrade the subthreshold characteristics.

MOSFETs with III-V semiconductor channels were first reported in 1965;<sup>8</sup> subsequent efforts to develop low- $D_{it}$  dielectrics on GaAs include sulfur surface treatments,<sup>9</sup> GdGaO<sub>x</sub> dielectrics,<sup>10</sup> and *in situ* Al<sub>2</sub>O<sub>3</sub> growth.<sup>11</sup> MOS capacitors (MOSCAPs) on In<sub>0.53</sub>Ga<sub>0.47</sub>As using amorphous arsenic caps to reduce surface oxygen exposure show smaller capacitance-voltage (CV) frequency dispersion than control samples exposed to air between semiconductor growth and dielectric deposition; data analyses by the Terman and conductance methods indicate improved surface Fermi level movement.<sup>12,13</sup> Given such capping, no intermediate transistor fabrication process steps can be performed between channel semiconductor growth and gate dielectric deposition. This restricts the design of the transistor fabrication process flow. In particular, depositing the gate dielectric as one of the final transistor process steps reduces opportunities for inadvertent process damage to the gate dielectric. In this letter, we report measurements on In<sub>0.53</sub>Ga<sub>0.47</sub>As/Al<sub>2</sub>O<sub>3</sub> MOSCAPs for alternative dielectric growth initiation treatments. MOSCAPs that had Al<sub>2</sub>O<sub>3</sub> growth initiated by cyclic hydrogen plasma and trimethylaluminum (TMA) exposures show reduced  $D_{it}$  compared to samples that were not treated, as calculated by methods in ref. 14.

For MOSFET application in VLSI,  $D_{it}$  must be sufficiently small to not degrade the subthreshold swing (SS). In state-of-the-art silicon VLSI MOSFETs,<sup>15</sup> the SS does not exceed 100 mV/decade. The SS of a planar long channel inversion mode MOSFET is:

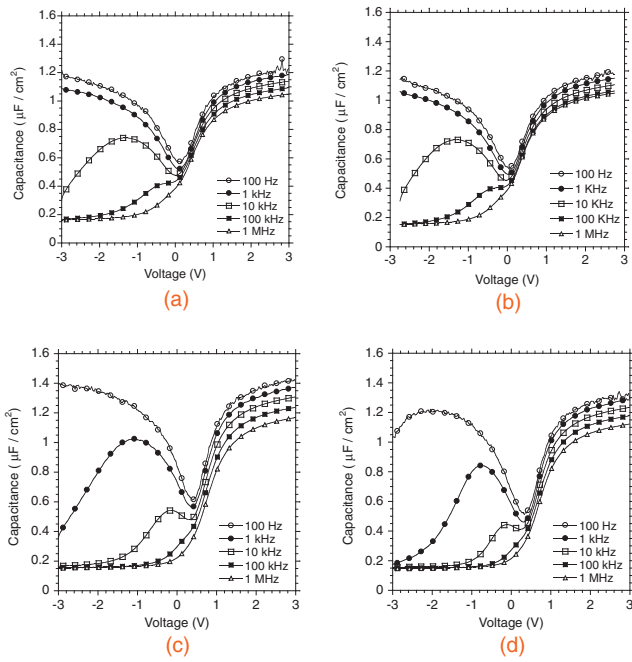
$$SS = \ln(10) \cdot \frac{k_B T}{q} \left( 1 + \frac{C_{dep} + C_{it}}{C_{ox}} \right), \quad (1)$$

where  $k_B$  is Boltzmann's constant,  $T$  is the temperature,  $C_{ox}$  is the effective oxide capacitance, taking into account the

gate dielectric capacitance and electron wave function depth,  $C_{dep}$  is the semiconductor depletion capacitance, and  $C_{it} = q^2 D_{it}$  is the interface state trap density capacitance.<sup>7</sup> For quantum well accumulation mode III-V MOSFETs,  $C_{dep} \ll C_{ox}$ . Therefore, to degrade the SS by less than 10%, the  $C_{it}$  must be less than 10% of the effective oxide capacitance. For 1 nm effective oxide thickness (EOT) MOSFETs,  $D_{it}$  throughout the semiconductor band gap cannot be greater than  $2.2 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ .

For the treatment experiments, samples with 300 nm  $1 \times 10^{17} \text{ cm}^{-3}$  Si-doped n-type In<sub>0.53</sub>Ga<sub>0.47</sub>As on  $\sim 3 \times 10^{18}$  sulfur-doped n-type InP were grown by molecular beam epitaxy (MBE). Before Al<sub>2</sub>O<sub>3</sub> deposition, samples were dipped for 10 s in 10 : 1 deionized H<sub>2</sub>O : HCl to remove surface oxides. Samples were then immediately loaded into a commercial atomic layer deposition (ALD) reactor (Oxford Instruments FlexAL ALD). The base pressure of the reactor was approximately  $10^{-6}$  Torr; the pressure was held at 0.2 Torr during the deposition. The substrate temperature was held constant at 300 °C. Prior to ALD Al<sub>2</sub>O<sub>3</sub> film growth, four different treatments involving remote inductively coupled plasmas (ICP) on the initial InGaAs surface were investigated. Treatment A was the reference point in which the surface was not treated in the chamber prior to ALD oxide growth. Treatment B exposed the surface to five cycles of trimethylaluminum (during each cycle: TMA pulse for 40 ms, 5 s Ar purge, and 10 s H<sub>2</sub> gas stabilization step) as a probe of TMA half cycle reactions on the surface prior to growth. Treatment C exposed the surface to five cycles of hydrogen plasma (during each cycle: 20 mTorr H<sub>2</sub> pressure at 100 W ICP power for 2 s, 5 s Ar purge, and 10 s H<sub>2</sub> stabilization step) as a probe of *in situ* surface oxide removal prior to growth. Treatment D subjected the surface to five cycles of hydrogen plasma and TMA exposure (during each cycle: 20 mTorr H<sub>2</sub> pressure at 100 W ICP power for 2 s, TMA pulse for 40 ms, 5 s Ar purge, and 10 s H<sub>2</sub> stabilization step) in order to determine the effects of active hydrogen not only on the surface oxide removal but also on the quality of the initial Al interface layer prior to bulk Al<sub>2</sub>O<sub>3</sub> growth. During each cycle of Al<sub>2</sub>O<sub>3</sub> film growth, TMA was pulsed for 20 ms followed by a 7 s Ar purge, deionized H<sub>2</sub>O was pulsed for 100 ms followed by a 7 s Ar purge, the reactor was pumped down for 7 s, and finally Ar was flowed at 0.2 Torr for 7 s. 50 such growth cycles were completed for all samples. *Ex situ* measurements using variable angle spectroscopic ellipsometry (J. A. Woollam M-2000DI) estimated

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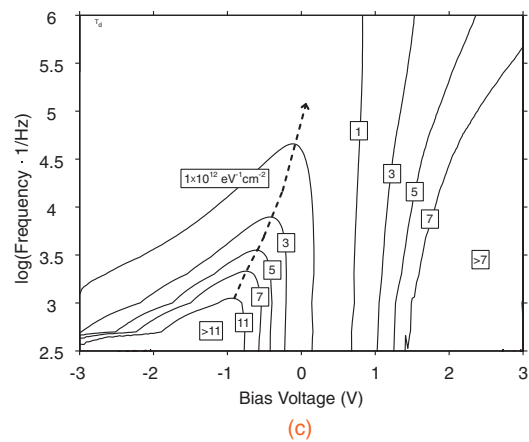
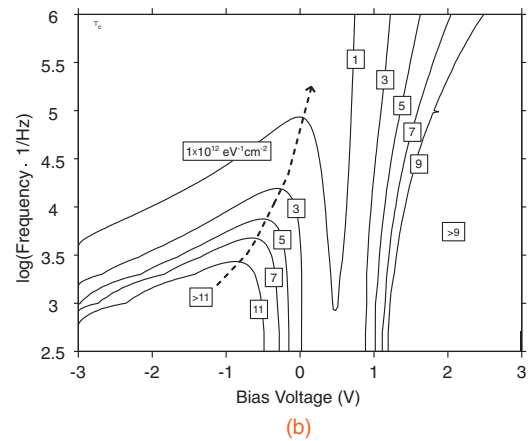
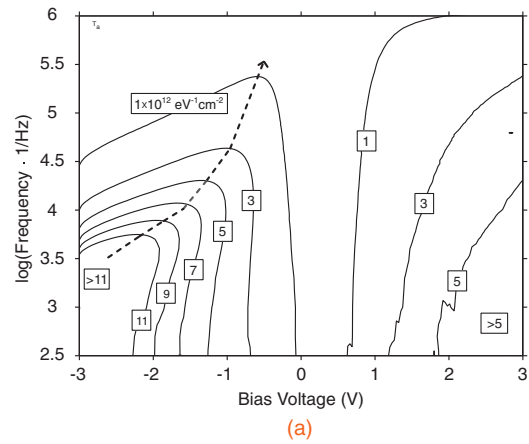
**Fig. 1.** Capacitance–voltage curves as a function of frequency for (a) the untreated sample, (b) the TMA-treated sample, (c) the hydrogen-plasma-treated sample, and (d) the hydrogen plasma and TMA-treated sample.

the nominal  $\text{Al}_2\text{O}_3$  growth rate at  $1.1 \text{ \AA}$  per cycle (5.5 nm total oxide thickness).

After oxide deposition, the samples were annealed at  $400^\circ\text{C}$  for 1 h in a rapid thermal annealer using 10 L/min forming gas flow at atmospheric pressure. In order to form MOSCAPs, 150- $\mu\text{m}$ -diameter, 100-nm-thick nickel gate electrodes were deposited by thermal evaporation on the  $\text{Al}_2\text{O}_3$  side of the sample through a shadow mask. Thermal evaporation was chosen to avoid sample damage by exposure to X-ray photons or high kinetic energy ions associated with electron beam evaporators and sputter deposition plasmas.<sup>16</sup> A back side ohmic contact was formed by blanket thermal evaporation of 10 nm Cr and 100 nm Au. Samples were then bonded to a gold-coated silicon carrier wafer with indium for subsequent measurements.

All electrical measurements used an Agilent 4294A impedance analyzer in a shielded dark box. The DC bias was swept from negative to positive voltages with a 50 mV RMS AC modulation signal. In order to accurately extract  $C_{\text{ox}}$ , MOSCAPs using Treatment D ( $\text{H}_2/\text{TMA}$  cycles) on a sample material with different  $\text{Al}_2\text{O}_3$  thicknesses were fabricated and measured at positive gate bias. From the variation of the measured capacitance with  $\text{Al}_2\text{O}_3$  thickness, a dielectric constant of  $8.7 \pm 0.2$  was determined.

Figures 1 and 2 show measurements of capacitance and conductance as a function of bias voltage and frequency. Samples having different surface preparations show clear differences in the capacitance dispersion in accumulation, in the false inversion capacitance peak,<sup>14</sup> in the rate of change of high-frequency capacitance with bias voltage, and in the conductance. Comparing accumulation capacitance at  $+2.75 \text{ V}$  bias, the ratio of low-frequency (100 Hz) to high-frequency (1 MHz) capacitance is 1.17 : 1 for the untreated sample (Treatment A), 1.12 : 1 for TMA-only treatment



**Fig. 2.** Contour plots of normalized conductance,  $G_p/(\omega A q)$ , as a function of frequency and bias voltage for (a) the untreated sample, (b) the hydrogen-plasma-treated sample, and (c) the hydrogen plasma and TMA-treated sample.

(Treatment B), 1.2 : 1 for  $\text{H}_2$ -only treatment (Treatment C), and 1.15 : 1 for  $\text{H}_2/\text{TMA}$  surface treatment (Treatment D). Yuan *et al.* attribute the dispersion in accumulation to border traps near the oxide/semiconductor interface.<sup>17</sup> Measurement of a peak in capacitance at biases below accumulation for n-type InGaAs samples is an indication of mid-gap  $D_{\text{it}}$ , not semiconductor surface inversion.<sup>14</sup> This false inversion capacitance peak is strongest in the untreated and TMA-only treated samples [Treatments A and B, Figs. 1(a) and 1(b)], moderate with  $\text{H}_2$ -only treatment [Treatment C, Fig. 1(c)], and smallest for  $\text{H}_2/\text{TMA}$  surface treatment [Treatment D,

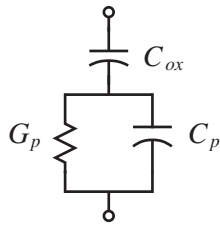


Fig. 3. Circuit model for the parallel conductance extraction.

Fig. 1(d)]. Another comparative measure of  $D_{it}$  is the rate of change of high-frequency capacitance with bias voltage called “stretch out”.<sup>18)</sup> For the untreated and TMA-only treated samples (Treatments A and B),  $dC/dV = 0.62 \mu\text{F cm}^{-2} \text{V}^{-1}$ , while for both the  $\text{H}_2$  and  $\text{H}_2/\text{TMA}$  samples (Treatments C and D),  $dC/dV \cong 0.9 \mu\text{F cm}^{-2} \text{V}^{-1}$ . For all four samples, there is no inversion response at negative bias. Furthermore, all samples fail to reach the minimum depletion capacitance ( $\sim 0.15 \mu\text{F/cm}^2$  measured versus  $0.11 \mu\text{F/cm}^2$  calculated via a Schrödinger–Poisson solver)<sup>19)</sup> expected for this epitaxial design at strong negative biases.

Engel-Herbert *et al.* have demonstrated quantitative measurement of  $D_{it}$  from measurement of the variation of conductance with bias voltage and frequency;<sup>14)</sup> Fig. 2 shows the normalized conductance–voltage maps for treatments A, C, and D. The parallel conductance  $G_p$  is derived from the circuit model of Fig. 3 and is expressed as

$$G_p = \frac{\omega^2 C_{ox}^2 G_{\text{measure}}}{G_{\text{measure}}^2 + \omega^2 (C_{ox} - C_{\text{measure}})^2}, \quad (2)$$

where  $\omega$  is the applied angular frequency, and  $C_{\text{measure}}$  and  $G_{\text{measure}}$  are the measured capacitance and conductance, respectively. Assuming Shockley-Read-Hall statistics for the traps, one can estimate the trap energy level below the conduction band edge from the applied measurement frequency:

$$\Delta E = \frac{k_B T}{q} \cdot \ln \left( \frac{\sigma v_{\text{thermal}} D_{\text{DOS}}}{\omega} \right), \quad (3)$$

where  $\sigma$  is the capture cross section,  $v_{\text{thermal}}$  is the semiconductor electron thermal velocity, and  $D_{\text{DOS}}$  is the three-dimensional effective conduction band density of states. The methods of Engel-Herbert *et al.* are used to determine  $D_{it}$  as a function of  $\Delta E$  below the  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  conduction band, and are described in detail in refs. 14 and 20.

Figure 4 shows  $D_{it}$  as a function of  $\Delta E$  below the  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  conduction band. For  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ , we assume  $\sigma = 1 \times 10^{-16} \text{ cm}^{-2}$ ,  $v_{\text{thermal}} = 5.6 \times 10^7 \text{ cm s}^{-1}$ , and  $D_{\text{DOS}} = 2.2 \times 10^{17} \text{ cm}^{-3}$ .<sup>14)</sup>  $D_{it}$  extracted by this method is highest for the untreated and TMA-only treated samples (Treatments A and B), both having  $4.6 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$  at 0.2 eV below  $E_c$ .  $D_{it}$  is moderate at  $2.5 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$  with  $\text{H}_2$ -only treatment (Treatment C), and smallest at  $1.7 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$  for  $\text{H}_2/\text{TMA}$  surface treatment (Treatment D). Figure 4 does not include measurements where  $C_{it} > C_{ox}$  since the conductance method is known to be inaccurate for this condition.<sup>14)</sup> The conductance map trend is clear in indicating the efficacy of the hydrogen plasma treatments to the  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{Al}_2\text{O}_3$  interface. It has been shown in the

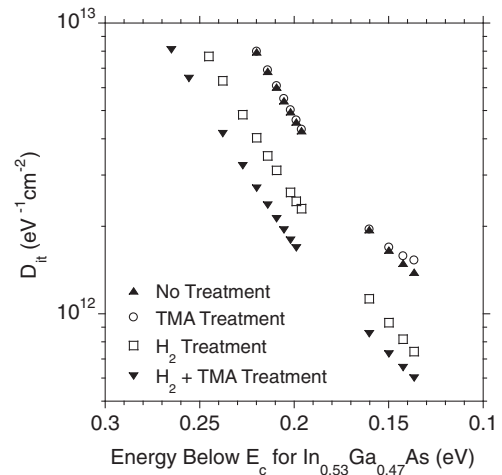


Fig. 4.  $D_{it}$  as a function of energy level below the (100)  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  conduction band edge for all three treatments.

literature that forming gas (5%  $\text{H}_2/95\% \text{N}_2$ ) annealing of Pt/high-k/ $\text{InGaAs}$  MOSCAPs improves the CV frequency dispersion and subsequently lowers the  $D_{it}$  extracted by the conductance method.<sup>14)</sup> Preliminary data on  $\text{H}_2/\text{TMA}$ -treated samples using the forming gas annealing shows similar trends and will be the subject of a subsequent publication.

In conclusion, we have shown that it is possible to reduce  $D_{it}$  using iterative exposures of hydrogen plasma and TMA before  $\text{Al}_2\text{O}_3$  growth on air-exposed  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  MOSCAP structures. This treatment will provide flexibility as to when gate dielectric deposition occurs during the MOSFET process flow. Further work is needed to understand the precise passivation mechanism to further reduce the  $D_{it}$  to acceptable levels throughout the band gap.

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