Workshop: Sub-millimeter-wave Monolithic Integrated Circuits. European Microwave Week. Amsterdam, Oct. 28, 2012

THz HBTs & sub-mm-wave ICs

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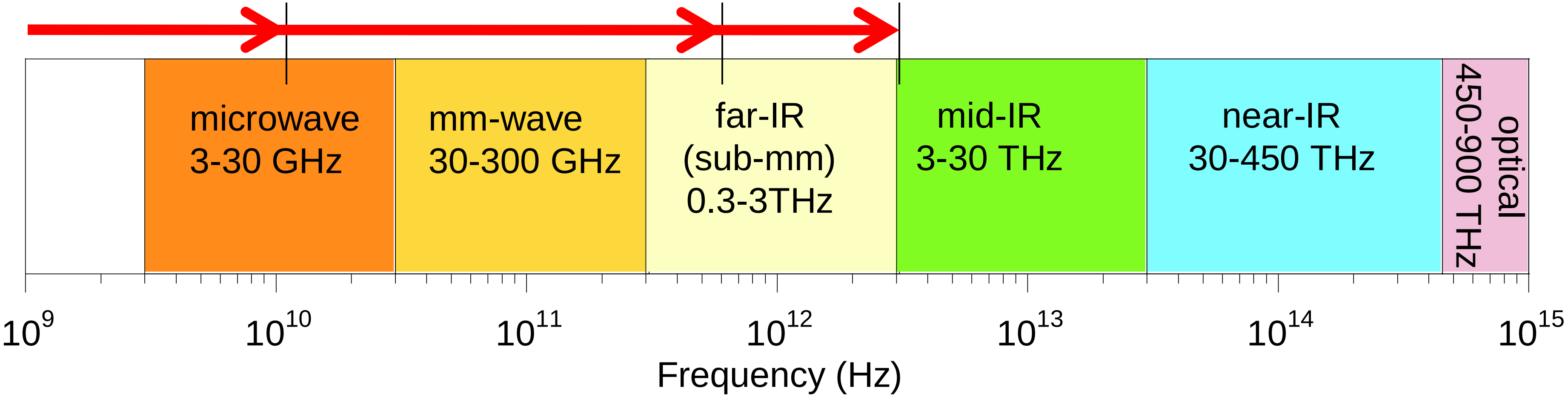
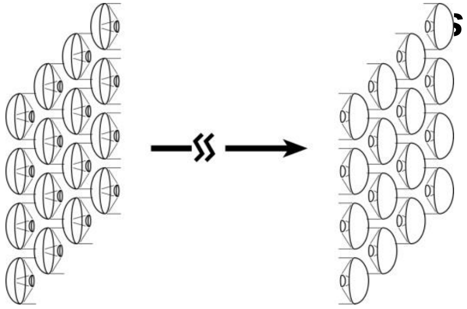
DC to Daylight. Far-Infrared Electronics

How high in frequency can we push electronics ?



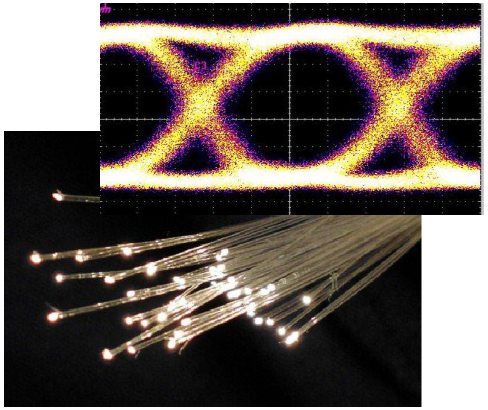
...and what would be do with it ?

0.1-0.4 THz radio: vast capacity



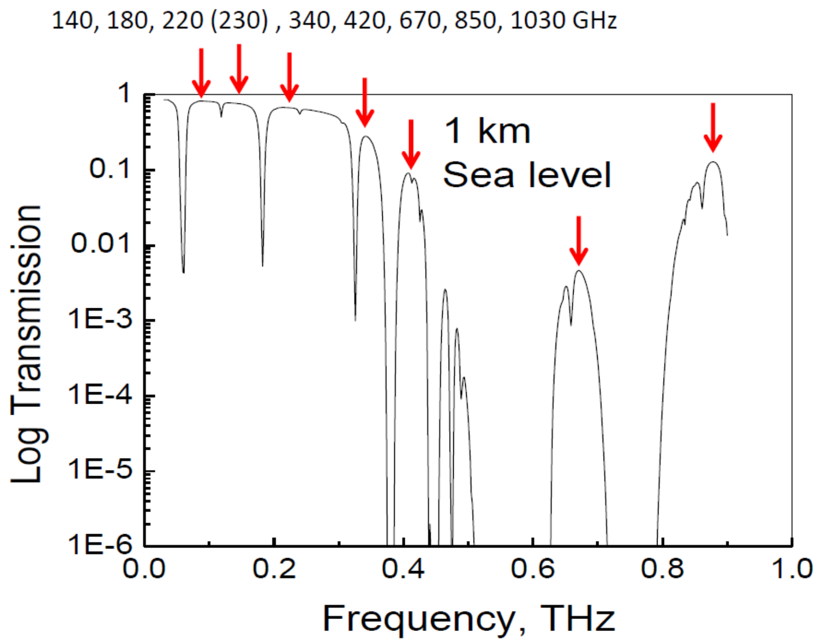
0.1-1 THz imaging systems

0.1-1 Tb/s optical fiber links

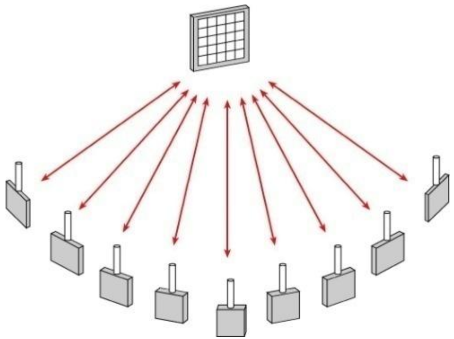


(Sub) mm-Wave Bands for Communications

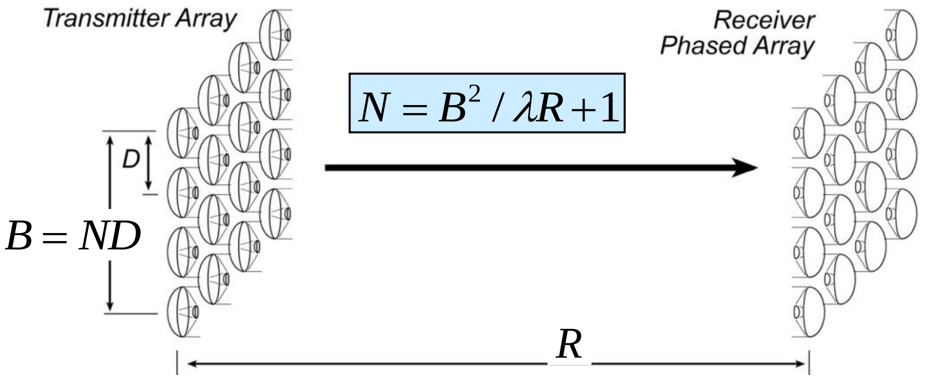
very large bandwidths available
→ large transmission capacity



short wavelengths→ many parallel channels



$$\text{angular resolution} \approx \frac{\text{wavelength}}{\text{array width}}$$



$$N = B^2/\lambda R + 1$$

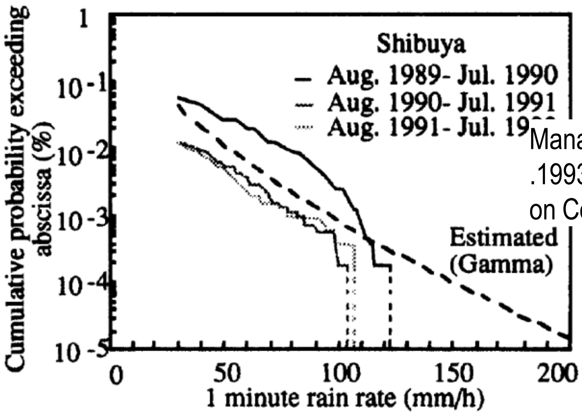
$$\#\text{channels} \propto (\text{aperture area})^2/(\text{wavelength}\cdot\text{distance})^2$$

50-400 GHz Links: ~750 meters Maximum Range

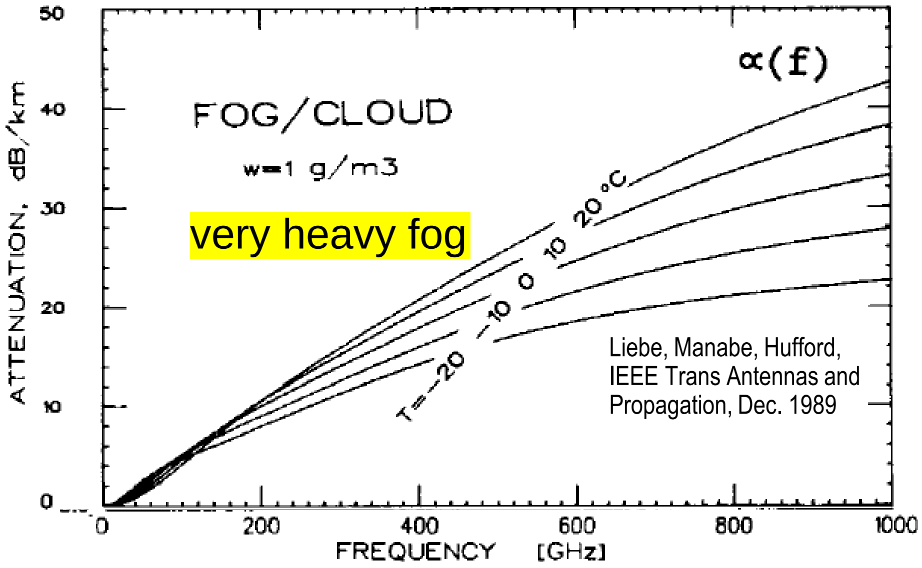
rain 50 mm/hr: 20 dB/km, 30-1000 GHz
150 mm/hr : 50 dB/km, 30-1000 GHz

Clouds, heavy fog:
~(25 dB/km)x(frequency/500 GHz)

90% Humidity: >30 dB/km above 300 GHz
nondominant below 250 GHz (Rosker 2007 IEEE IMS)



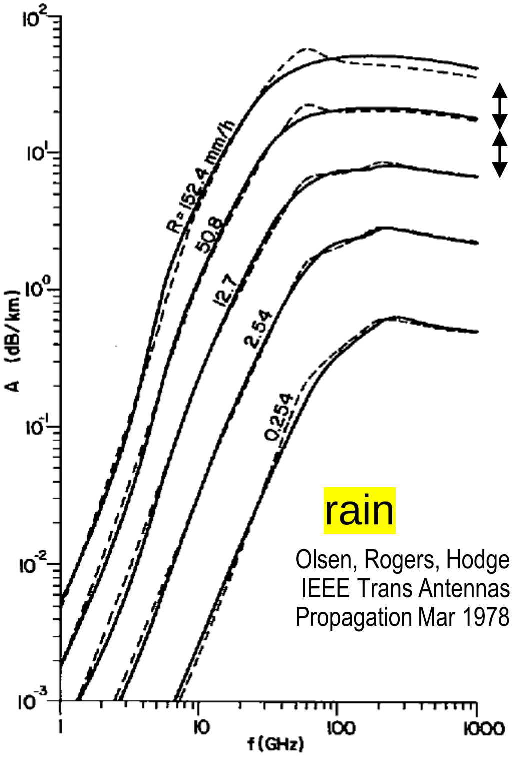
Manabe, Yoshida,
.1993 EEE Int. Conf.
on Communications,



very heavy fog

Liebe, Manabe, Hufford,
IEEE Trans Antennas and
Propagation, Dec. 1989

Fig. 1. SWD model predictions of attenuation $\alpha(f)$ and delay $\tau(f)$ for frequencies up to 1000 GHz assuming a water content, $w = 1$ g/m^3, and temperatures from -20 to $+20$°C (numerical examples are listed in Table I).

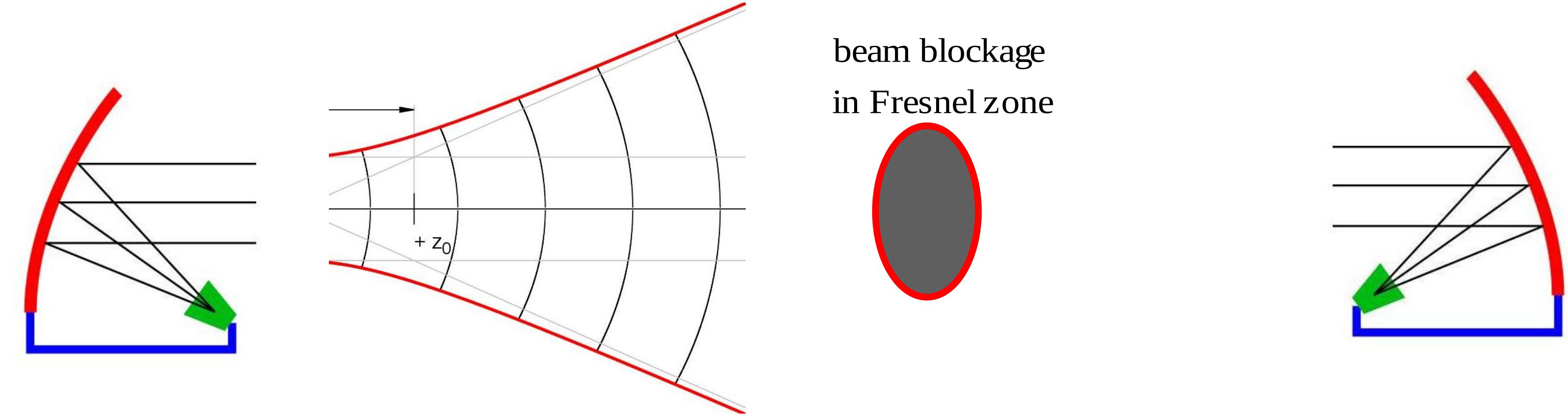


tropical deluge
heavy rain

rain

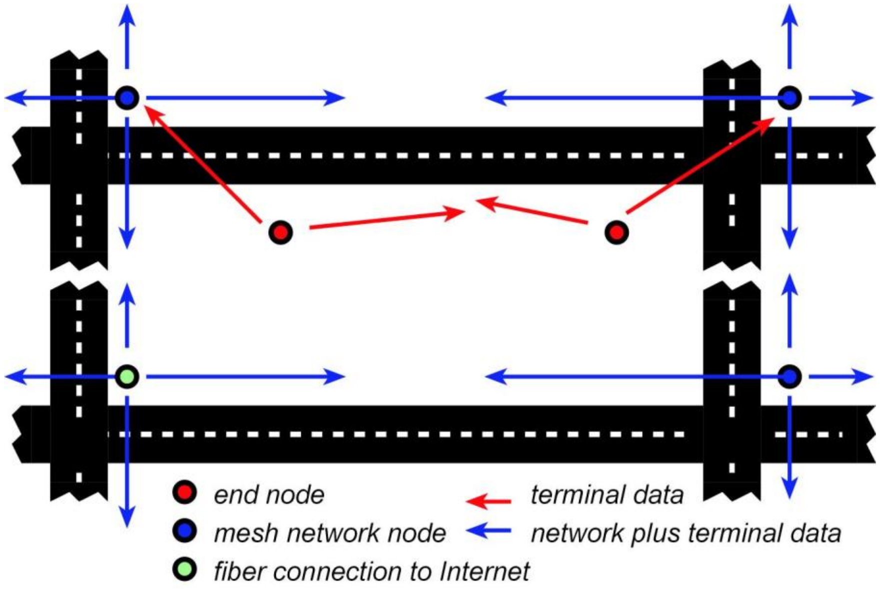
Olsen, Rogers, Hodge,
IEEE Trans Antennas &
Propagation Mar 1978

Short Wavelengths → Mesh Networks

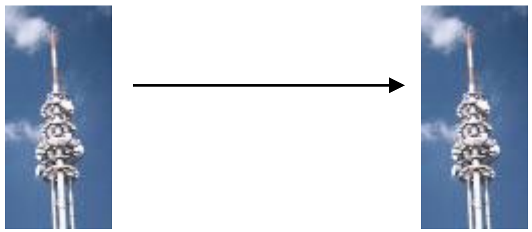


$\text{Fresnel zone area} \approx \text{wavelength} \cdot \text{distance}$ → Beam readily blocked

Mesh Networks
for Robust Service



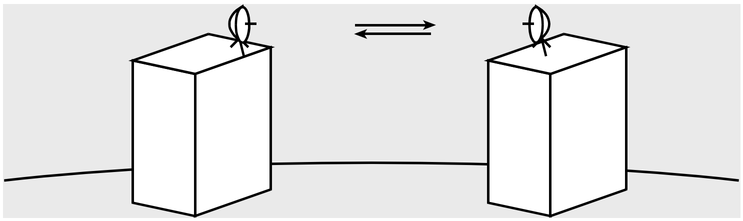
mm-Wave / THz Links Need Large Arrays



mm-wave Bands → Lots of bandwidth

$$\left(\frac{P_{received}}{P_{transmitted}}\right)=\left(\frac{1}{16\pi^2}\right)\left(\frac{\lambda^2}{R^2}\right)e^{-\alpha R}$$

short wavelength→ weak signal →short range

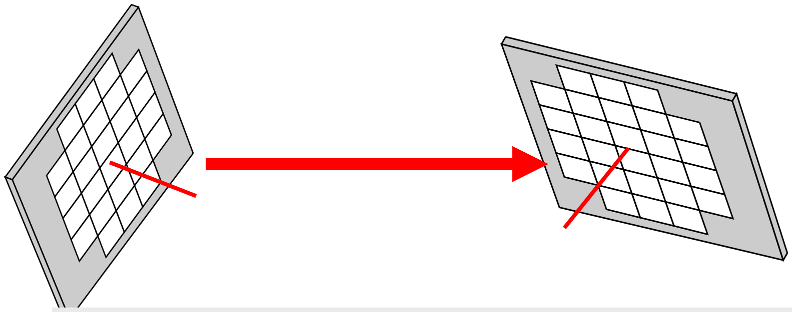


highly directional antenna → strong signal → long range

$$\left(\frac{P_{received}}{P_{transmitted}}\right)=\left(\frac{D_t D_r}{16\pi^2}\right)\left(\frac{\lambda^2}{R^2}\right)e^{-\alpha R}$$

narrow beam → must be aimed →no good for mobile

very narrow beam → must be precisely aimed →too expensive for telecom operators



monolithic beam steering arrays → strong signal, steerable

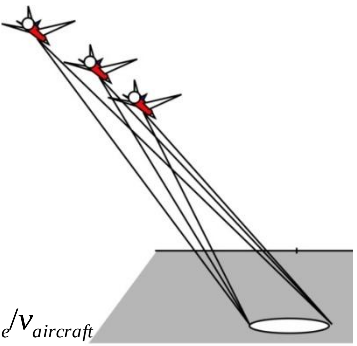
$$\frac{P_{received}}{P_{transmit}}=\frac{N_{receive}N_{transmit}}{16}\frac{\lambda^2}{R^2}e^{-\alpha R}$$

32 x 32 array → 60-90 dB increased SNR →vastly increased range

Large arrays needed above ~50 GHz
for adequate link range and capacity

RADAR / Imaging Needs Watts of Power, Low Noise Figure

220 GHz video-rate synthetic aperture radar



Azimuthal resolution $\delta_a = \lambda R f_{image}/v_{aircraft}$

$$\mathrm{SNR} = \frac{P_{trans}}{kTFf_{image}}\frac{1}{4\pi R^2}\frac{LH}{\lambda^2}\cdot\delta_a\delta_r\sin\psi\cdot\rho\cdot\frac{LH}{4\pi R^2}e^{-2\alpha R}$$

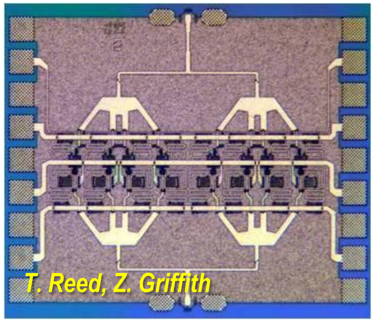
10 Hz video rate.
570 x 500 pixel image
5.5 cm resolution.
16 dB SNR
@10% reflectivity.

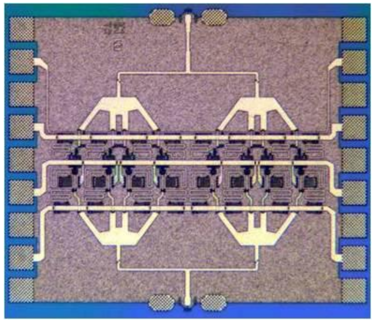
1 km range
100 mm x 44 mm total aperture,
32 receive elements.
250 m/s aircraft velocity
7 dB/km attenuation

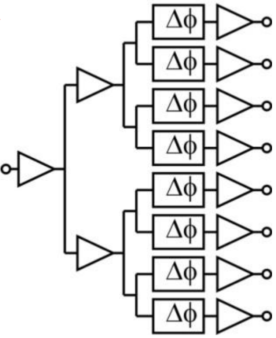
50 W transmitted power. 6 dB noise figure.

...to reach such levels with a solid-state source:

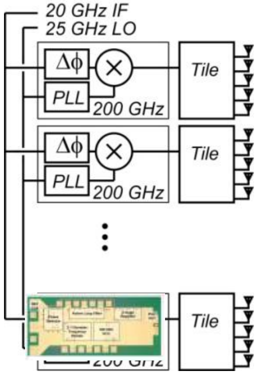
Present 220 GHz, 66 mW PA → Develop 200 mW PA → 8-element array tile IC: 1.6 W → 32 tiles/array→ 51 W







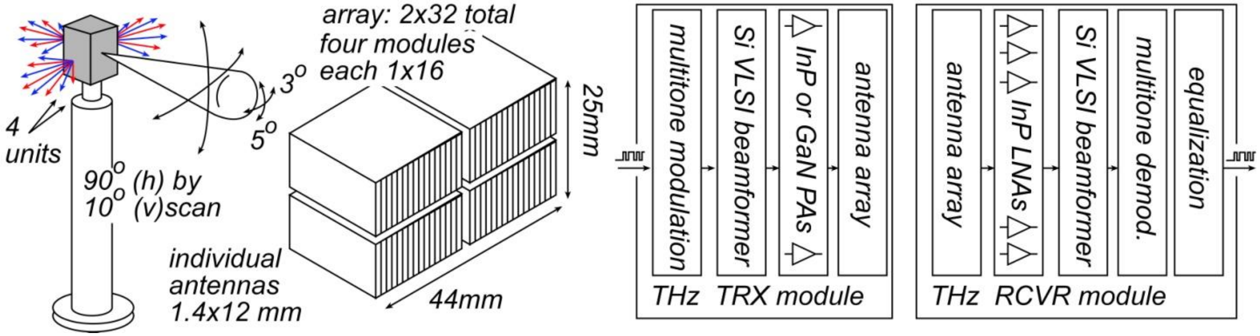
(200 GHz PLL is existing design by M. Seo)



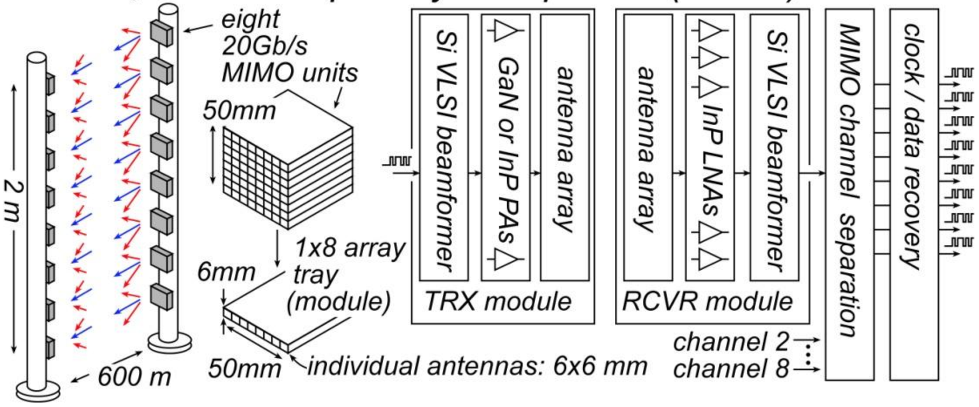
As a function of range, weather, and data rate, effective sub-mm-wave technologies must low noise figure, high transmit power, and/or moderate to large phased arrays

THz Communications Needs High Power, Low Noise

140 GHz, 10 Gb/s spatially scanned network node



340 GHz, 160Gb/s spatially multiplexed (MIMO) backhaul

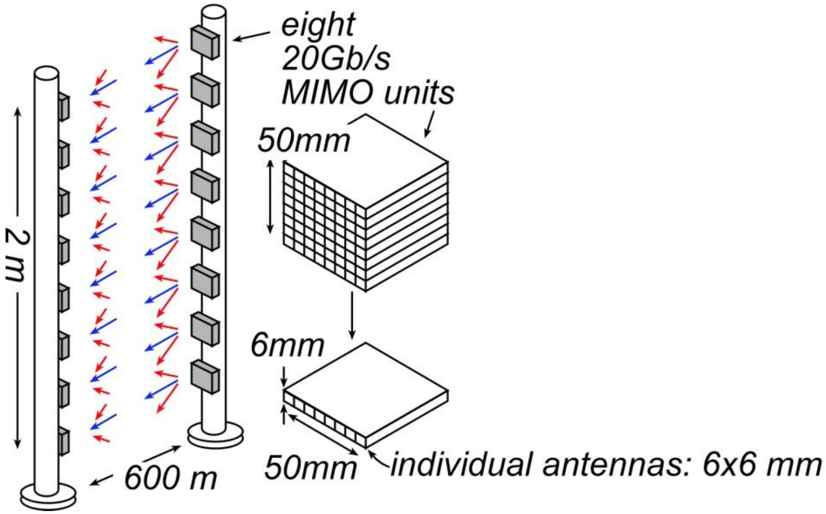


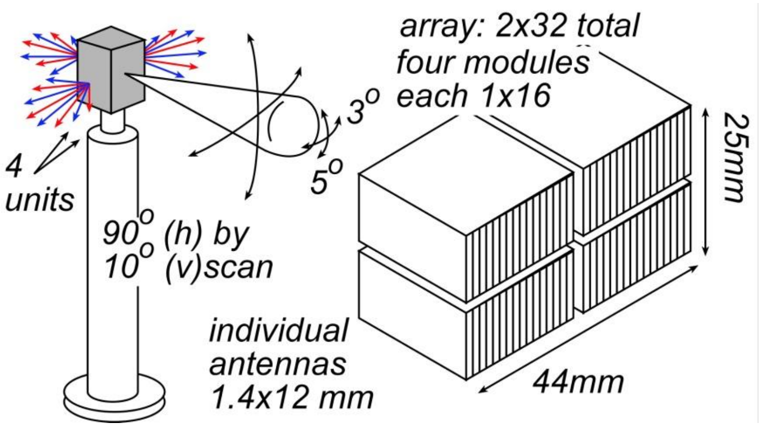
Real systems with real-world weather & design margins, 500-1000m range:

Will require:

3-7 dB Noise figure, 50mW- 1W output/element, 64-256 element arrays
→ InP or GaN PAs and LNAs, Silicon beamformer ICs

0.1-1 THz Comms Links: No Monolithic Arrays





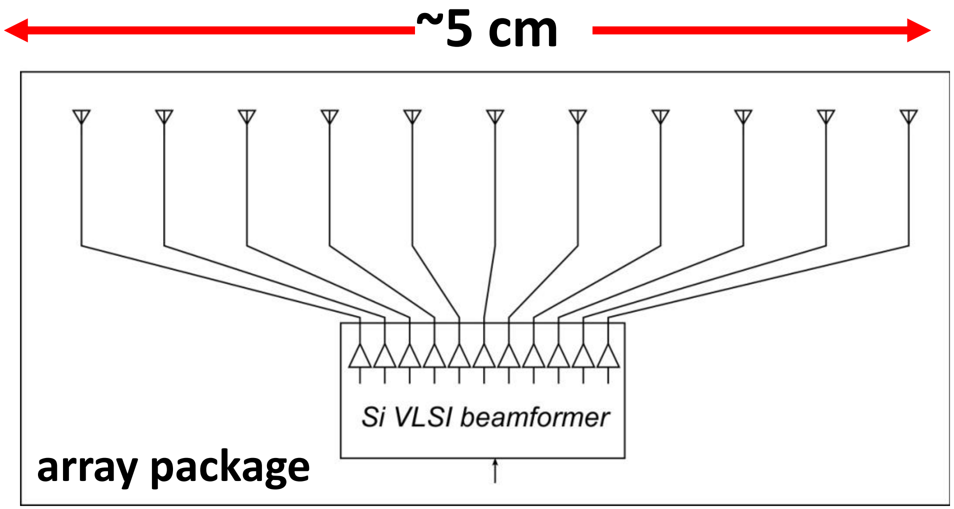
On-wafer antennas
substantial die area, have high losses

For useful directivity, aperture areas are ~ 25 cm^2.
→ vastly too large for an IC

0.1-1 THz Comms Links: Discrete LNAs & PAs

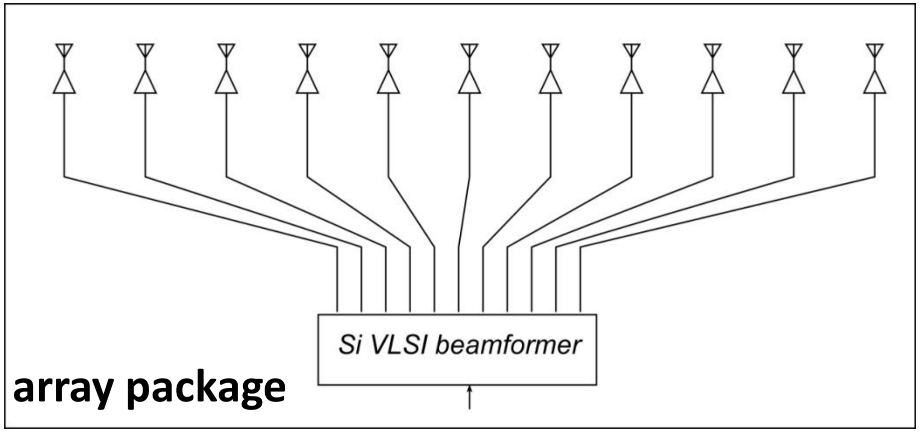
Monolithic PAs & LNAs

- long lines to antennas
- many dB losses on transmit
- many dB losses on transmit
- degraded noise, degraded power



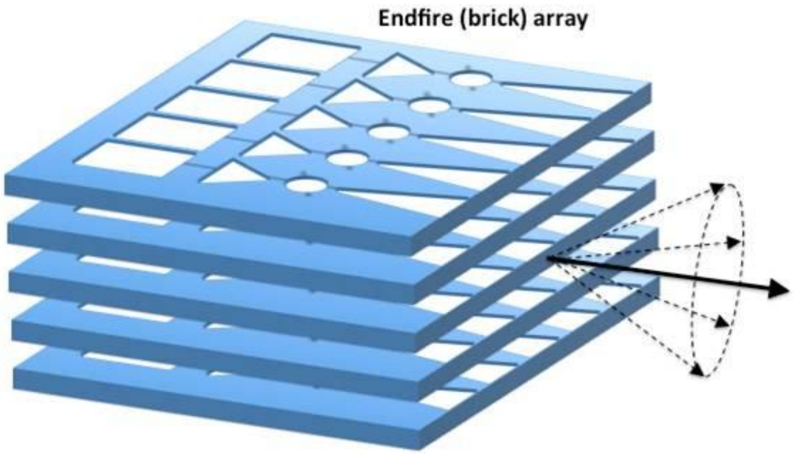
Discrete LNAs and PAs

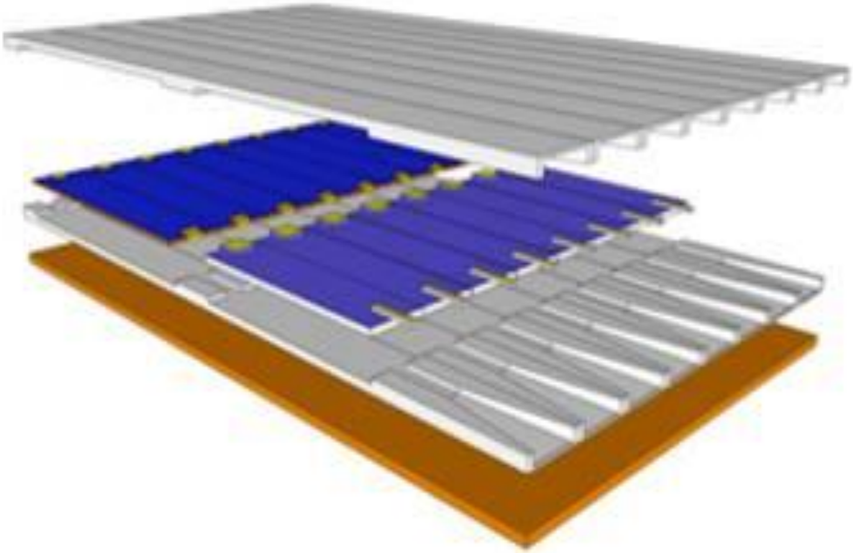
- LNAs & PAs: adjacent to antennas
- losses no longer impair link

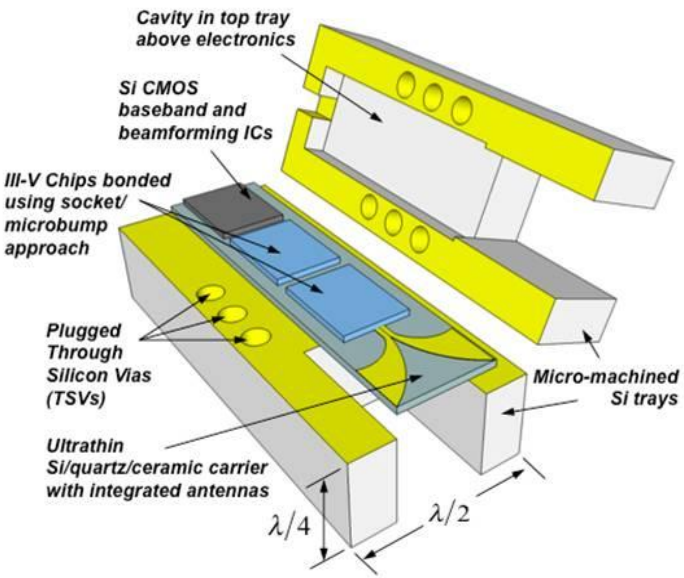


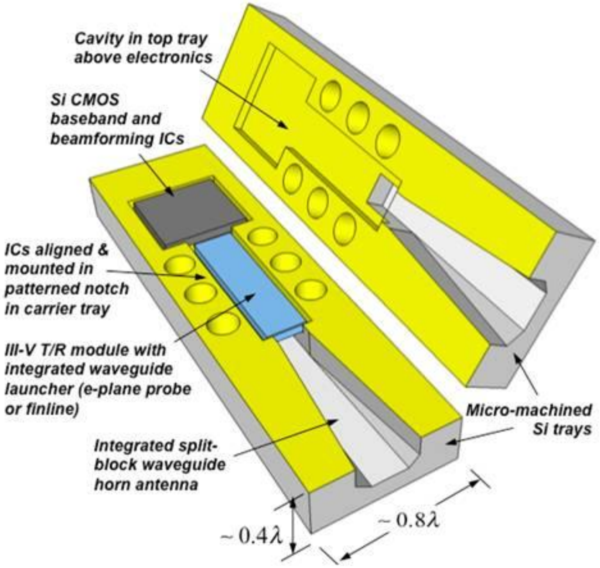
Given that we should not integrate the LNA and PA on the beamformer, it is to our benefit to use high-performance GaN & InP LNAs and PAs.

0.1-1 THz Comms Links: Array Design Concepts







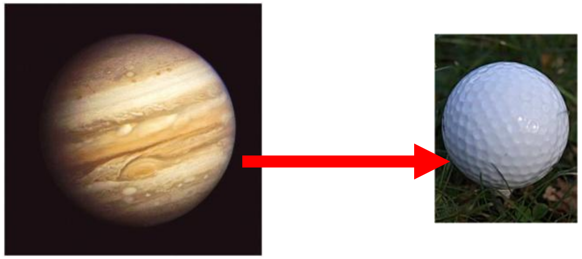


Concepts: Robert York, UCSB

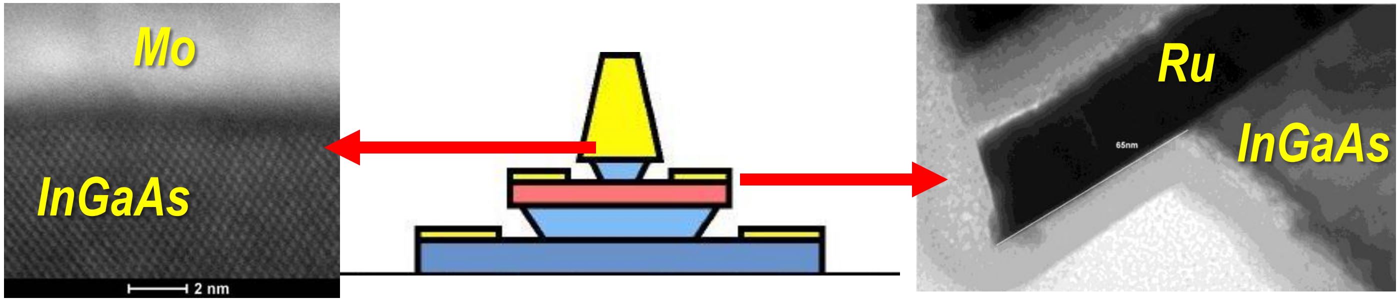
THz InP HBTs

THz & nm Transistors: what it's all about

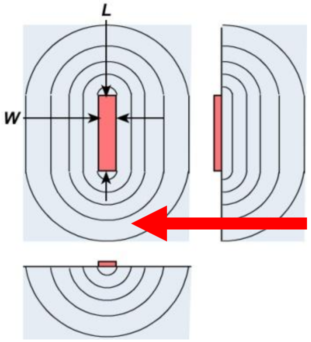
Metal-semiconductor interfaces (Ohmic contacts): very low resistivity
Dielectric-semiconductor interfaces (Gate dielectrics---FETs only): thin !



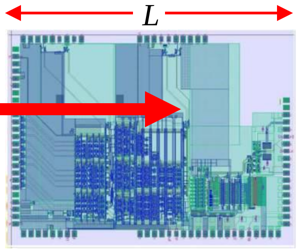
Ultra-low-resistivity (~0.25 Ω-μm^2), ultra shallow (1 nm), ultra-robust (0.2 A/μm^2) contacts



Heat

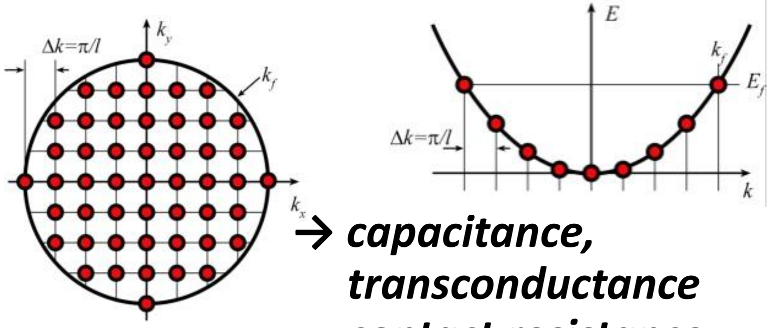


$$\Delta T_{IC} \propto \frac{P_{IC}}{K_{th} L}$$



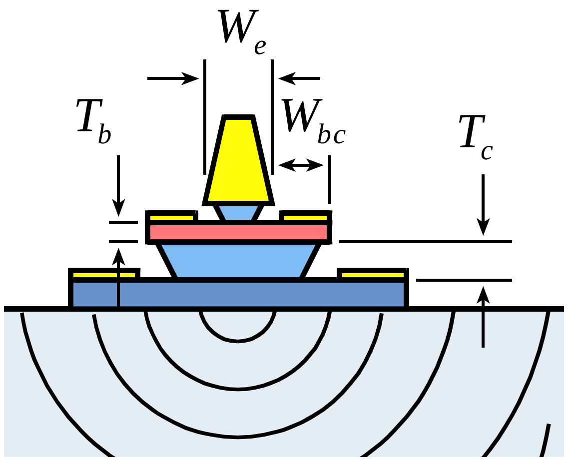
$$\Delta T_{\text{transistor}} \sim \frac{P}{\pi K_{th} L} \ln\left(\frac{L}{W}\right)$$

Available quantum states to carry current



→ ***capacitance, transconductance contact resistance***

Bipolar Transistor Design



$\left(\text{emitter length } L_E\right)$

$$\tau_b \approx T_b^2 / 2D_n$$

$$\tau_c = T_c / 2v_{sat}$$

$$C_{cb} = \varepsilon A_c / T_c$$

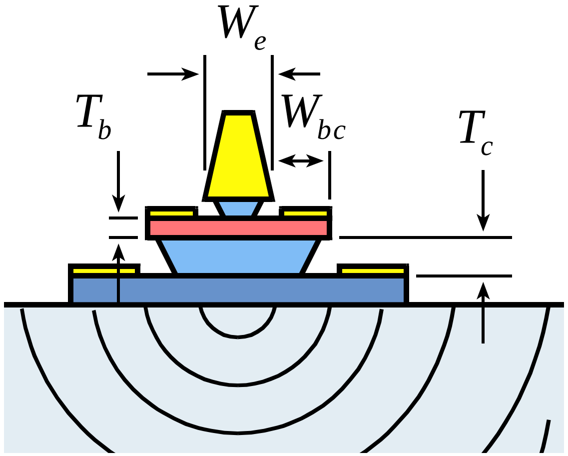
$$I_{c,\max} \propto v_{sat} A_e \left(V_{\text{ce,operating}} + V_{\text{ce,punch-through}}\right) / T_c^2$$

$$\Delta T \propto \frac{P}{L_E}\left[1 + \ln\left(\frac{L_e}{W_e}\right)\right]$$

$$R_{ex} = \rho_{\text{contact}} / A_e$$

$$R_{bb} = \rho_{\text{sheet}}\left(\frac{W_e}{12L_e} + \frac{W_{bc}}{6L_e}\right) + \frac{\rho_{\text{contact}}}{A_{\text{contacts}}}$$

Bipolar Transistor Design: Scaling



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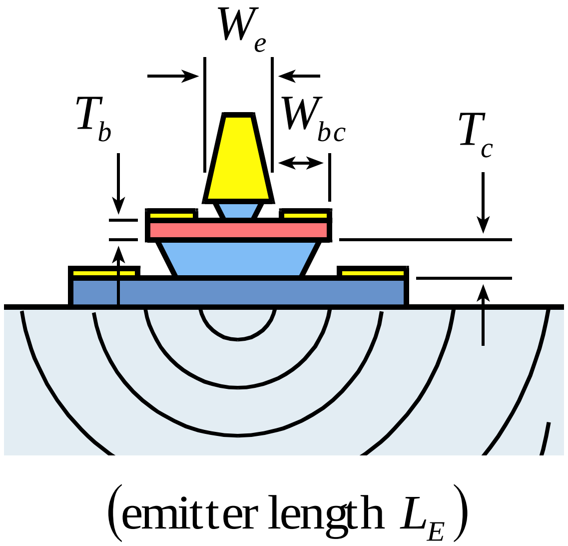
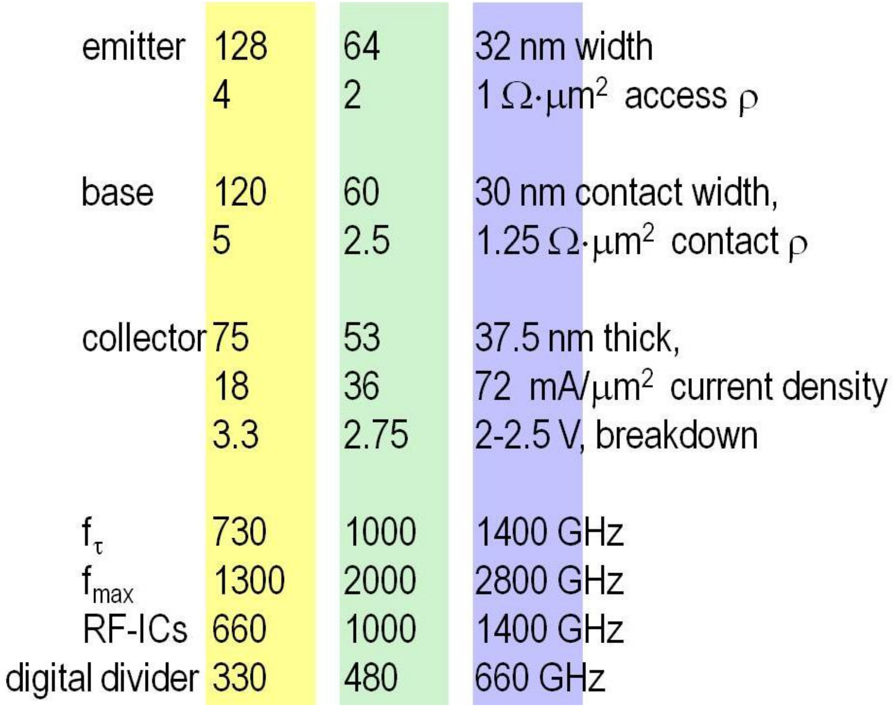
Scaling Laws, Scaling Roadmap

scaling laws: to double bandwidth

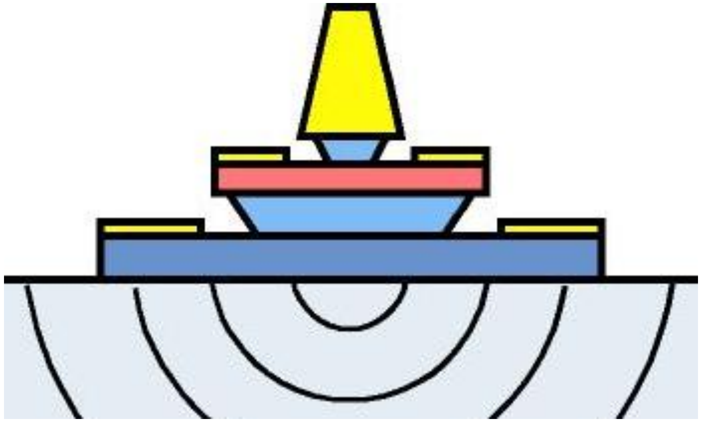
HBT parameter	change
emitter & collector junction widths	decrease 4:1
current density (mA/μm^2)	increase 4:1
current density (mA/μm)	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1





emitter	128	64	32 nm width
	4	2	1 $\Omega\cdot\mu$m^2 access ρ
base	120	60	30 nm contact width,
	5	2.5	1.25 $\Omega\cdot\mu$m^2 contact ρ
collector	75	53	37.5 nm thick,
	18	36	72 mA/μm^2 current density
	3.3	2.75	2-2.5 V, breakdown
f_τ	730	1000	1400 GHz
f_{max}	1300	2000	2800 GHz
RF-ICs	660	1000	1400 GHz
digital divider	330	480	660 GHz

HBT Fabrication Process Must Change... Greatly



32 nm width base & emitter contacts...self-aligned

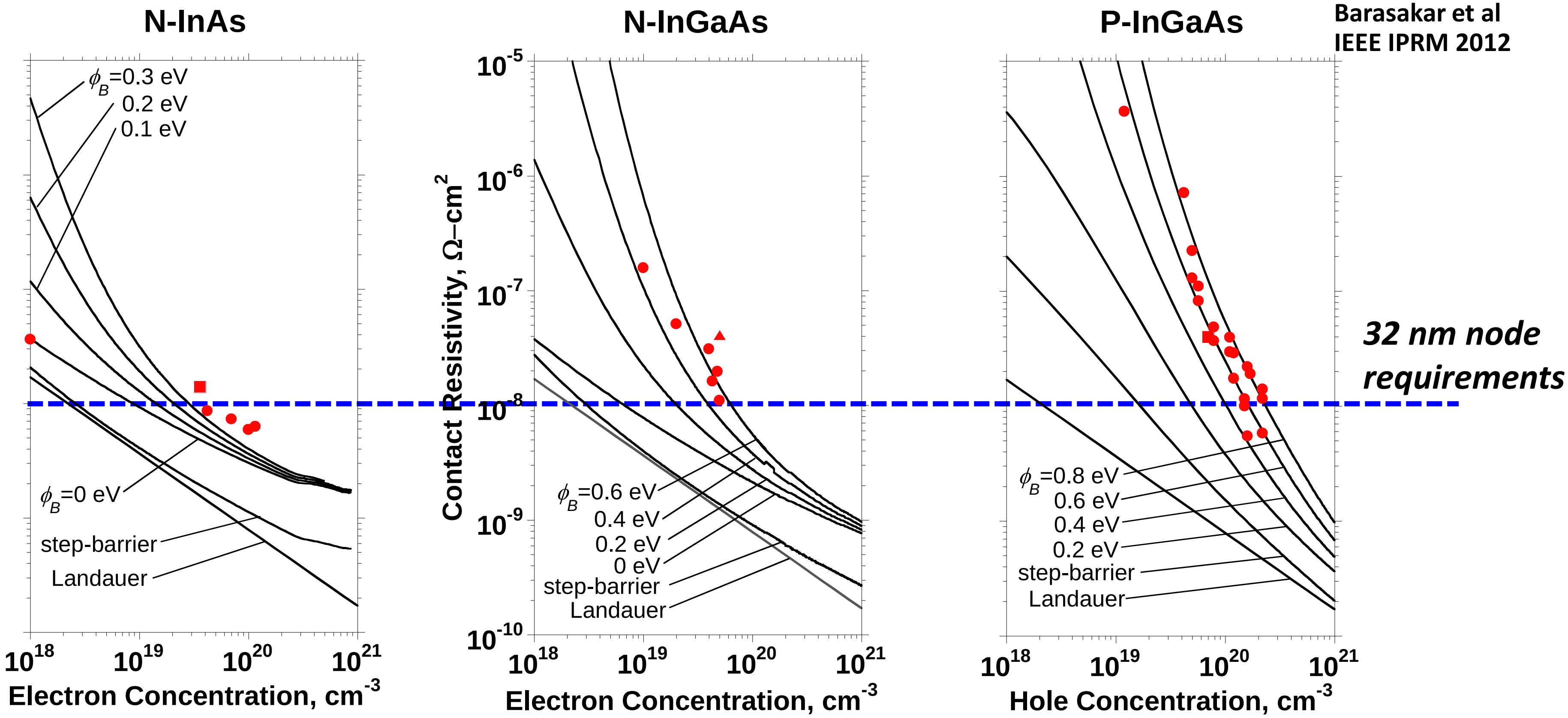
32 nm width emitter semiconductor junctions

Contacts:

1 Ω-μm^2 resistivities
70 mA/μm^2 current density
~1 nm penetration depths
→ refractory contacts

nm III-V FET, Si FET processes have similar requirements

Ultra Low-Resistivity Refractory *In-Situ* Contacts



Barasakar et al IEEE IPRM 2012

In-situ**: *avoids surface contaminants***

Refractory**: *robust under high-current operation***

Low penetration depth, ~ 1 nm

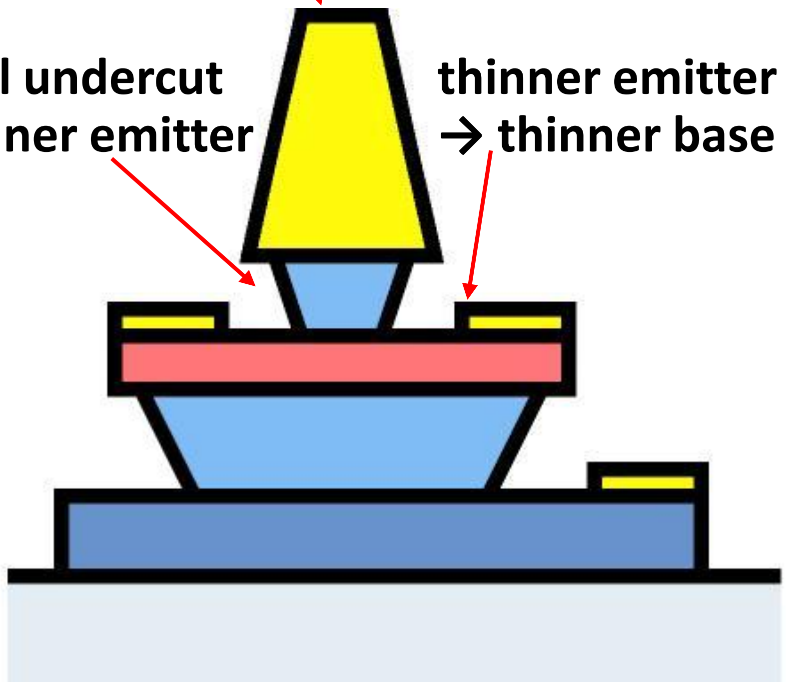
Contact performance sufficient for 32 nm /2.8 THz node.

HBT Fabrication Process Must Change... Greatly

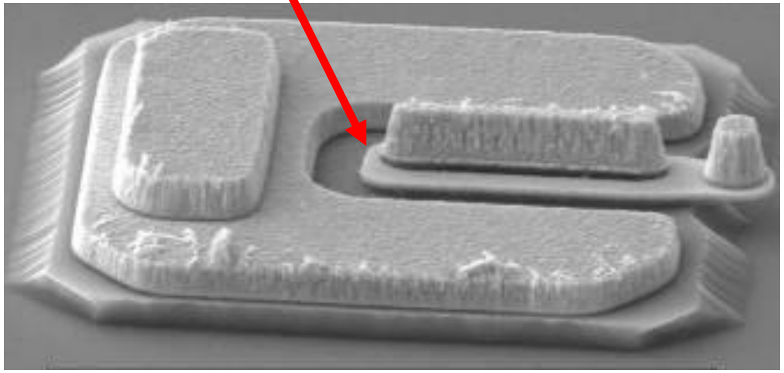
tall, narrow contacts: liftoff fails !

control undercut
→ thinner emitter

thinner emitter
→ thinner base metal

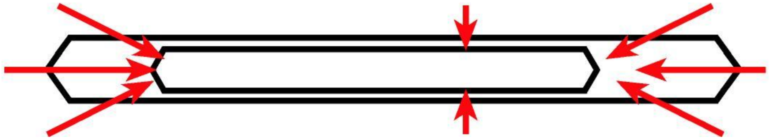


thinner base metal
→ excess base metal resistance

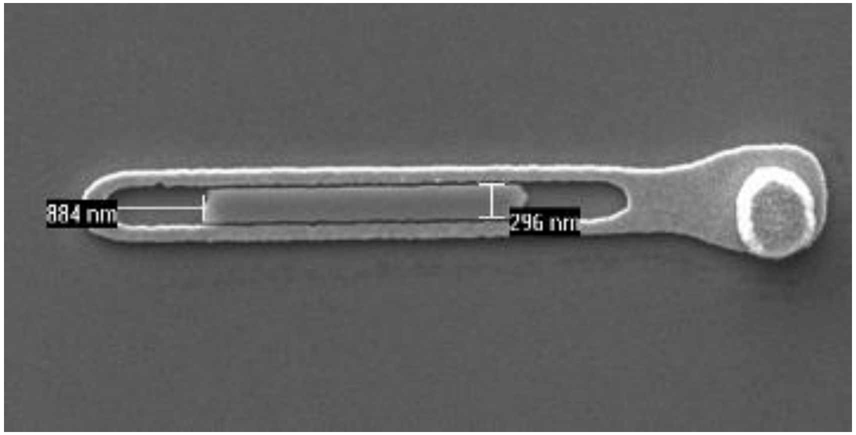


Undercutting of emitter ends

{101}A planes: fast



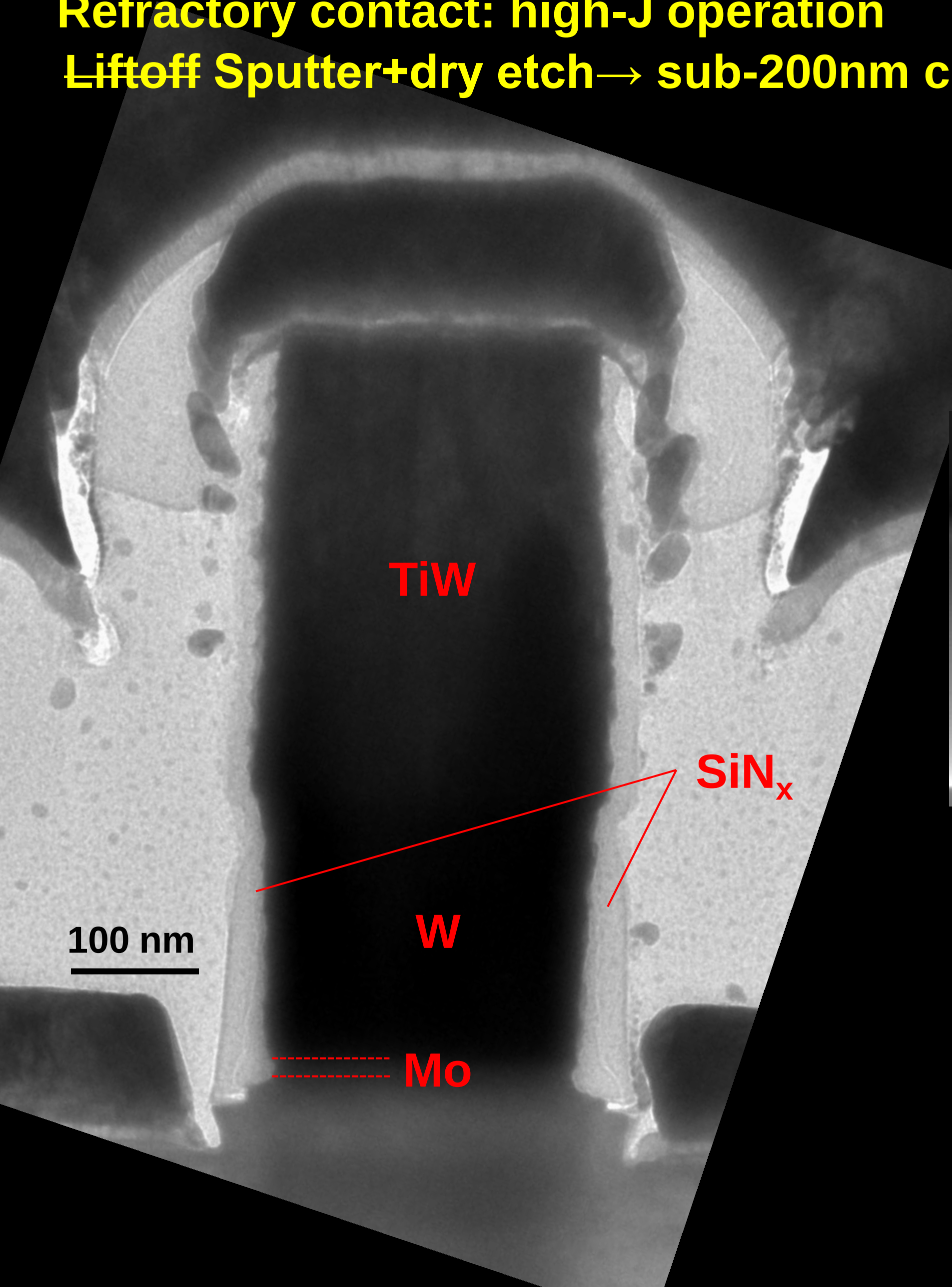
{111}A planes: slow

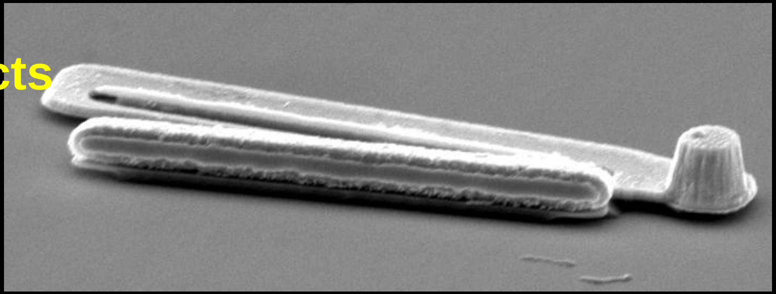


Sub-200-nm Emitter Anatomy

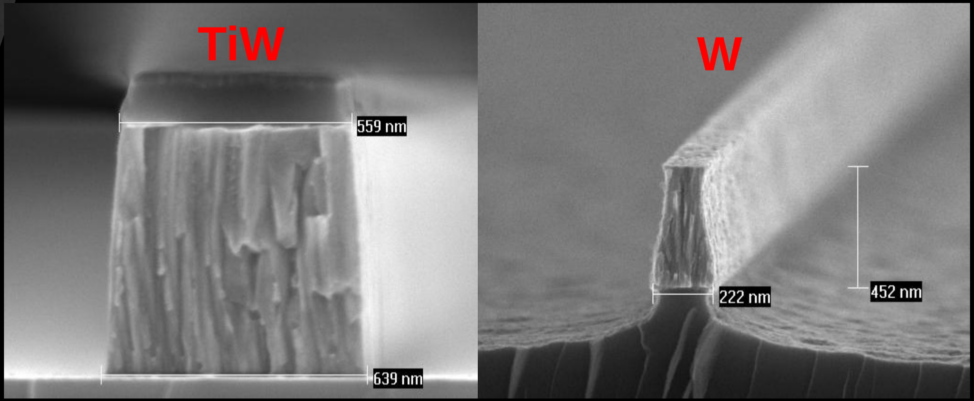
Refractory contact: high-J operation

~~Liftoff~~ Sputter+dry etch→ sub-200nm contacts





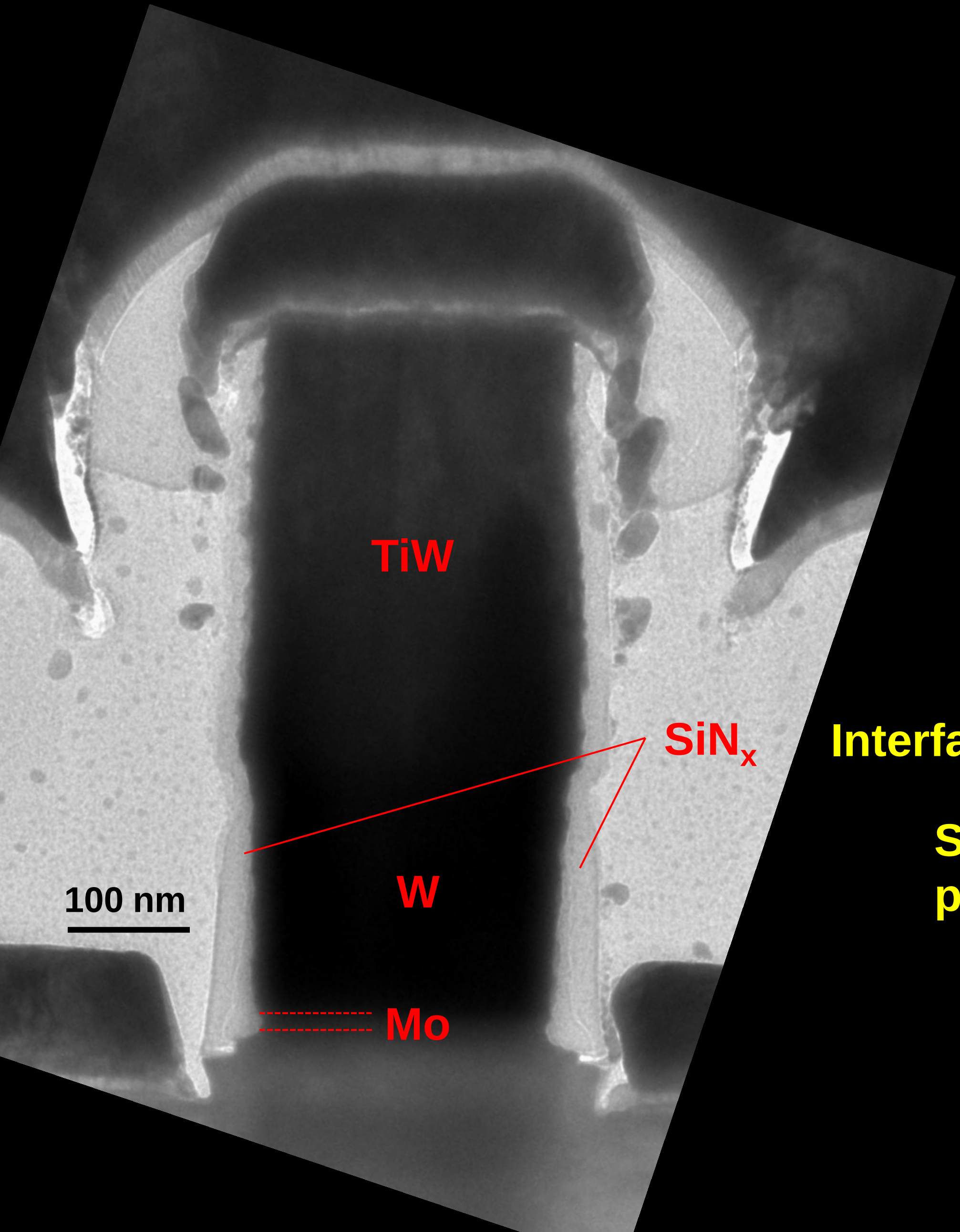
High-stress emitters fall off during subsequent



Single sputtered metal has non-vertical etch profile

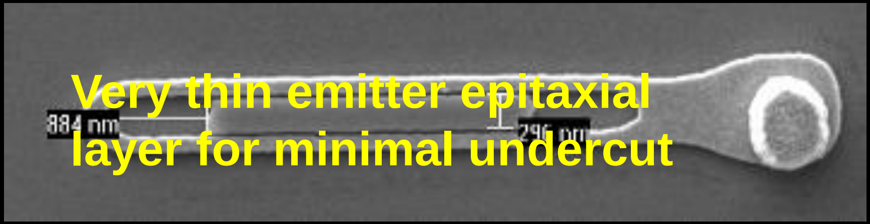
slide: E. Lobisser. HBT: V. Jain. Process: Jain & Lobisser

Sub-200-nm Emitter Anatomy



Hybrid sputtered metal stack for low-stress, vertical profile

W/TiW interfacial discontinuity enables base contact lift-off



Very thin emitter epitaxial layer for minimal undercut

Semiconductor wet etch undercuts emitter contact

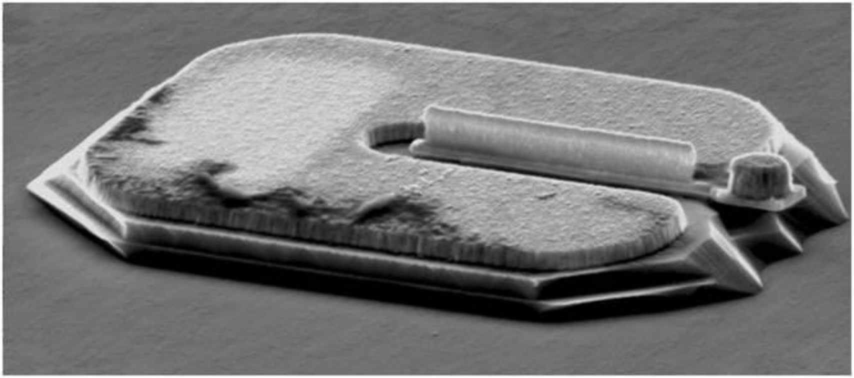
Interfacial Mo blanket-evaporated for low ρ_c

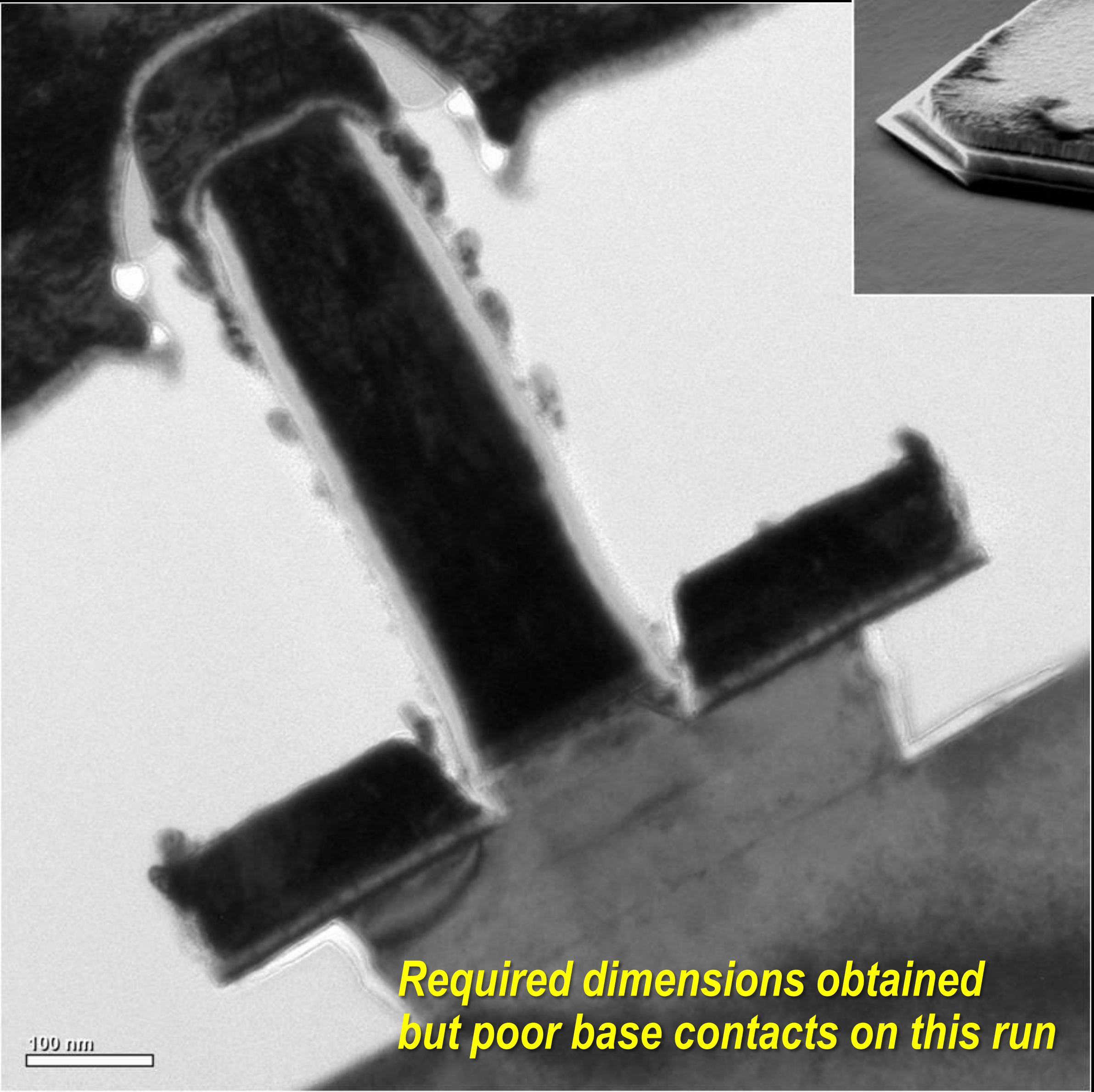
SiNx sidewalls protect emitter contact, prevent emitter-base shorts during liftoff

slide: E. Lobisser. HBT: V. Jain. Process: Jain & Lobisser

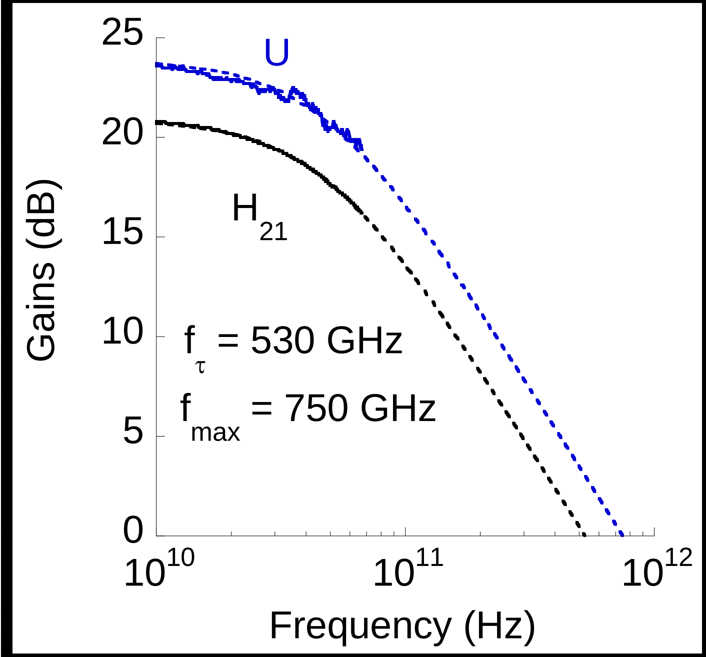
RF Data: 25 nm thick base, 75 nm Thick Collector

140 nm wide emitter
380 nm wide collector



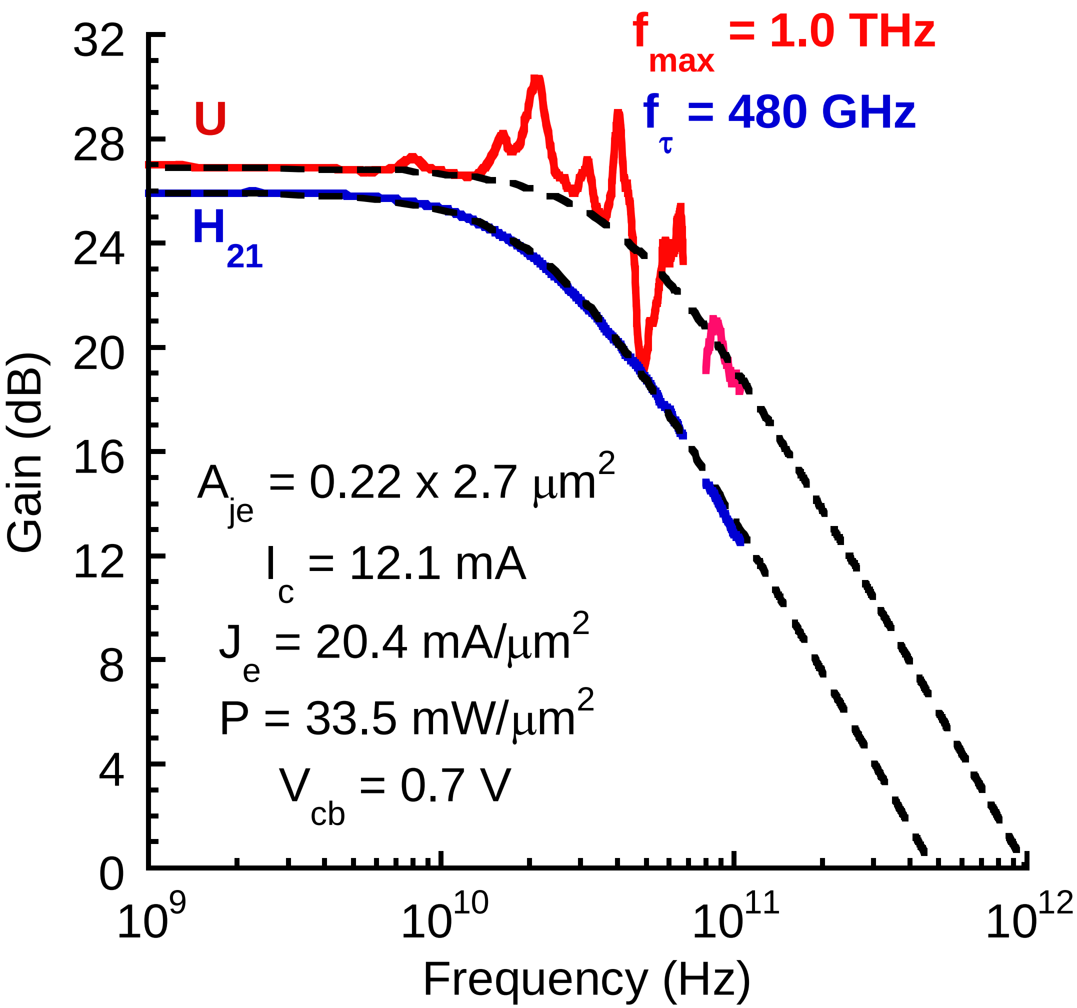


Required dimensions obtained but poor base contacts on this run

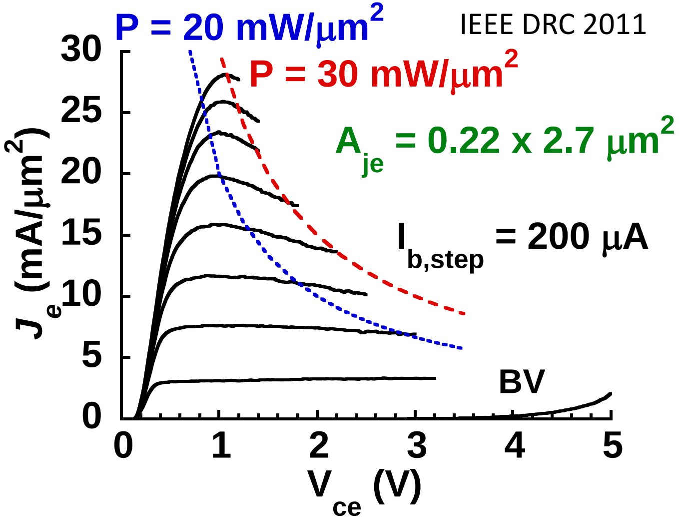


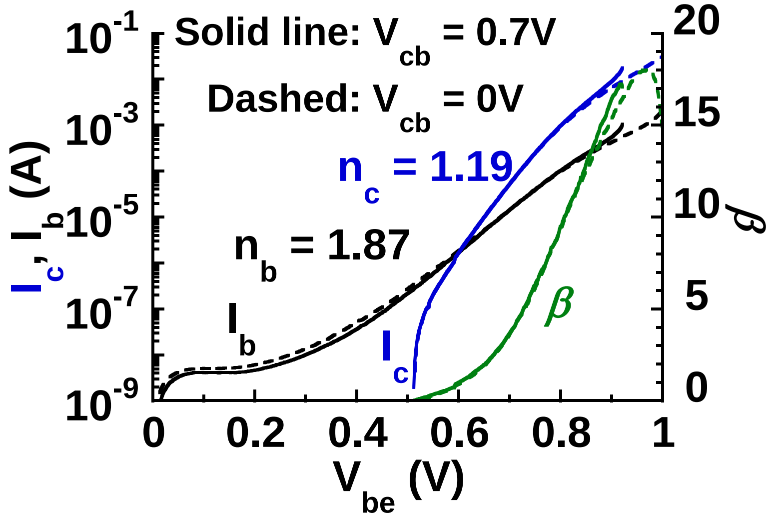
E. Lobisser, ISCS 2012, August, Santa Barbara

DC, RF Data: 100 nm Thick Collector



Jain et al
IEEE DRC 2011





THz InP HBTs From Teledyne

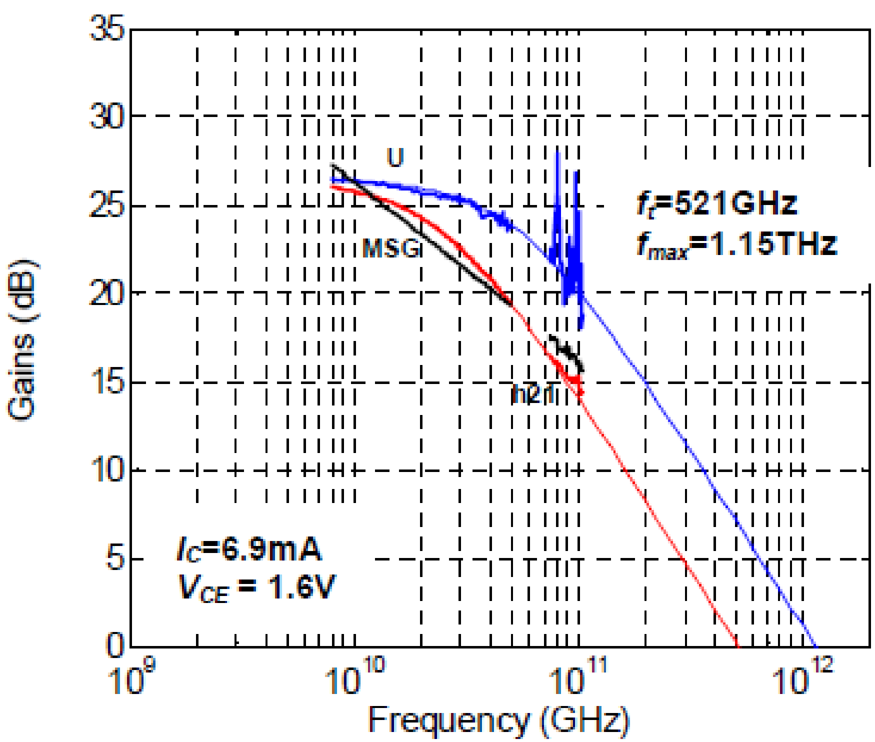


Fig. 3 RF gains of 0.13x2μm^2 HBT

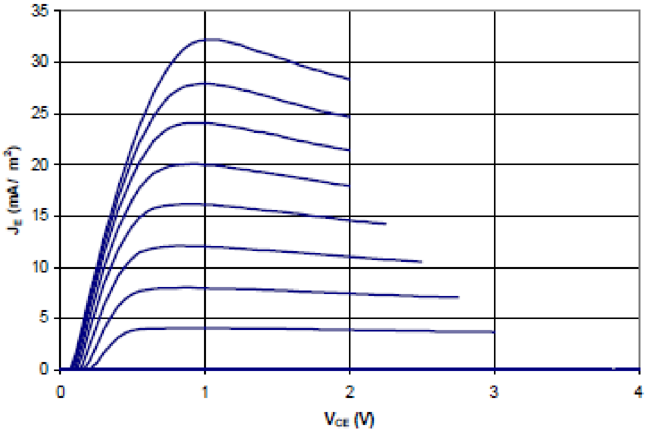


Fig. 2 Common-emitter IV characteristics of 130nm HBT normalized to emitter area

130nm InP DHBTs with f_t>0.52THz and f_{max} >1.1THz

M. Urteaga[1], R. Pierson[1], P. Rowell[1], V. Jain[2], E. Lobisser[2], M.J.W. Rodwell[2]
[1]Teledyne Scientific Company, Thousand Oaks, CA 93160. [2]Department of ECE, University of California, Santa Barbara, CA 93106. E-mail: murteaga@teledyne-si.com

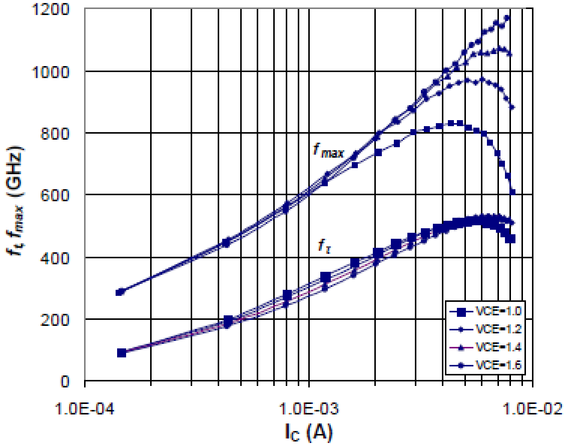


Fig. 4 f_t and f_{max} versus collector current at varying values of V_{CE} for 0.13x2μm^2 HBT

Urteaga et al, DRC 2011, June

InP HBT: Key Features

512 nm node:

high-yield "pilot-line" process, ~4000 HBTs/IC

256 nm node:

Power Amplifiers: >0.5 W/mm @ 220 GHz
highly competitive mm-wave / THz power technology

128 nm node:

>500 GHz f_τ , >1.1 THz f_{max}, ~3.5 V breakdown
breakdown* f_τ = 1.75 THz*Volts
highly competitive mm-wave / THz power technology

64 nm (2 THz) & 32 nm (2.8 THz) nodes:

Development needs major effort, but no serious scaling barriers

1.5 THz monolithic ICs are feasible.

Can we make a 1 THz SiGe Bipolar Transistor ?

Simple physics clearly drives scaling

transit times, C_{cb}/I_c

→ thinner layers, higher current density

high power density → narrow junctions

small junctions→ low resistance contacts

Key challenge: Breakdown

15 nm collector → very low breakdown

Also required:

low resistivity Ohmic contacts to Si

very high current densities: heat

	InP	SiGe	
emitter	64	18	nm width
	2	**0.6**	$\Omega\cdot\mu m^2$ access ρ
base	64	18	nm contact width,
	2.5	**0.7**	$\Omega\cdot\mu m^2$ contact ρ
collector	53	**15**	nm thick
	36	125	$mA/\mu m^2$
	2.75	**1.3?**	V, breakdown
f_τ	**1000**	**1000**	GHz
f_{max}	**2000**	**2000**	GHz
PAs	1000	1000	GHz
digital	480	480	GHz
(2:1 static divider metric)			

Assumes collector junction 3:1 wider than emitter.

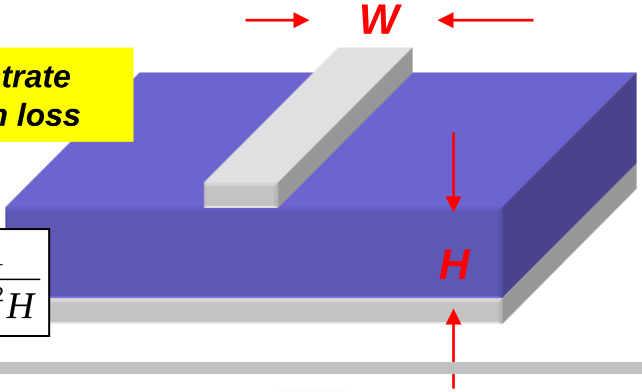
Assumes SiGe contacts no wider than junctions

0.1-1THz
IC Design

III-V MIMIC Interconnects -- Classic Substrate Microstrip

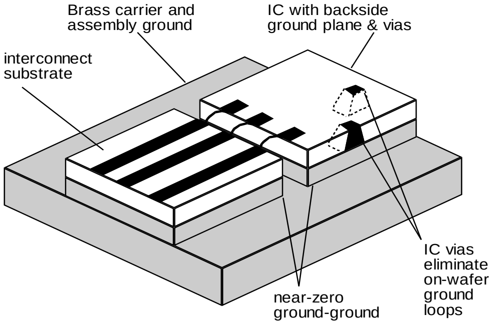
Thick Substrate
→ low skin loss

$$\alpha_{skin} \propto \frac{1}{\varepsilon_r^{1/2} H}$$

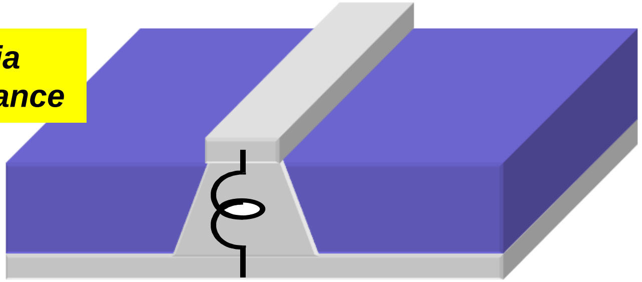


Zero ground inductance in package

No ground plane breaks in IC

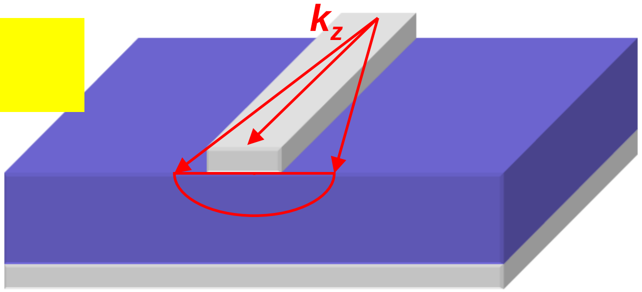


High via inductance



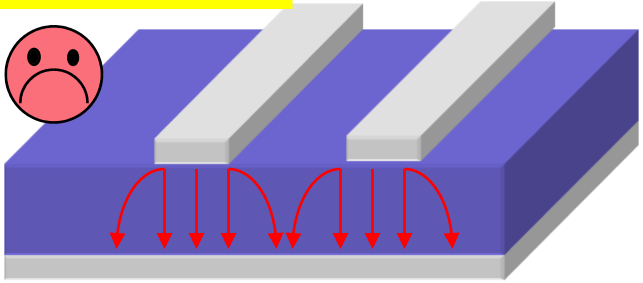
12 pH for 100 μm substrate -- 7.5 Ω @ 100 GHz

TM substrate mode coupling



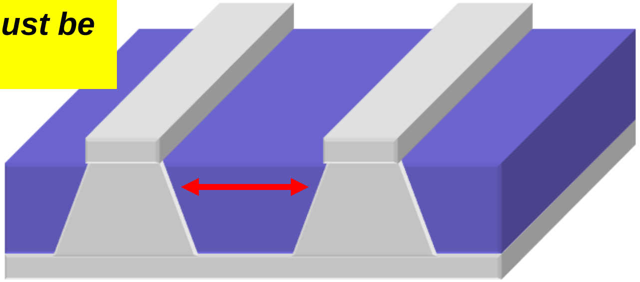
Strong coupling when substrate approaches ~λ_d / 4 thickness

lines must be widely spaced



Line spacings must be ~3(substrate thickness)*

ground vias must be widely spaced

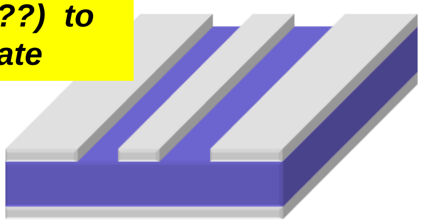


all factors require very thin substrates for >100 GHz ICs
→ lapping to ~50 μm substrate thickness typical for 100+ GHz

Coplanar Waveguide

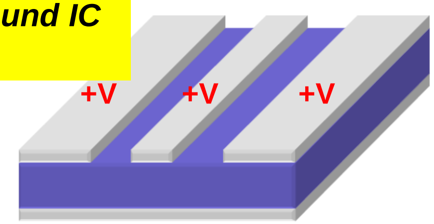
No ground vias
No need (???) to thin substrate

☺

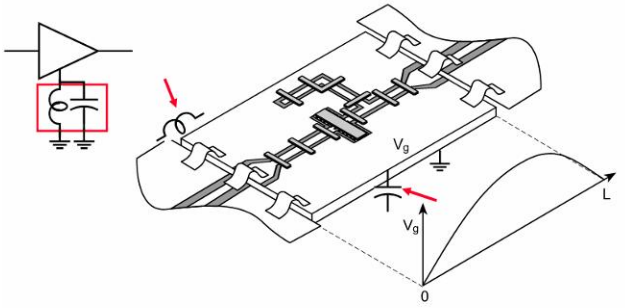


Hard to ground IC to package

☹

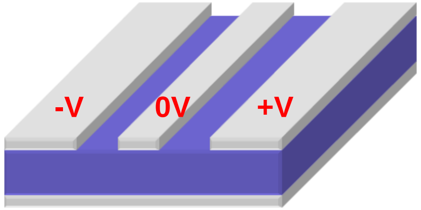


Parasitic microstrip mode



ground plane breaks → loss of ground integrity

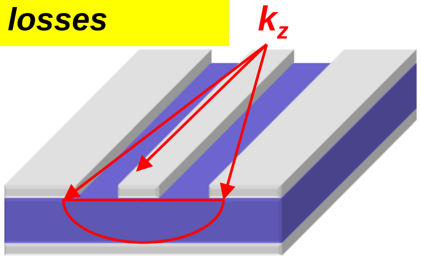
☹



Parasitic slot mode

substrate mode coupling or substrate losses

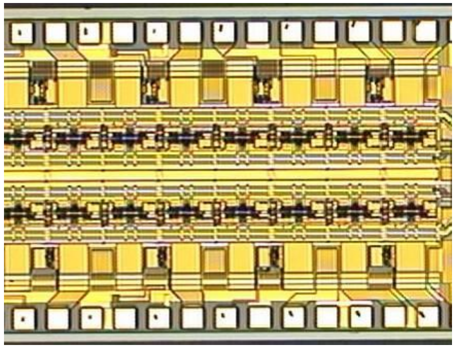
☹



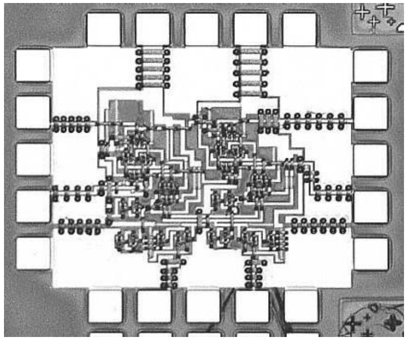
III-V: semi-insulating substrate→ substrate mode coupling

Silicon conducting substrate → substrate conductivity losses

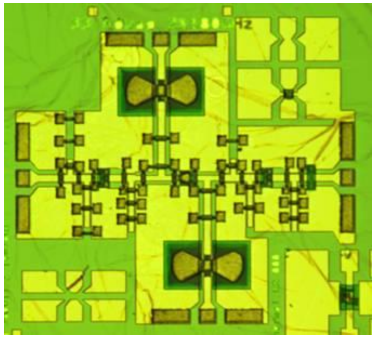
Repairing ground plane with ground straps is effective only in simple ICs
In more complex CPW ICs, ground plane rapidly vanishes
→ common-lead inductance → strong circuit-circuit coupling



40 Gb/s differential TWA modulator driver
note CPW lines, fragmented ground plane



35 GHz master-slave latch in CPW
note fragmented ground plane



175 GHz tuned amplifier in CPW
note fragmented ground plane

poor ground integrity ☹

↓

loss of impedance control ☹

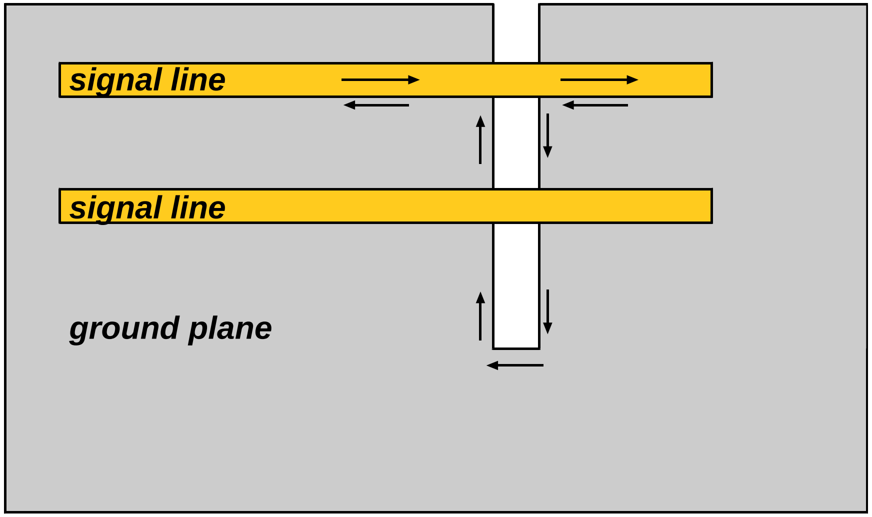
↓

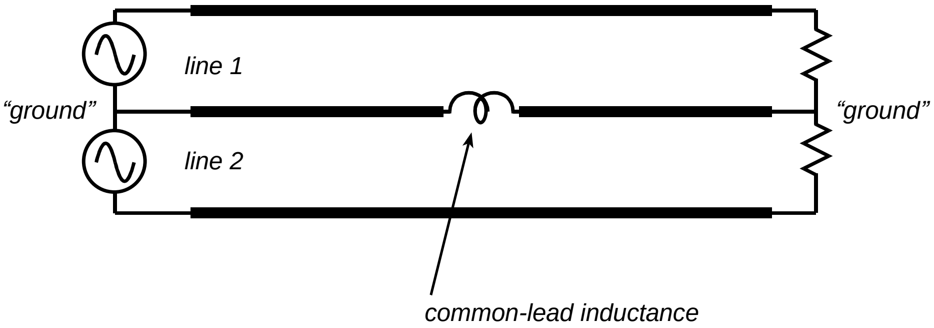
ground bounce ☹

↓

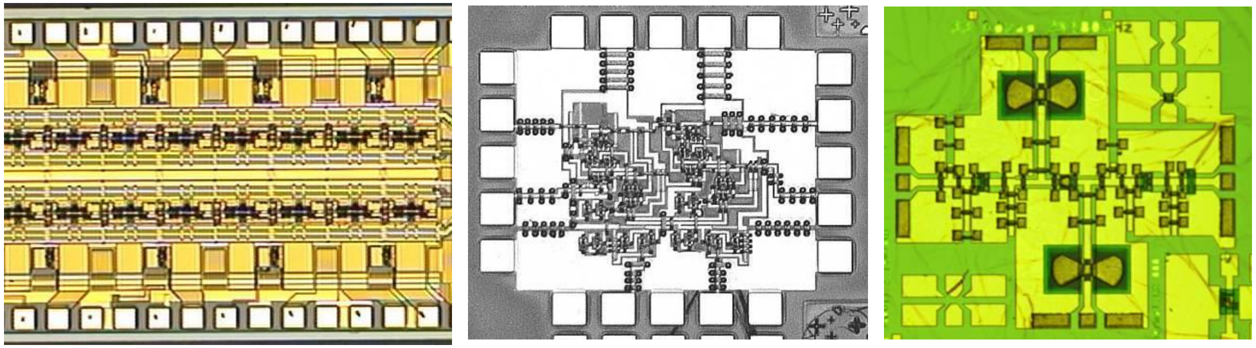
coupling, EMI, oscillation ☹

If It Has Breaks, It Is Not A Ground Plane !





coupling / EMI due to poor ground system integrity is common in high-frequency systems
whether on PC boards
...or on ICs.



III-V MIMIC Interconnects -- Thin-Film Microstrip

narrow line spacing → IC density ☺

no substrate radiation, no substrate losses ☺

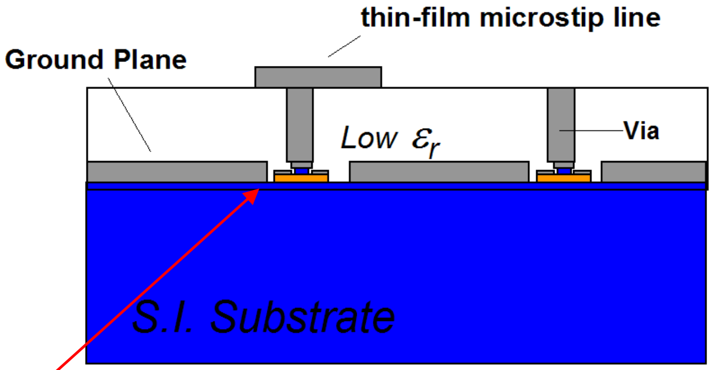
fewer breaks in ground plane than CPW ☺

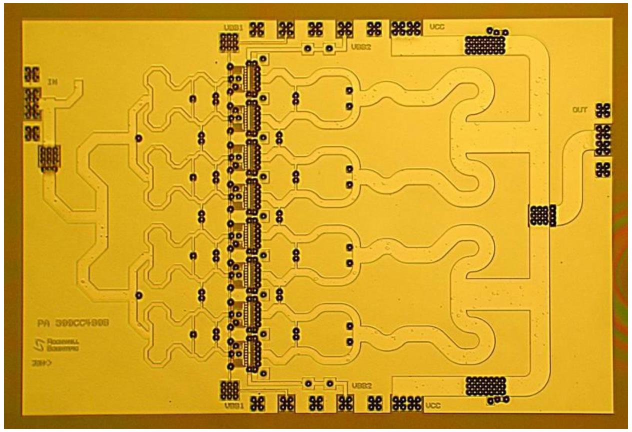
... but ground breaks at device placements ☹

still have problem with package grounding ☹

...need to flip-chip bond

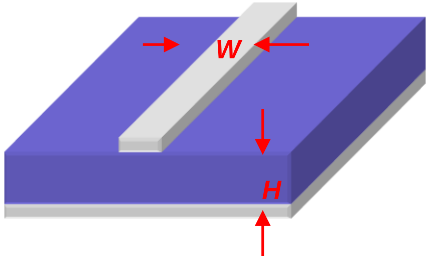
thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines ☹





InP 34 GHz PA
(Jon Hacker , Teledyne)

$$Z_o \sim \frac{\eta_o}{\varepsilon_r^{1/2}}\left(\frac{H}{W+H}\right)$$



III-V MIMIC Interconnects -- Inverted Thin-Film Microstrip

narrow line spacing → IC density 🙂

Some substrate radiation / substrate losses 🙁

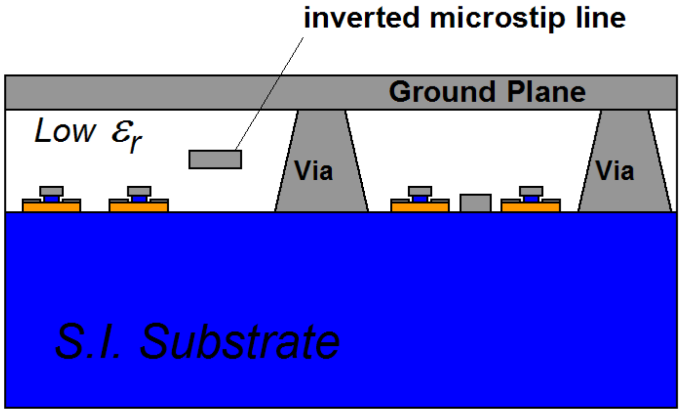
No breaks in ground plane 🙂

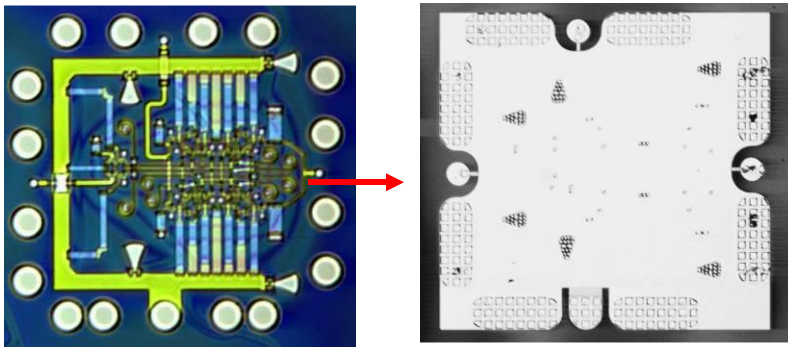
... no ground breaks at device placements 🙂

still have problem with package grounding 🙁

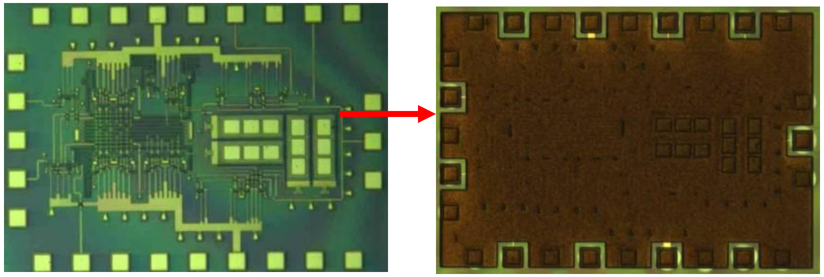
...need to flip-chip bond

thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines 🙁





InP 150 GHz master-slave latch



InP 8 GHz clock rate delta-sigma ADC

VLSI mm-wave interconnects with ground integrity

narrow line spacing → IC density ☺

no substrate radiation, no substrate losses ☺

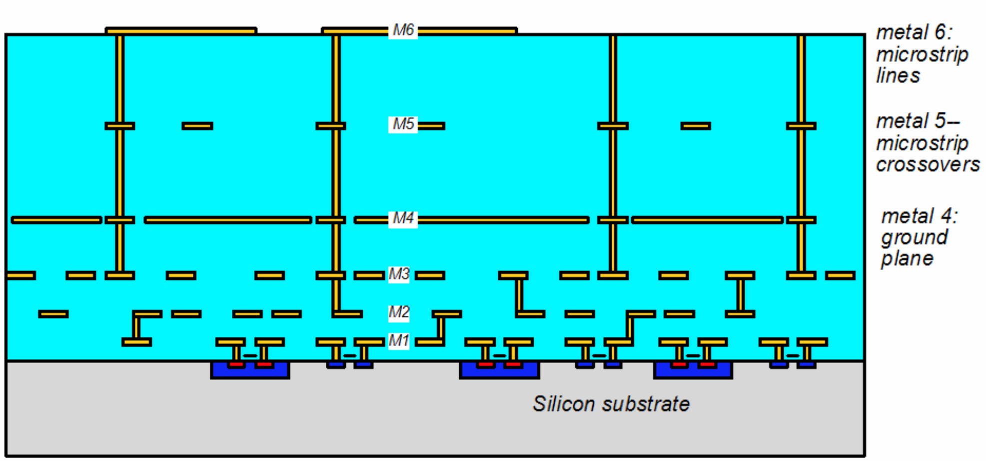
negligible breaks in ground plane ☺

negligible ground breaks @ device placements ☺

still have problem with package grounding ☹

...need to flip-chip bond

thin dielectrics → narrow lines ☹
→ high line losses
→ low current capability
→ no high-Z_o lines

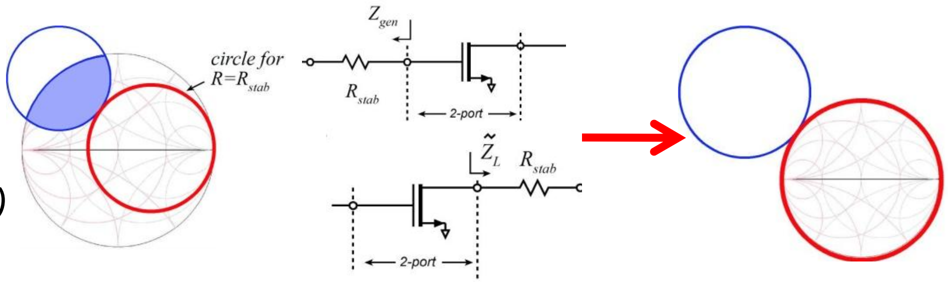


Also:
Ground plane at *intermediate level* permits critical signal paths to cross supply lines, or other interconnects without coupling.
(critical signal line is placed above ground, other lines and supplies are placed below ground)

RF-IC Design: Simple & Well-Known Procedures

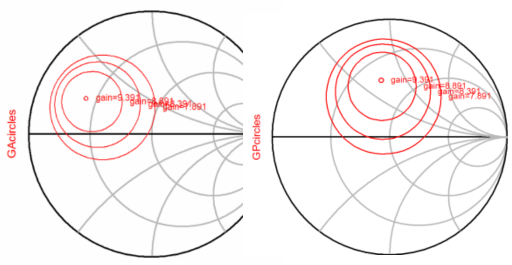
1: (over)stabilize at the design frequency
guided by stability circles

2: Tune input for F_{min} (LNAs) or output for P_{sat} (PAs)



3: Tune remaining port for maximum gain

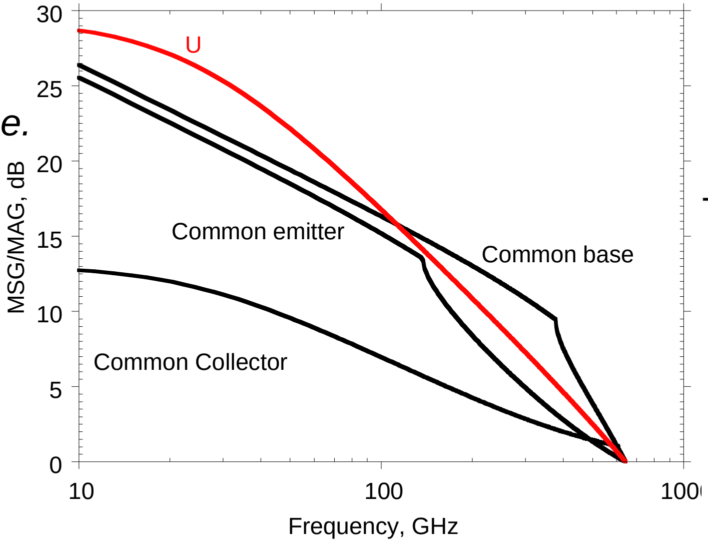
4: Add out-of-band stabilization.

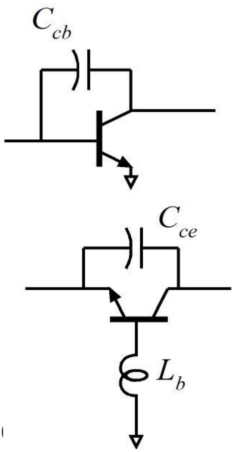


There are many ways to tune port impedances: microstrip lines, MIM capacitors, transformers
Choice guided by tuning losses. No particular preferences.

For BJT's, MAG/MSG usually highest for common-base.
→ preferred topology.

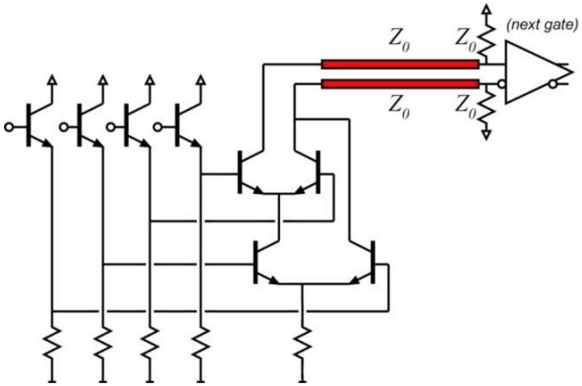
Common-base gain is however reduced by:
base (layout) inductance
emitter-collector layout capacitance.



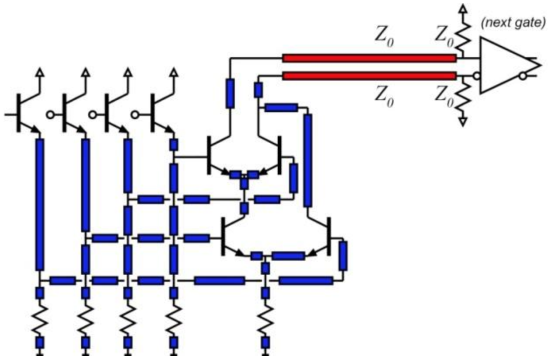


Modeling Interconnects: Digital & Mixed-Signal IC's

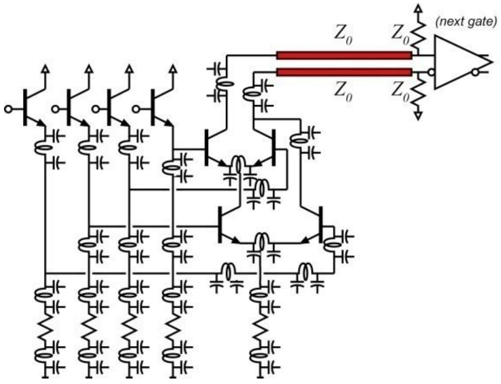
longer interconnects: 🟥
lines terminated in Zo → no reflections.



Shorter interconnects: 🟦
lines NOT terminated in Zo .
But they are *still* transmission-lines.
Ignore their effect at your peril !



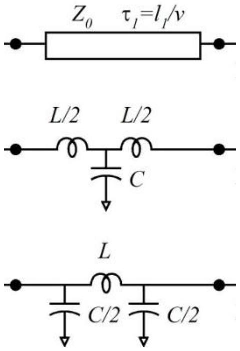
If length << wavelength,
or line delay<<risetime,
short interconnects behave
as lumped L and C.



$$L = Z_0 \tau \ ,$$

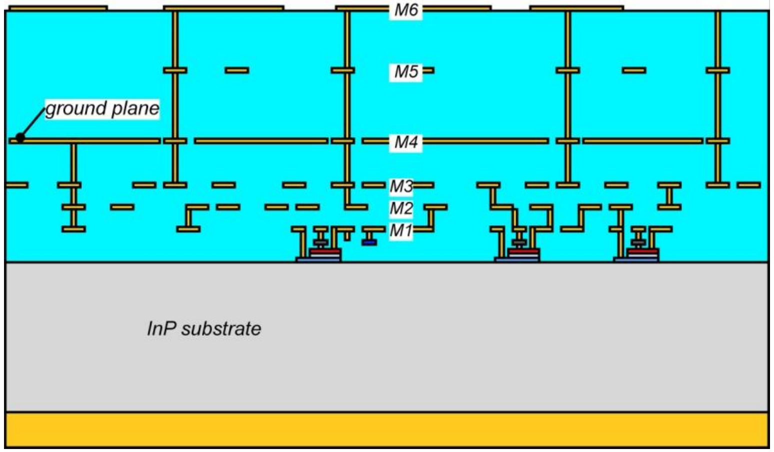
$$C = \tau / Z_0 ,$$

$$\tau = l / v$$



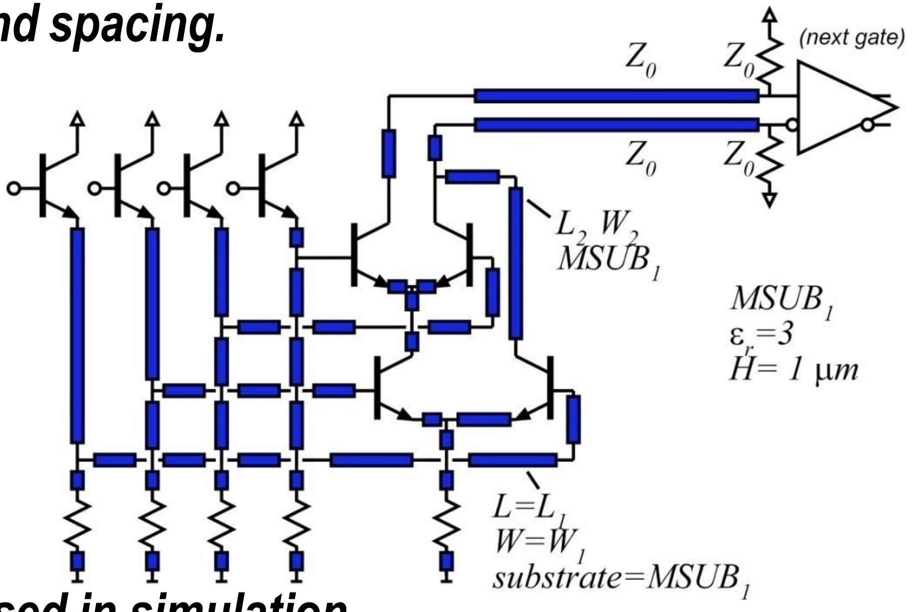
Design Flow: Digital & Mixed-Signal IC's

All interconnects: thin-film microstrip environment.
Continuous ground on one plane.



2.5-D simulations run on representative lines.
various widths, various planes
same reference (ground) plane.

Simulation data manually fit to CAD line model
effective substrate ε_r***, effective line-ground spacing.***

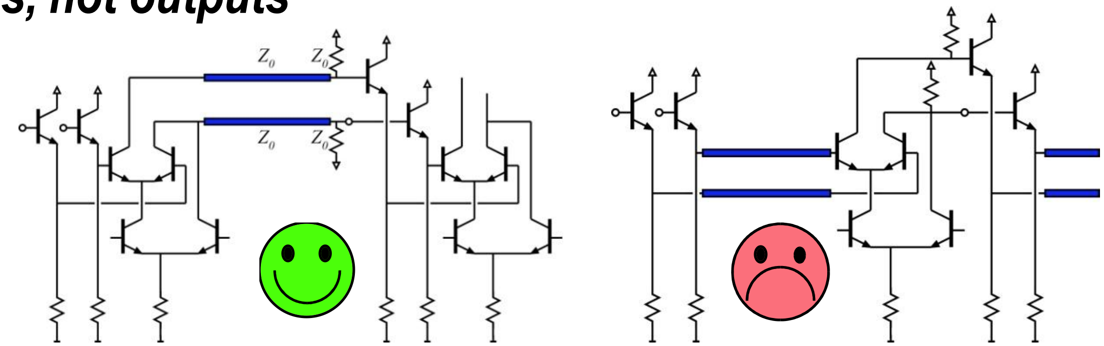


Width, length, substrate of each line
entered on CAD schematic.
rapid data entry, rapid simulation.

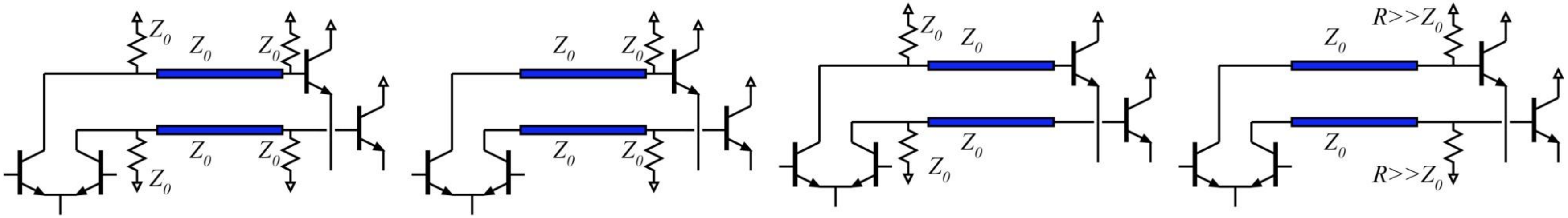
Resistors and capacitors:
2.5-D simulation→ RLC fit
RLC model ---or simulation S-parameters --used in simulation.

High Speed ECL Design

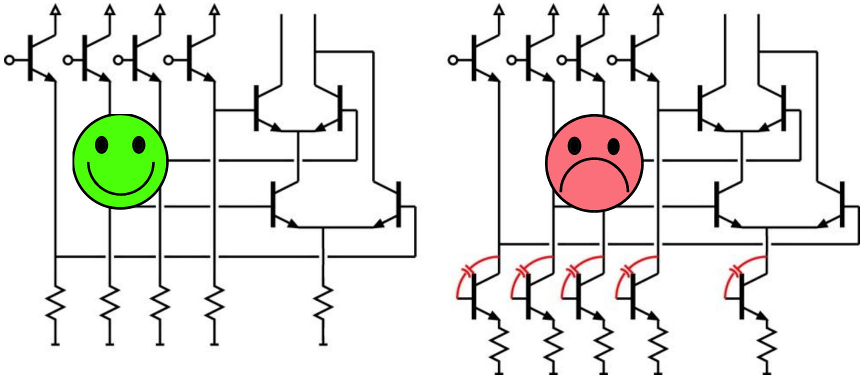
Followers associated with inputs, not outputs
Emitters never drive long wires.
(instability with capacitive load)



Double termination for least ringing, send or receive termination for moderate-length lines, high-Z loading saves power but kills speed.



Current mirror biasing is more compact.
Mirror capacitance→ ringing, instability.
Resistors provide follower damping.

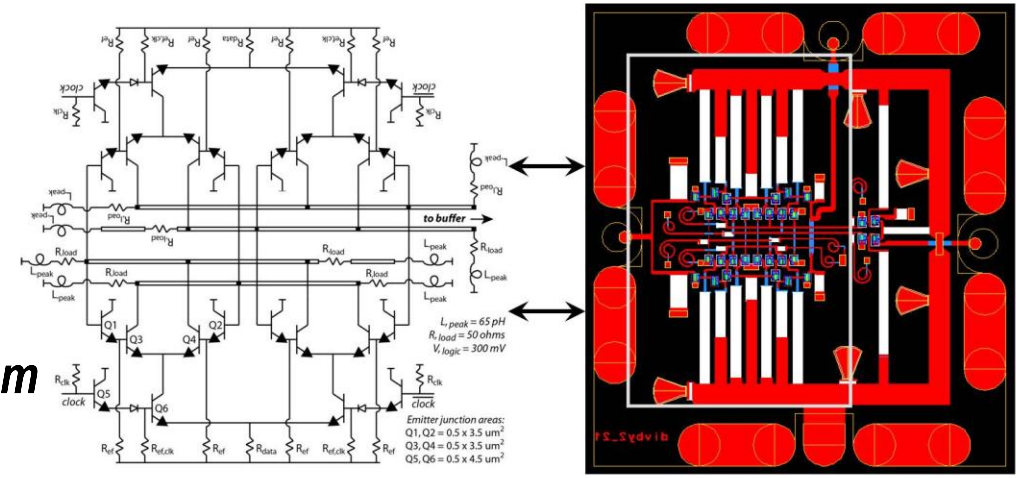


High Speed ECL Design

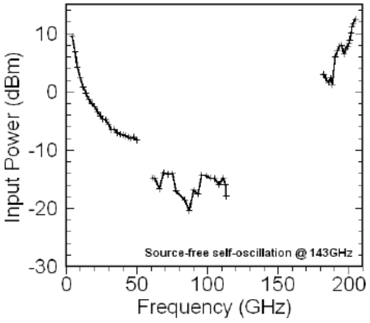
Layout: short signal paths at gate centers, bias sources surround core. Inverted thin film microstrip wiring.

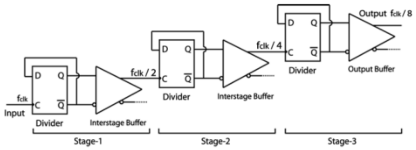
Key: transistors in on-state operate at Kirk limited-current.
→ minimizes C_{cb}/I_c delay.

Key: transistors designed for minimum ECL gate delay*, not peak (f_τ, f_{max}).
**hand expression, charge-control analysis*

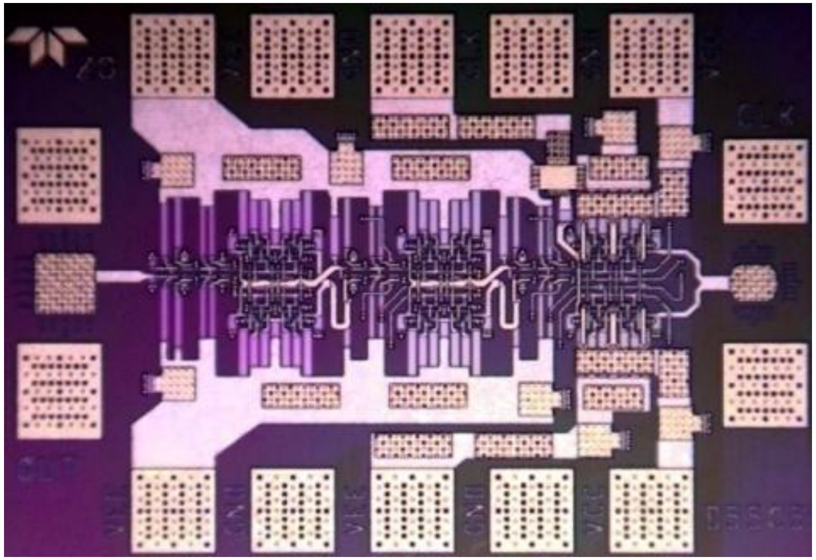


Example: 8:1 205 GHz static divider in 256 nm InP HBT.

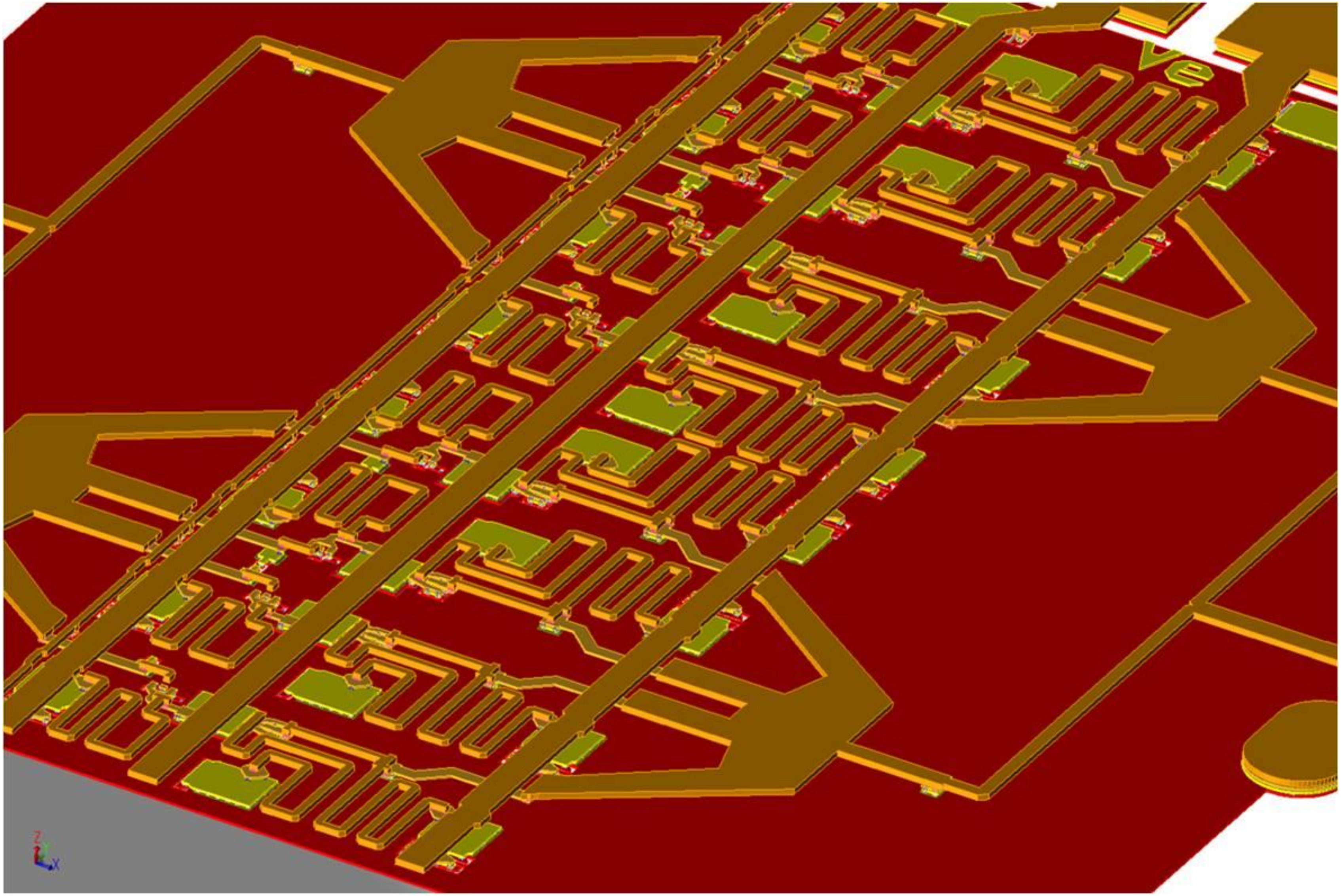




205 GHz divider, Griffith et al, IEEE CSIC, Oct. 2010

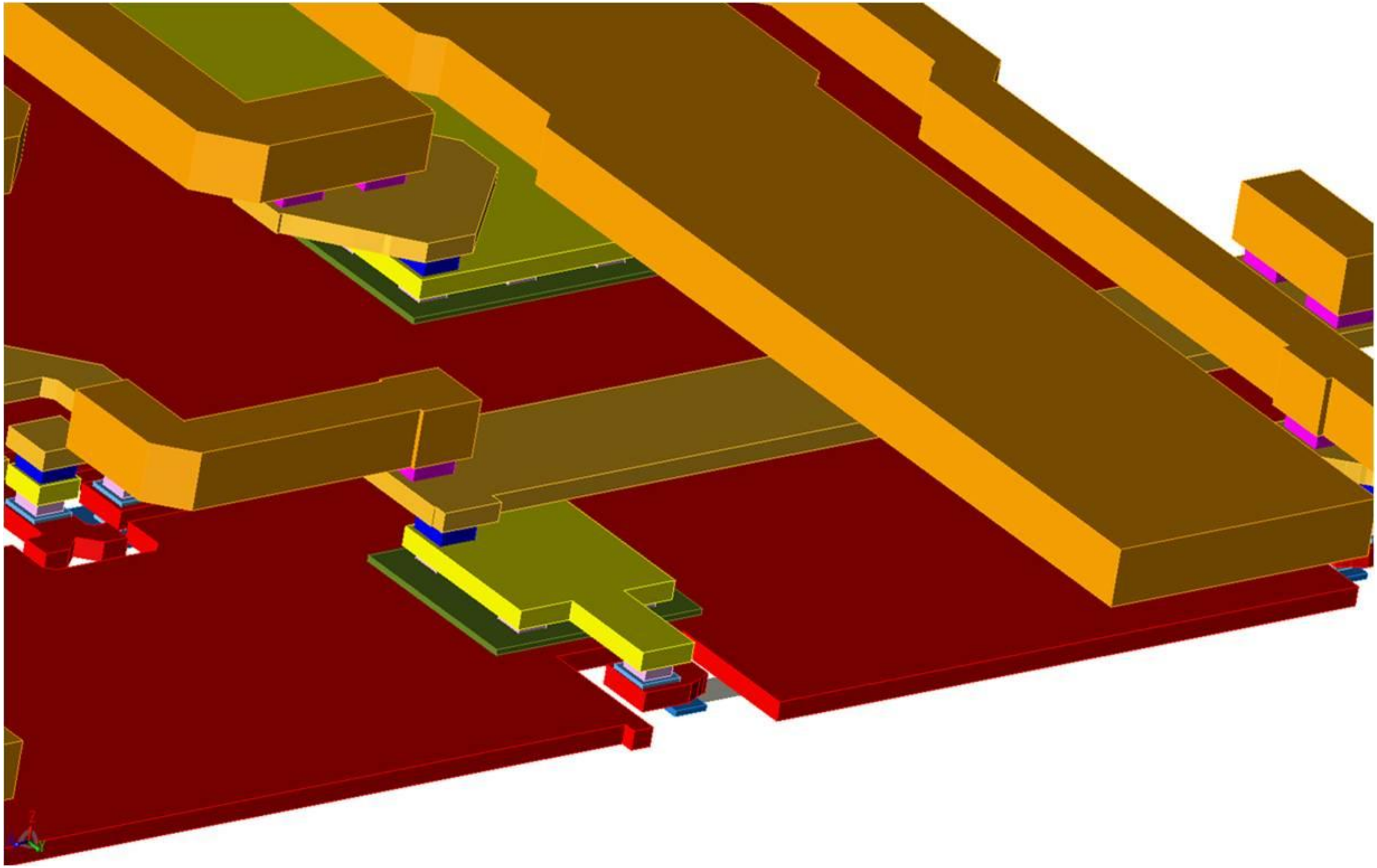


ICs in Thin-Film (Not Inverted) Microstrip



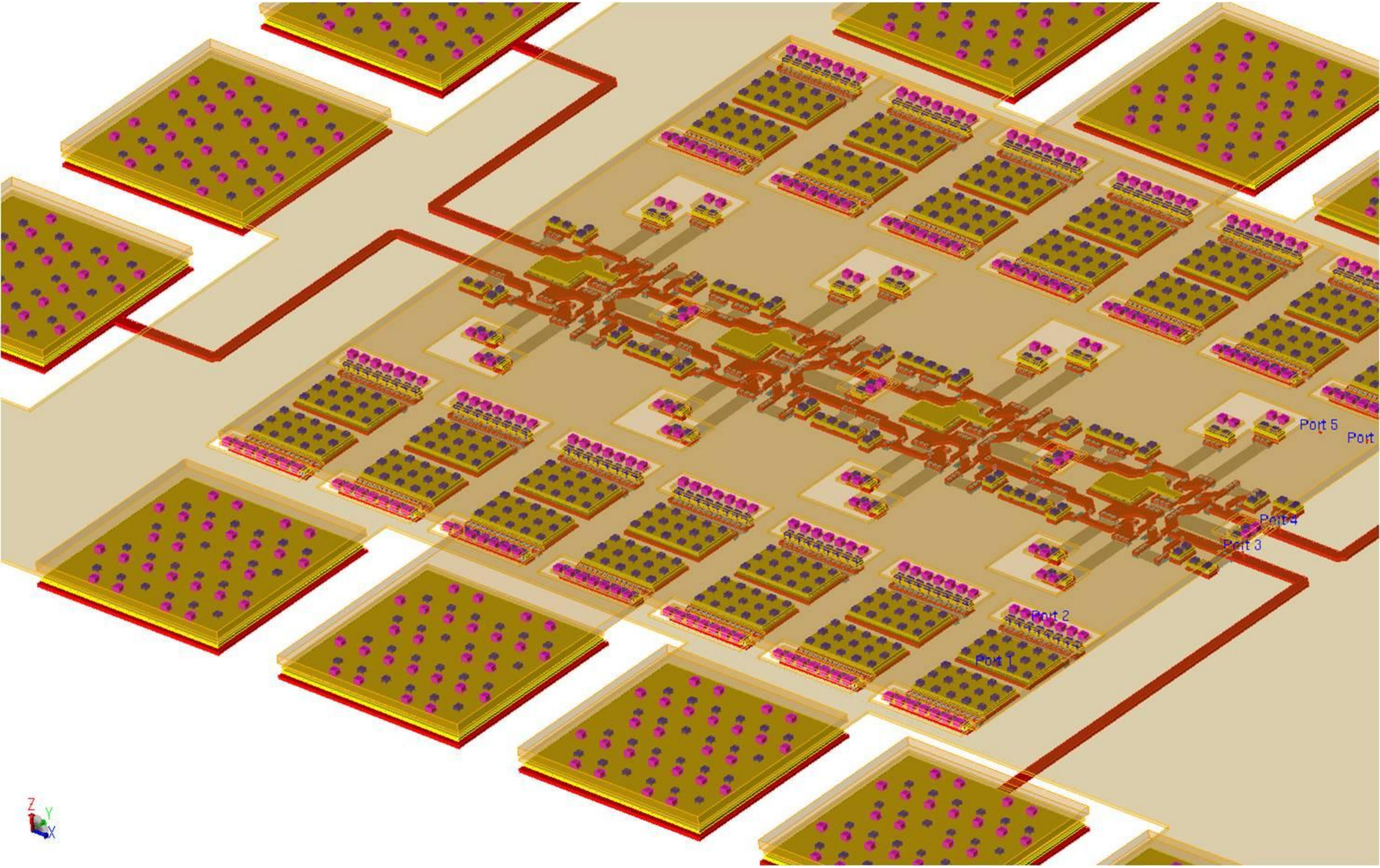
Note breaks in ground plane at transistors, resistors, capacitors

ICs in Thin-Film (Not Inverted) Microstrip



Note breaks in ground plane at transistors, resistors, capacitors

ICs in Thin-Film Inverted Microstrip



100 GHz differential TASTIS Amp.   512nm InP HBT

High Frequency Bipolar IC Design

Digital, mixed-signal, RF-IC (tuned) IC designs----at very high frequencies

Even at 670 GHz, design procedures differ little from that at lower frequencies:

Classic IC design extends readily to the far-infrared.

<u>Key considerations: Tuned ("RF") ICs</u>
Rigorous E&M modeling of all interconnects & passive elements
Continuous ground plane → required for predicable interconnect models.
Higher frequencies→ close conductor planes→ higher loss, lower current

<u>Key considerations: digital & mixed-signal :</u>
Transmission-line modeling of <u>all</u> interconnects
Continuous ground plane → required for predicable interconnect models.
Unterminated lines within blocks; terminated lines interconnecting blocks.
Analog & digital blocks design to naturally interface to 50 or 75Ω.

Design Examples, IC Results

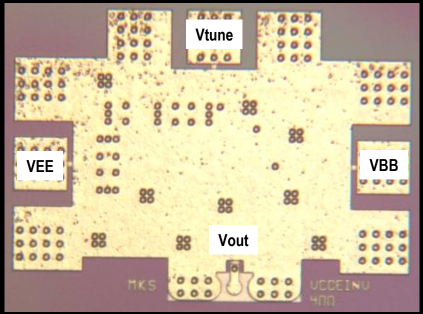
InP HBT Integrated Circuits: 600 GHz & Beyond

TELEDYNE SCIENTIFIC COMPANY
A Teledyne Technologies Company

UCSB

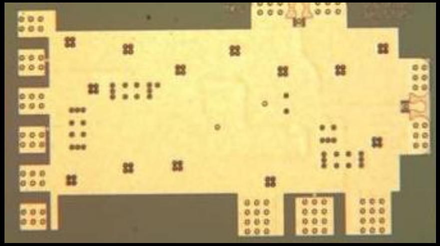
614 GHz fundamental VCO

M. Seo, TSC / UCSB



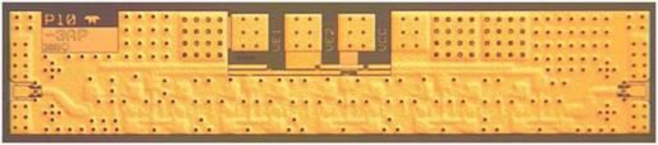
340 GHz dynamic frequency divider

M. Seo, UCSB/TSC
IMS 2010



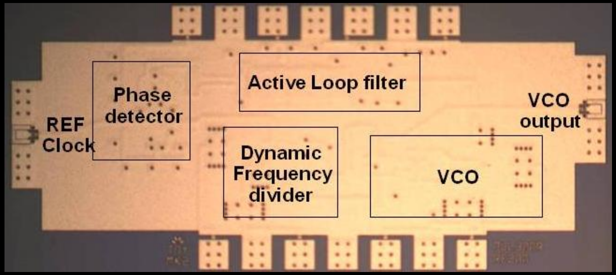
565 GHz, 34 dB, 0.4 mW output power amplifier

J. Hacker, TSC



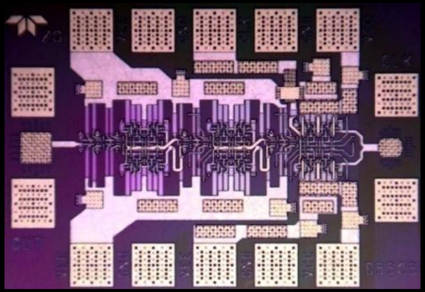
300 GHz fundamental PLL

M. Seo, TSC
IMS 2011



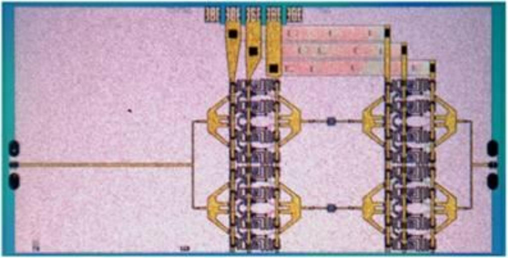
204 GHz static frequency divider (ECL master-slave latch)

Z. Griffith, TSC
CSIC 2010

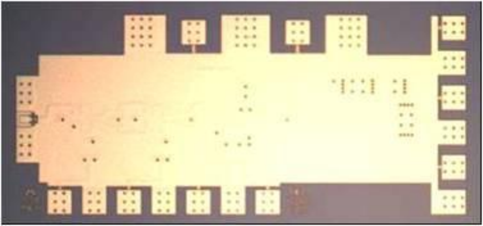


220 GHz 90 mW power amplifier

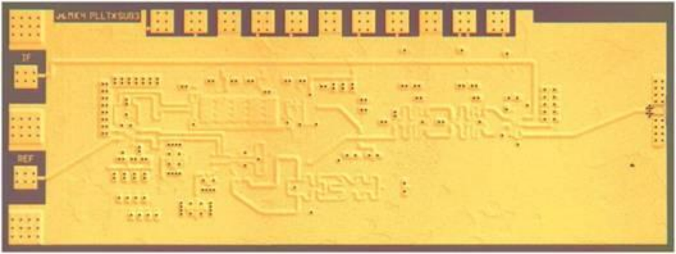
T. Reed, UCSB



Integrated 300/350GHz Receivers:
LNA/Mixer/VCO
M. Seo TSC

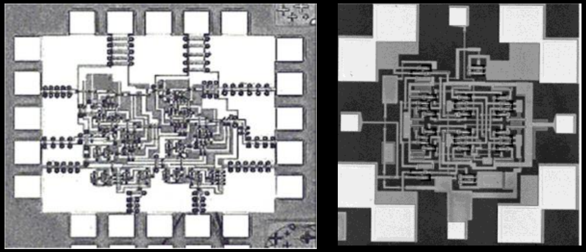


600 GHz Integrated Transmitter
PLL + Mixer
M. Seo TSC

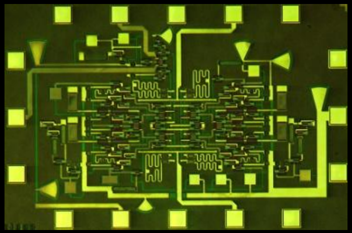


Digital Logic: 30 GHz to 204 GHz in 12 Years

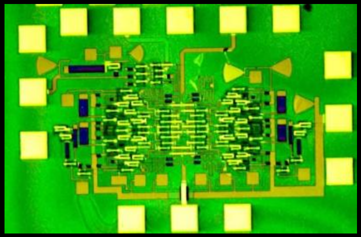
1998: 30 GHz→ 48 GHz



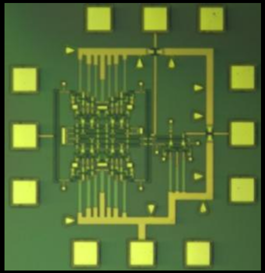
2000: 66 GHz



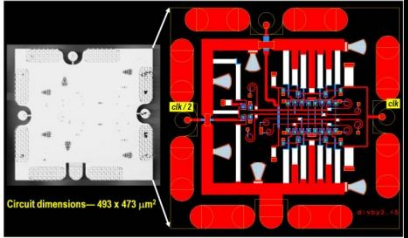
2001: 75GHz



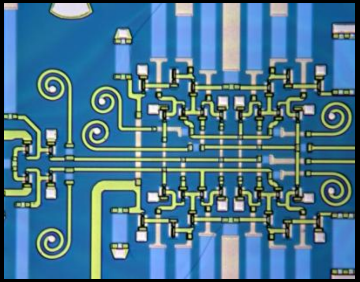
2002: 87GHz



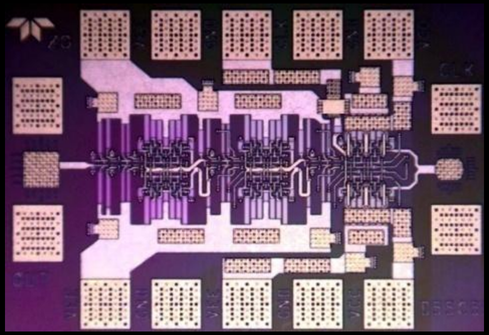
2004: 118 GHz



2004: 142 GHz, 150 GHz

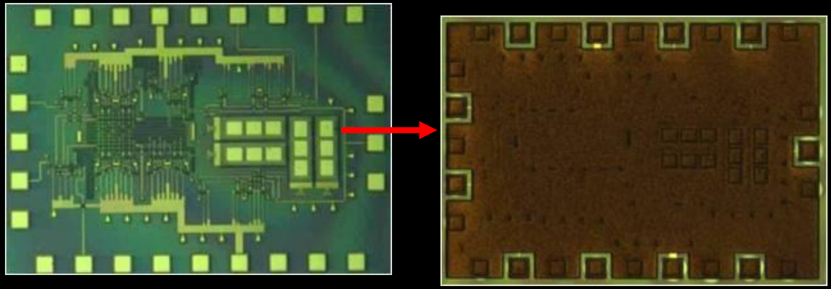


2010: 204 GHz (with Teledyne)

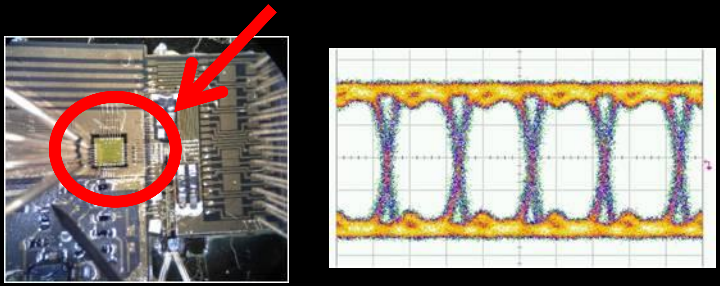


Other InP HBT ICs in Inverted Microstrip

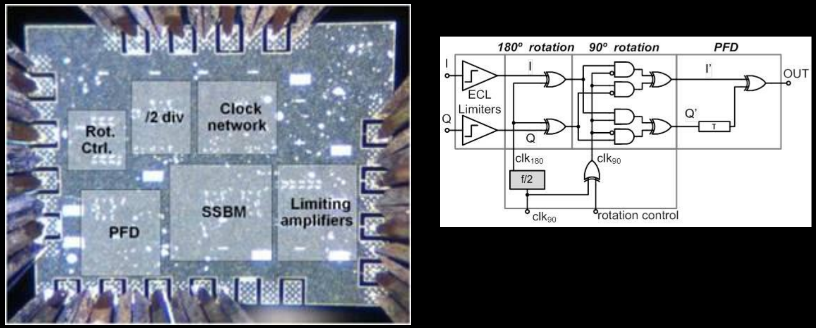
Teledyne InP HBT
256 nm, 512 nm



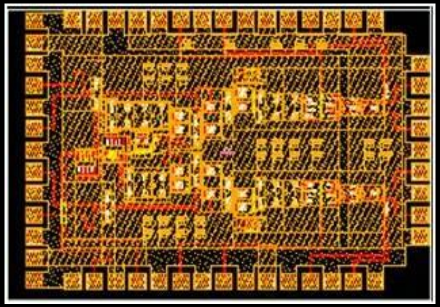
InP 8 GHz clock rate delta-sigma ADC
(Krishnan, IMS 2003)



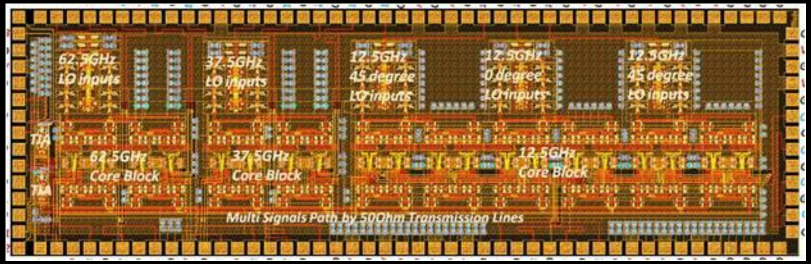
40 Gb/s coherent optically-phase-locked
BSPK optical receiver (Bloch, Park, ECOC 2012)



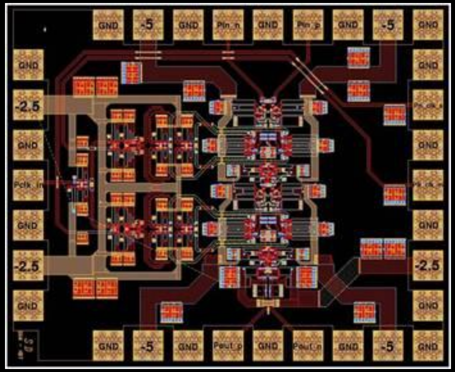
30 GHz digital SSB mixer / PFD for optical PLL
(Bloch, IMS 2012)



40 Gb/s coherent optically-phase-locked
QPSK optical receiver (E. Bloch, in fab)



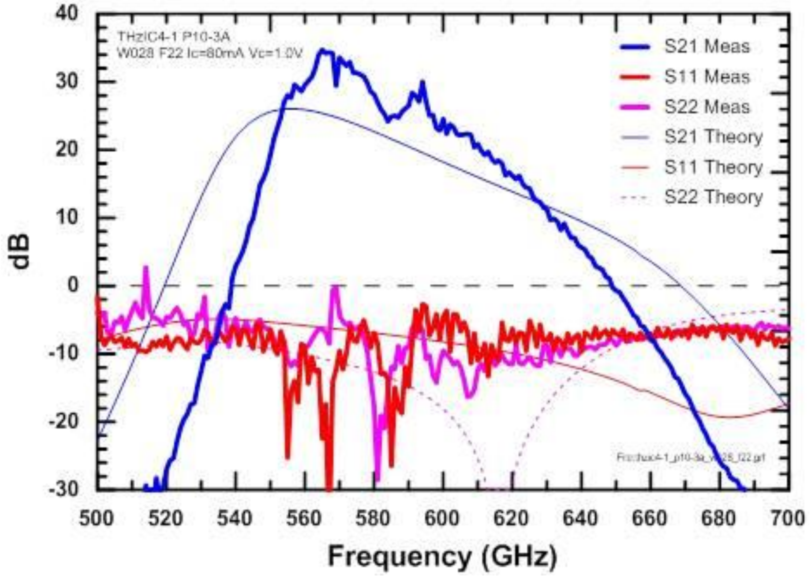
10 Gb/s x 6-channel (+/- 12.5, +/- 37.5, +/- 62.5 GHz)
WDM receiver IC for coherent optical links
(H. Park, in fab)



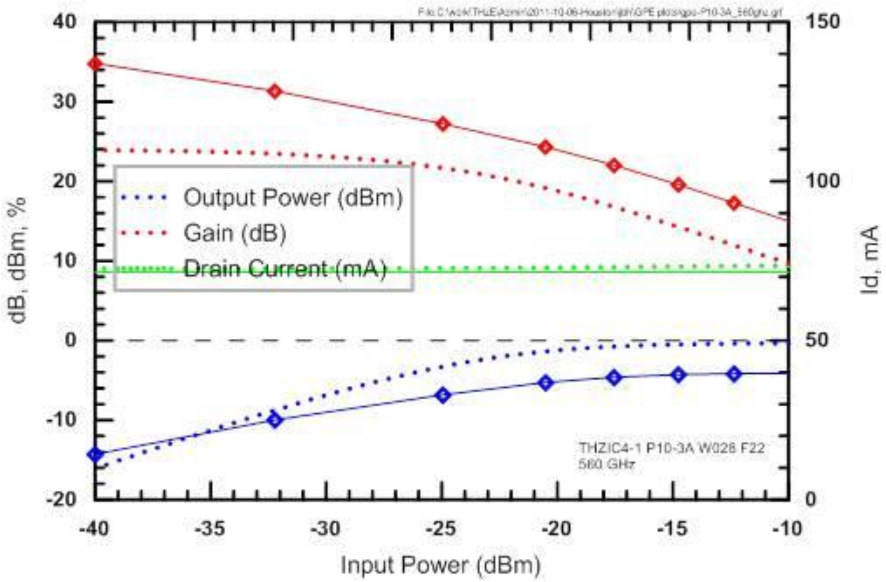
50 GS/s Track/hold and sample/hold amplifiers
Daneshgar, IEEE CSICS Oct. 2012

Teledyne: 560 GHz Common-Base Amplifier IC

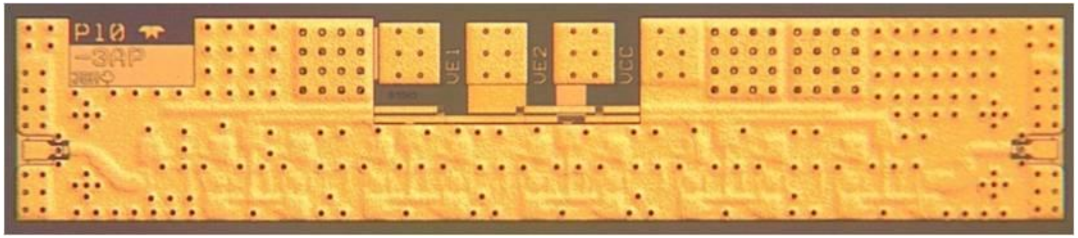
S-parameters



Output Power



- 10-Stage Common-base using inverted CPW-G architecture
- 34 dB at 565 GHz
- Psat -3.9 dBm at 560 GHz

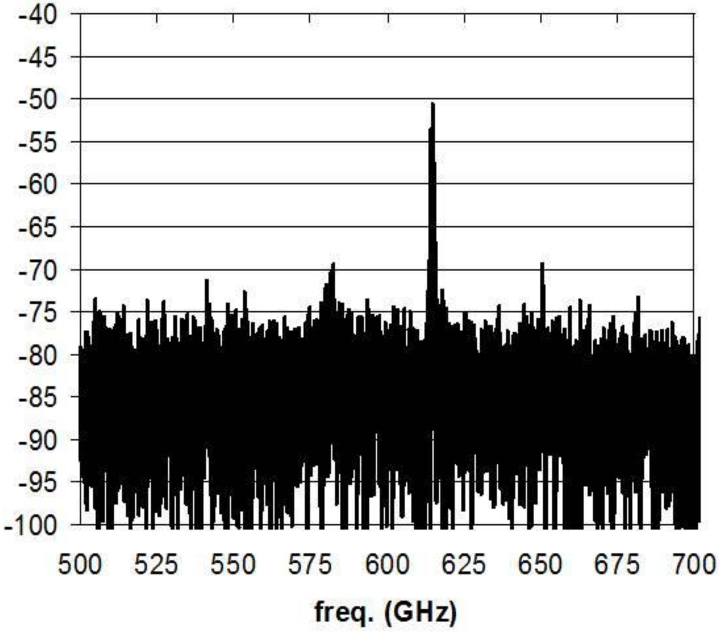


1200x230 μm^2

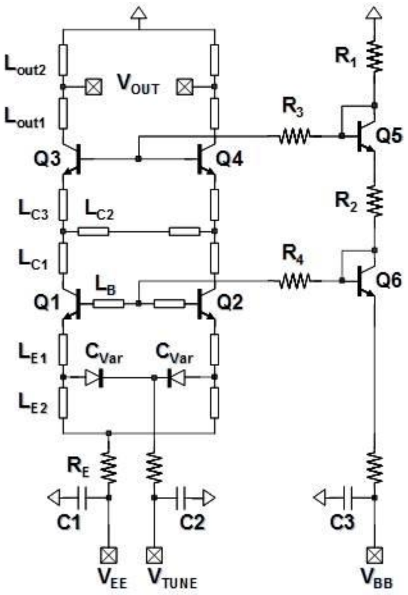
J. Hacker *et al*, Teledyne Scientific

130nm 600 GHz Fundamental Oscillators

Output spectrum of 614GHz oscillator fabricated with 130nm HBTs



Oscillator Schematic



Oscillator Output Power

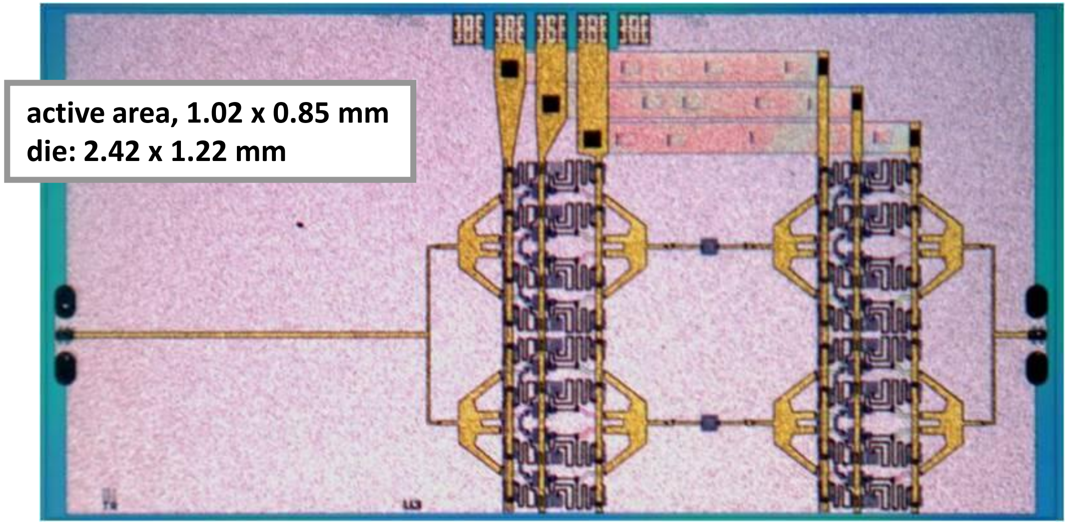
Measured Freq.	Measure P_{out} (dBm)
540GHz	-10.1
560GHz	-14.1
570GHz	-13.8
598GHz	-17.8
610 GHz	-19.2

Output spectrum measurements performed on-wafer using UVA Wafer probes and Virginia Diodes VNA Extender Heads

Single-ended power measurements performed with on-wafer probe coupled to Erickson calorimeter power meter. P_{out} corrected based on measured probe loss at osc. frequency.

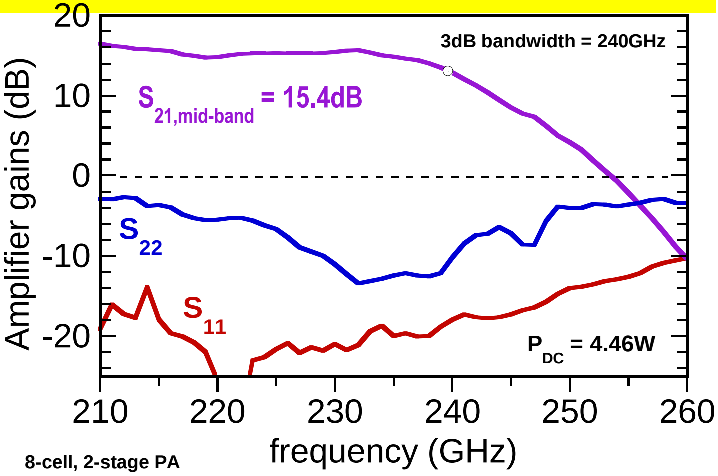
M. Seo *et al*, Teledyne Scientific

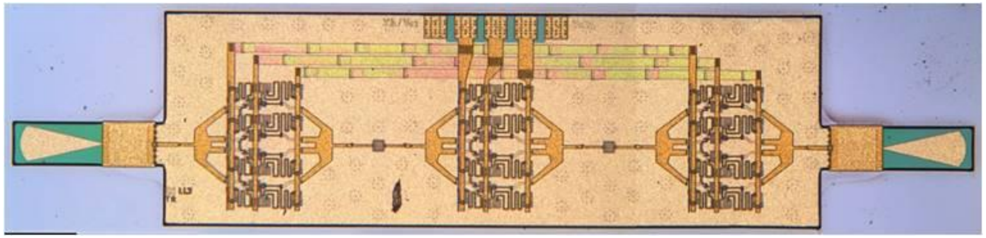
90 mW, 220 GHz Power Amplifier

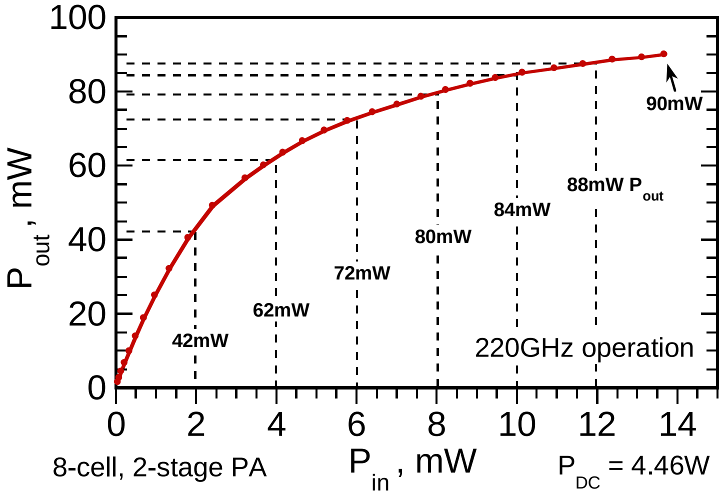


active area, 1.02 x 0.85 mm
die: 2.42 x 1.22 mm

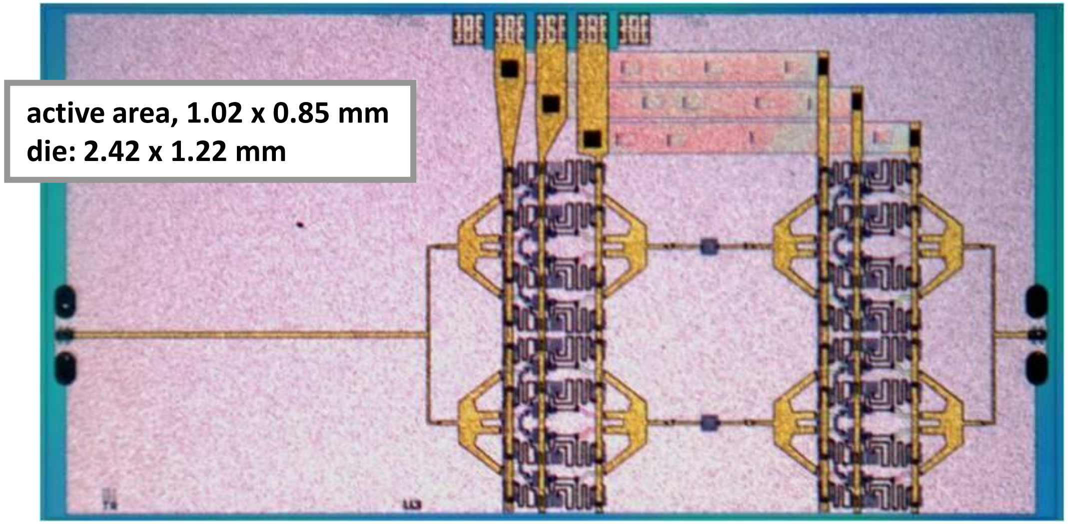
Reed (UCSB) and Griffith (Teledyne): CSIC 2012
Teledyne 250 nm InP HBT







90 mW, 220 GHz Power Amplifier



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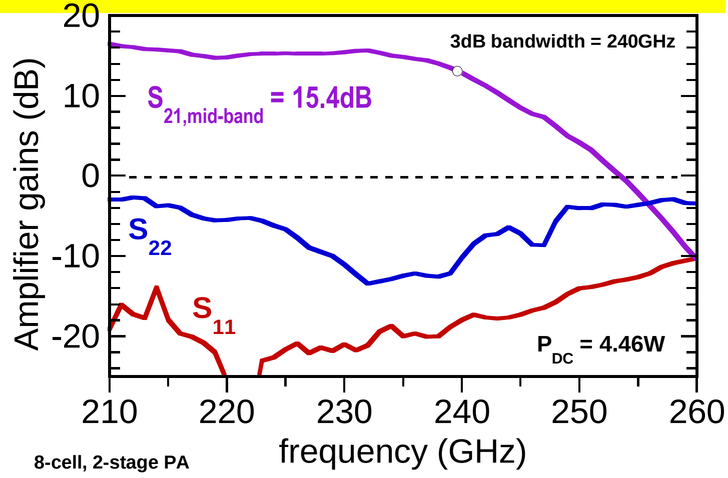
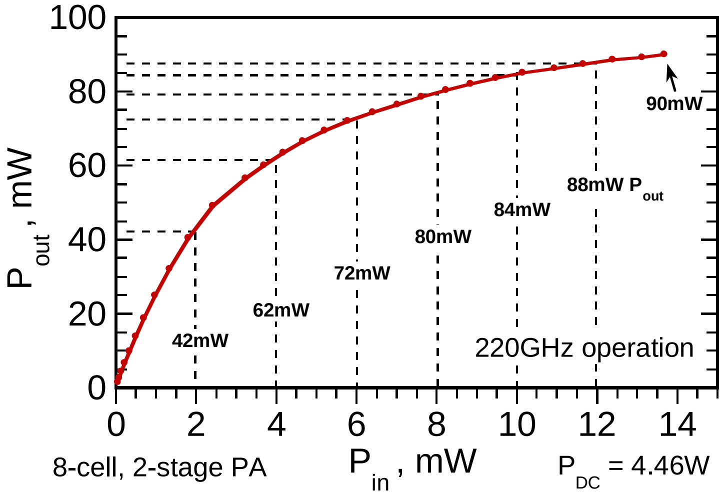
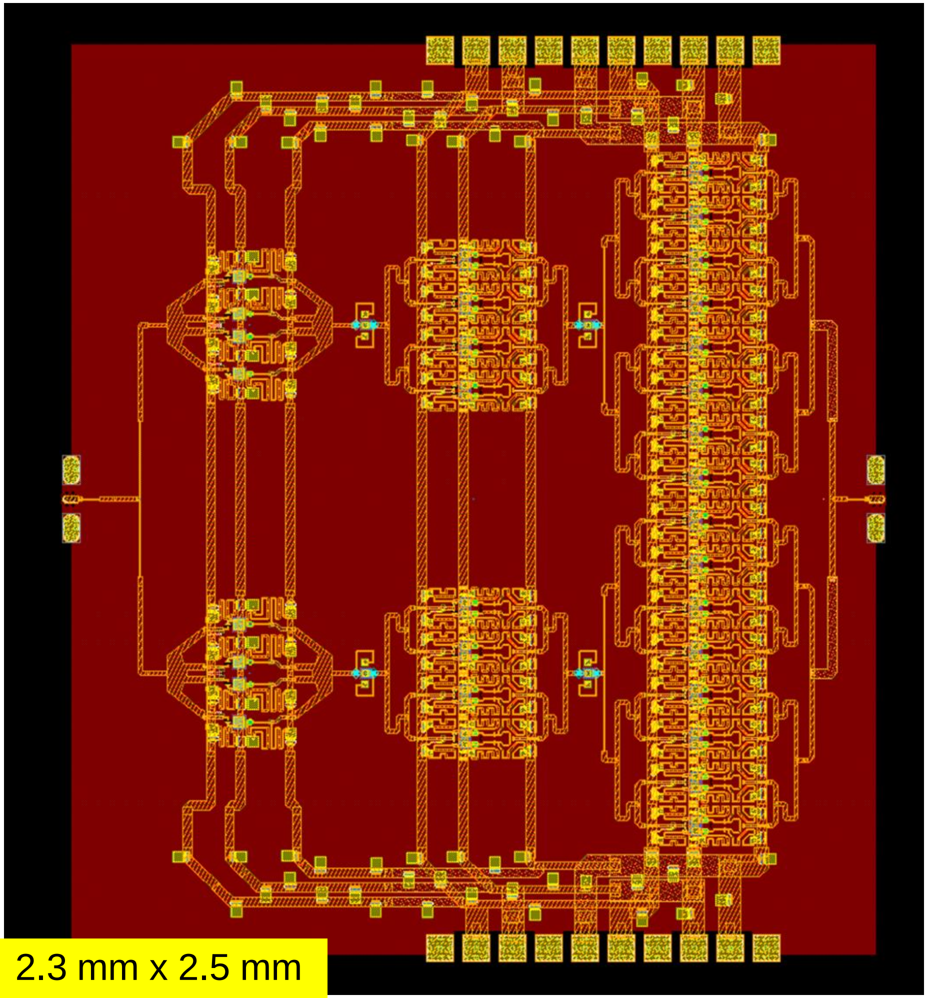




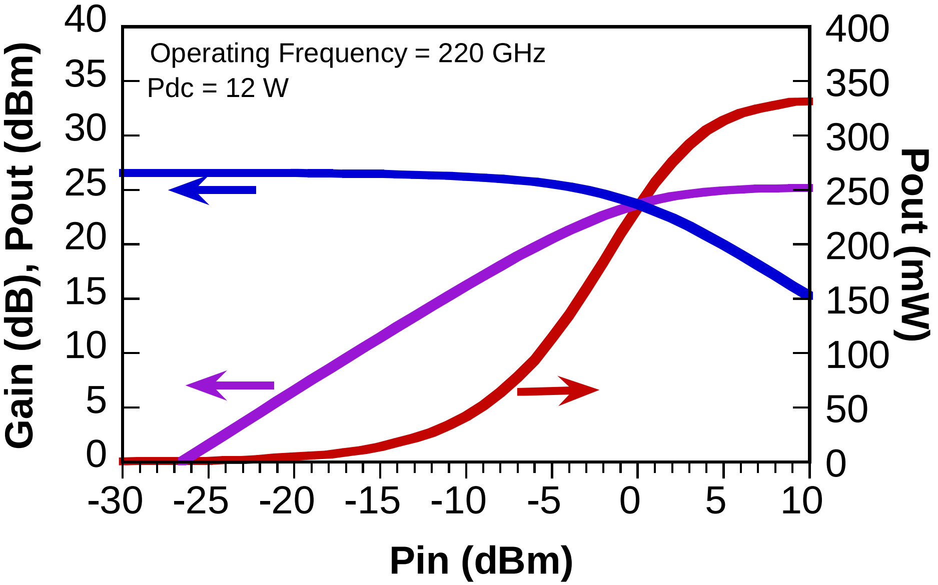
RF output power densities up to 0.5 W/mm @ 220 GHz.

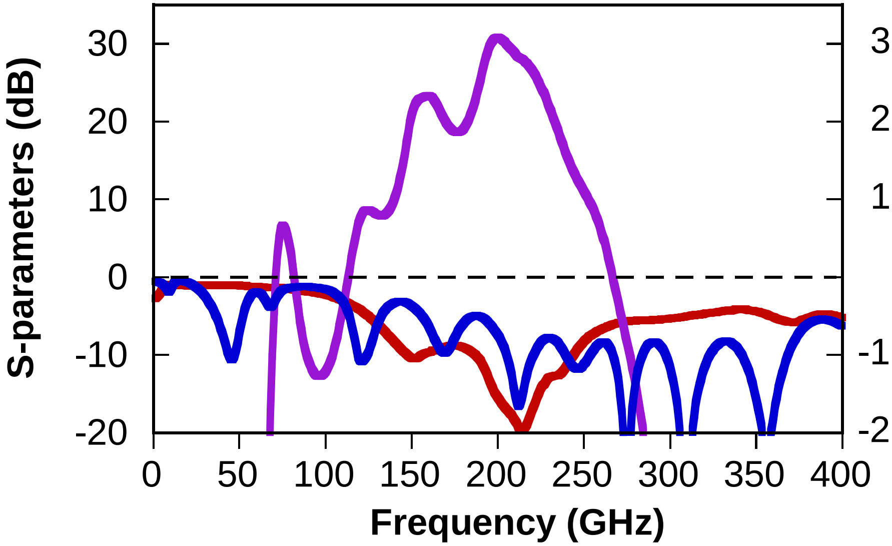
→ InP HBT is a competitive mm-wave / sub-mm-wave power technology.

220 GHz 330mW Power Amplifier Design



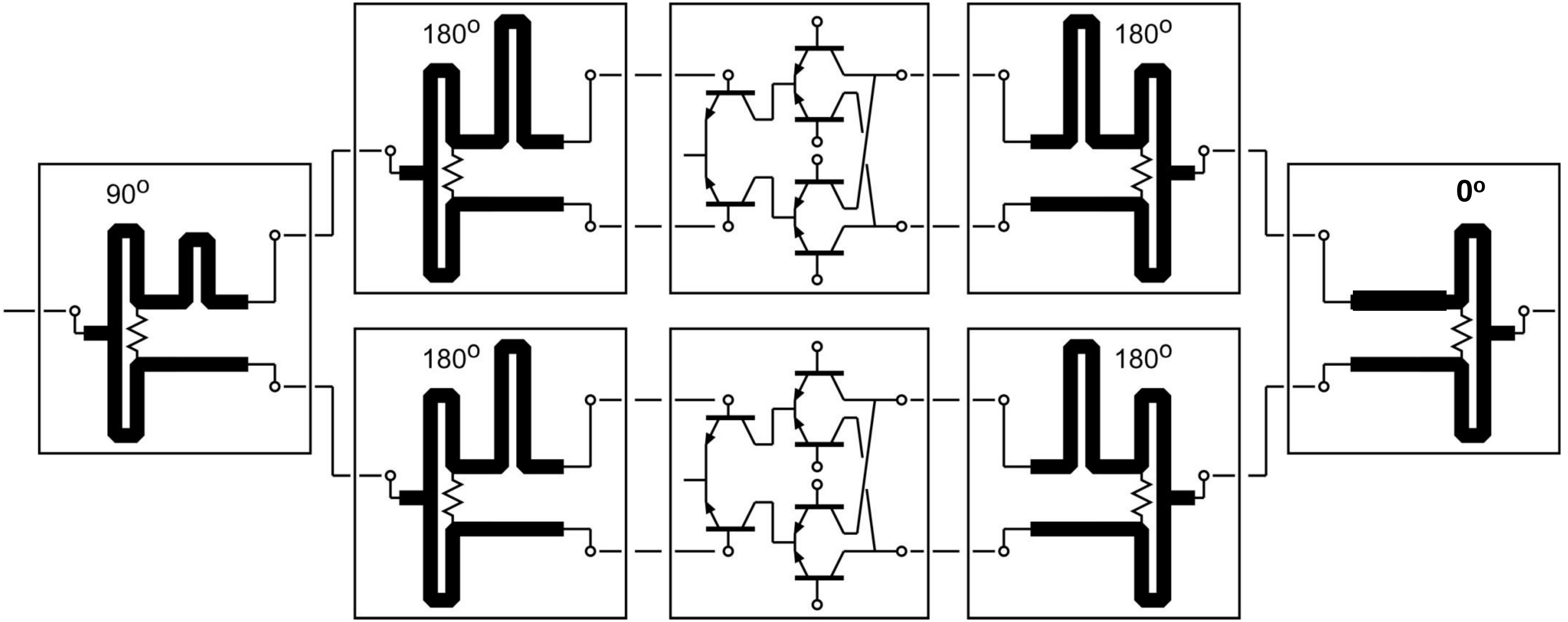
2.3 mm x 2.5 mm



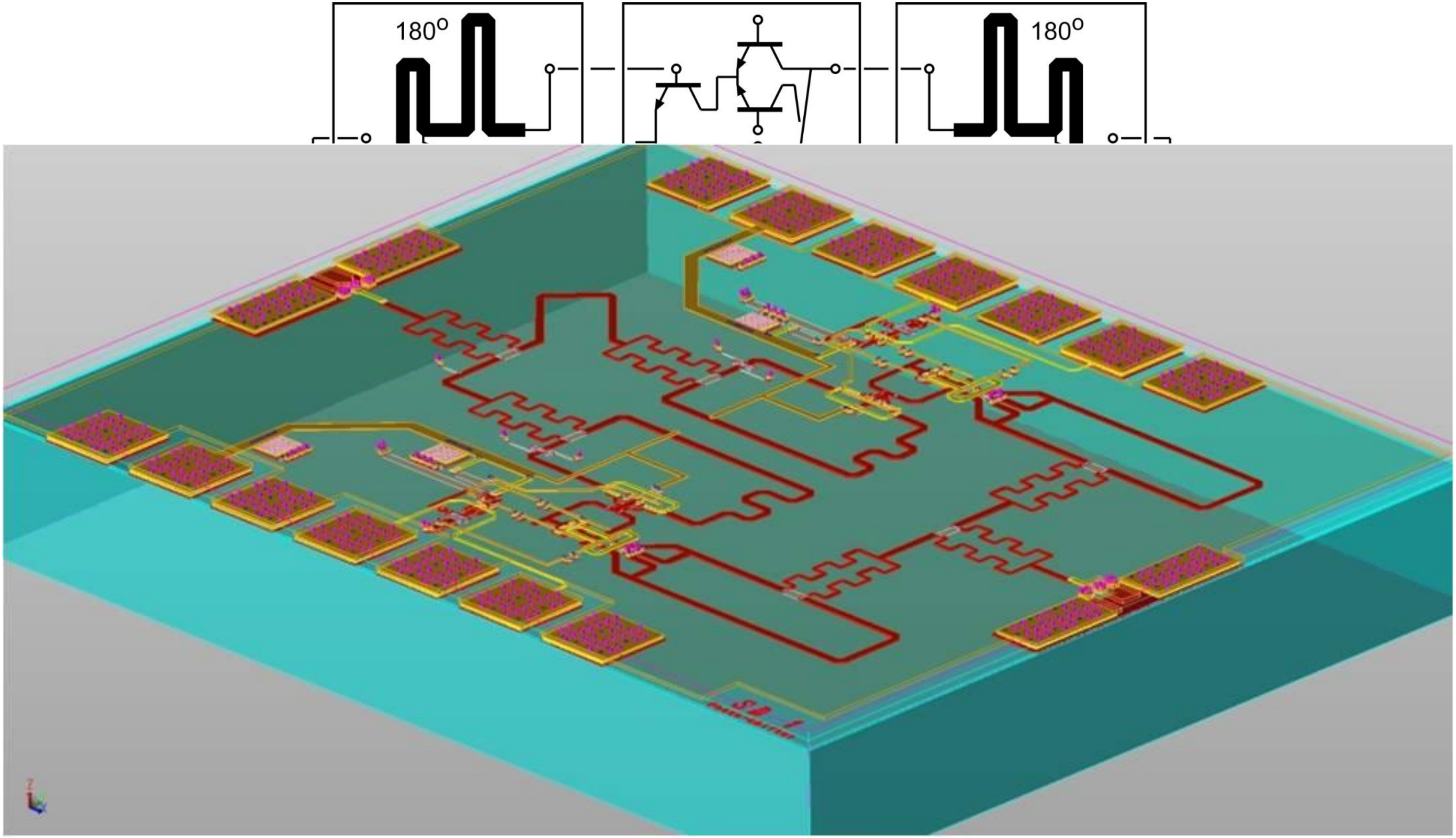


T. Reed, UCSB
Z. Griffith, Teledyne
Teledyne 250 nm InP HBT

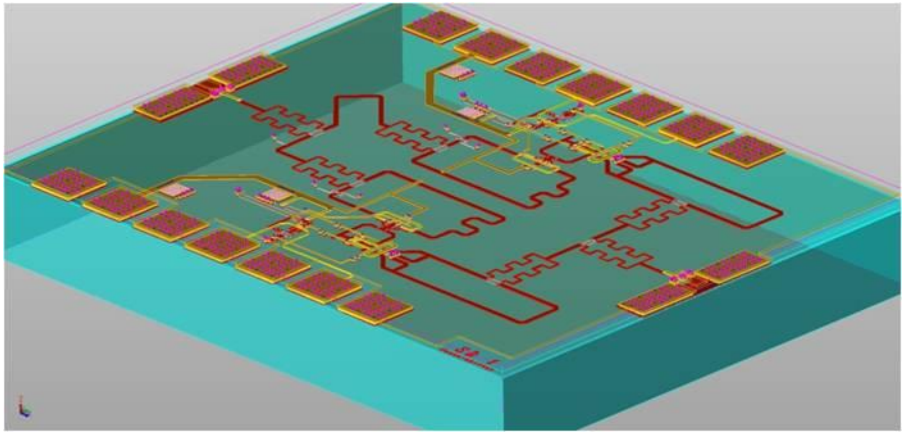
220 GHz Vector Modulator / Phase Shifter Design

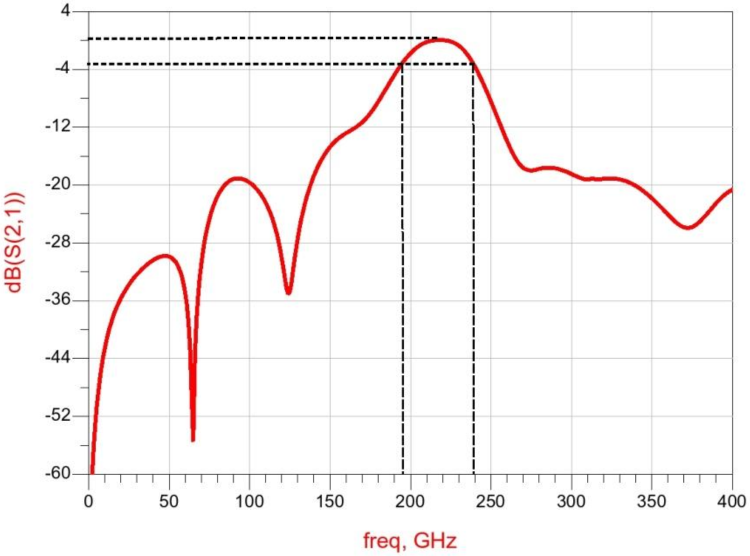


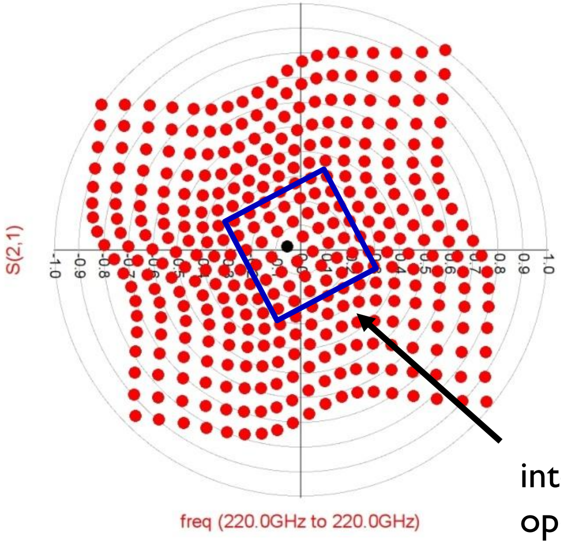
220 GHz Vector Modulator / Phase Shifter Design



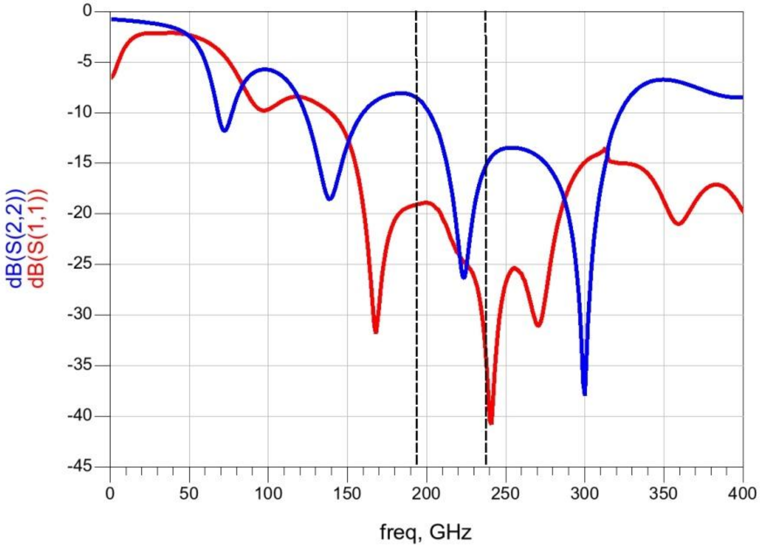
220 GHz Vector Modulator / Phase Shifter Design







intended
operating range

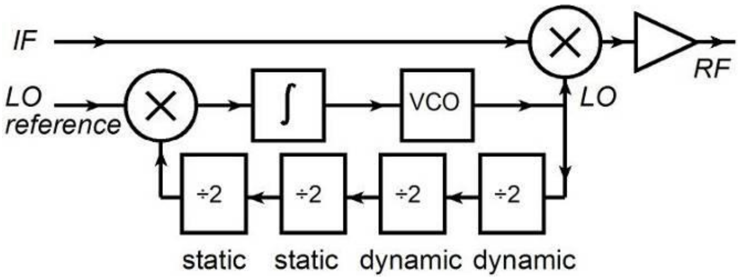


Technology: 256nm InP HBT
9/2012 tapeout; ICs expected 12/2012

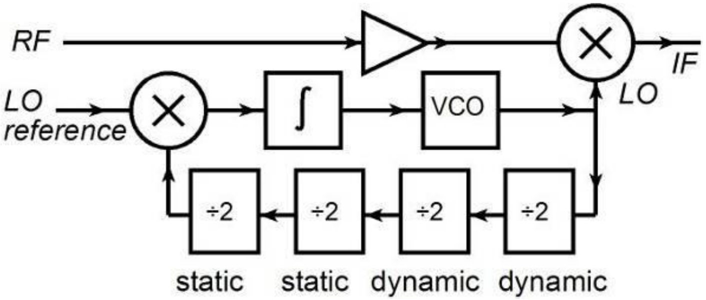
Closing

Where Next ? → 2 THz Transistors, 1 THz Radios.

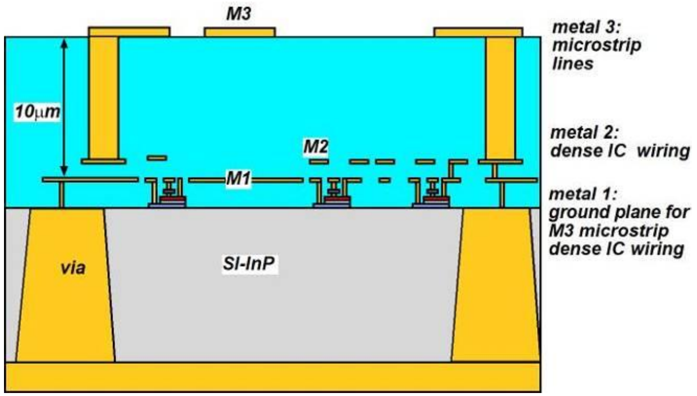
transmitter



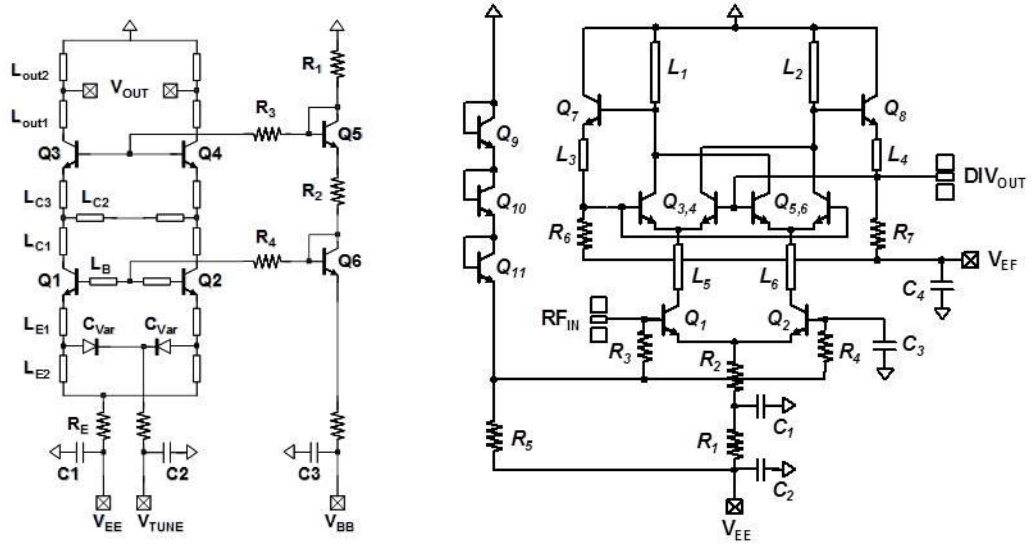
receiver



interconnects

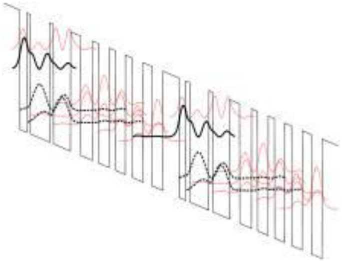


circuits

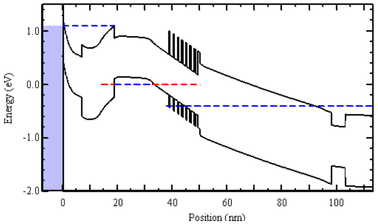


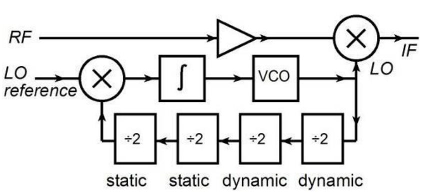
THz and Far-Infrared Electronics

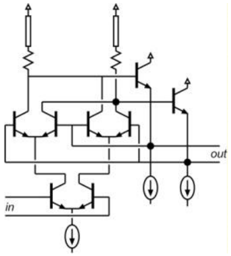
IR today→ lasers & bolometers → generate & detect

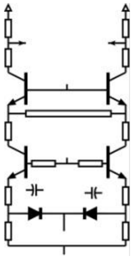


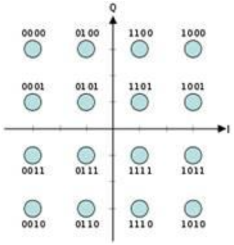
Far-infrared ICs: classic device physics, classic circuit design











Power, power-added efficiency, noise figure are all very important

fundamental-mode operation, not harmonic generation

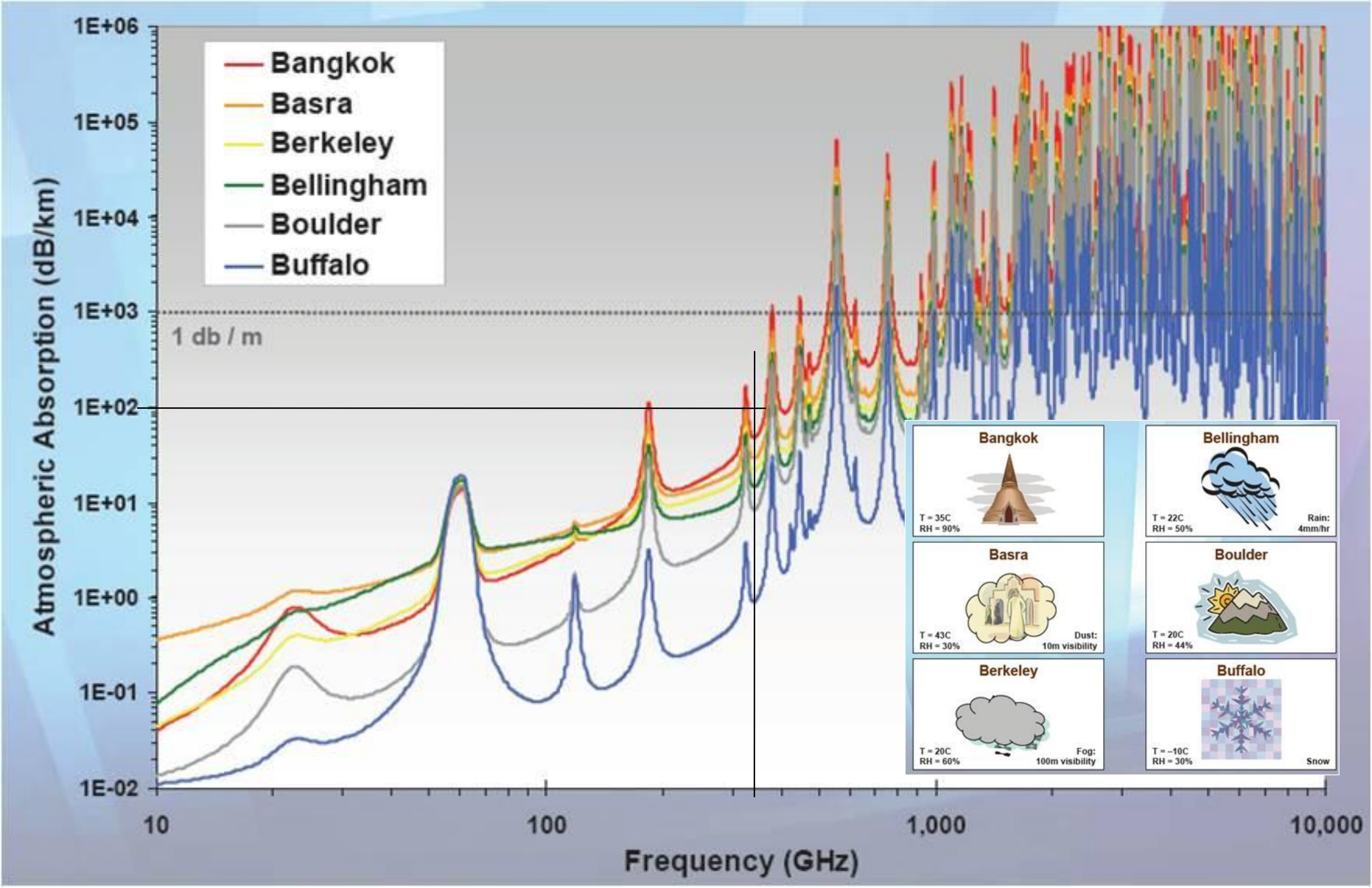
The transistors will scale to at least 2 THz bandwidths

Even 1-3 THz ICs will be feasible

(backup slides follow)

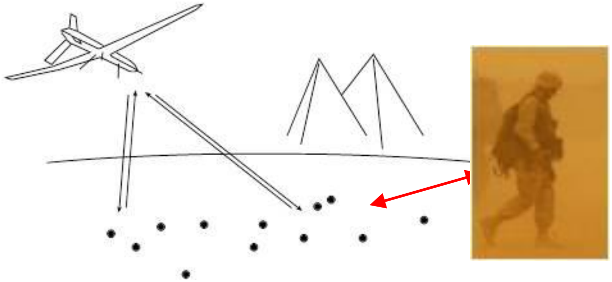
At High Frequencies The Atmosphere Is Opaque

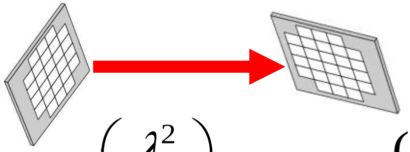
Mark Rosker
IEEE IMS 2007



Why THz Transistors ? Why THz ICs ?

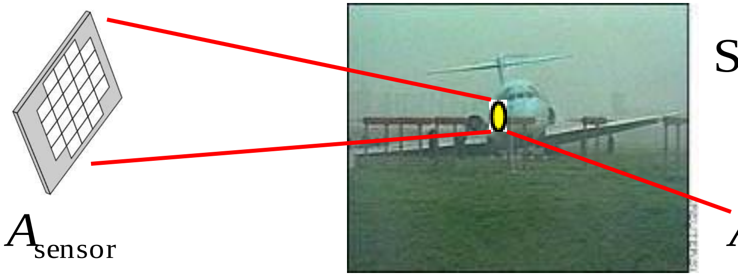
Communications





$$\text{bit rate} \propto \frac{P_{\text{transmit}}}{T_{\text{ambient}} + T_{\text{receiver}}} \left(\frac{\lambda^2}{R^2} \right) e^{-\alpha R} \cdot \frac{(\#\,\text{elements})^2}{(\text{steerable angle})^4}$$

Imaging / RADAR

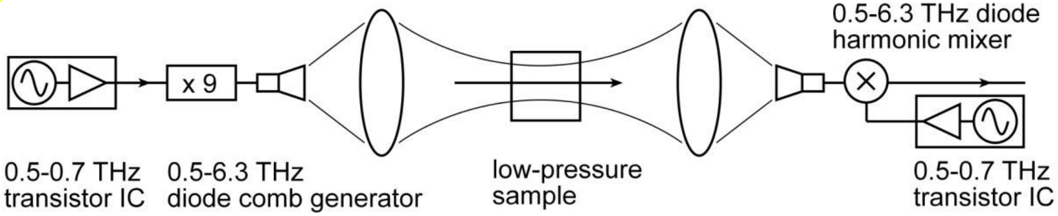


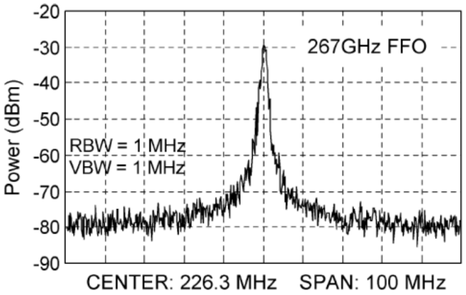
A_{sensor}

$$\text{SNR} \propto \frac{P_{\text{transmit}}}{T_{\text{ambient}} + T_{\text{receiver}}} \left(\frac{A_{\text{sensor}}}{R^2} \right) e^{-\alpha R} \cdot \frac{\text{Acquisition time}}{\#\,\text{pixels}}$$

$$A_{\text{pixel}} \propto \lambda^2 R^2 / A_{\text{sensor}}$$

Spectroscopy





$$P_{\text{received}} \cong P_{\text{transmitted}}$$

ICs give very compact source, very low spectral linewidth