A 220GHz InP HBT Solid-State Power Amplifier MMIC with 90mW P_{OUT} at 8.2dB Compressed Gain

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***Abstract* — A 220 GHz Solid State Power Amplifer MMIC is presented simultaneously demonstrating 90mW output power P_{out} and 8.2dB compressed gain. This 2-Stage, 8-Cell amplifier has 14.8dB S_{21} gain at 220GHz, with small signal bandwidth from at least 190 to 240GHz. P_{DC} is 4.46W. Amplifier cells were fabricated from a 250nm InP HBT technology, jointly with a substrate-shielded, thin-film microstrip wiring environment using BCB. The 90mW P_{out} is achieved by combining eight amplifier cascode cells. The use of two gain stages relaxes the RF source power demands, where only 13.6mW P_{in} is needed to achieve 90mW P_{out}. Over 10GHz bandwidth, at least 75mW P_{out} is observed from 210 to 220GHz.**

***Index Terms* — Millimeter wave integrated circuits, MMICs, Power amplifier, Solid State Power Amplifier (SSPA).**

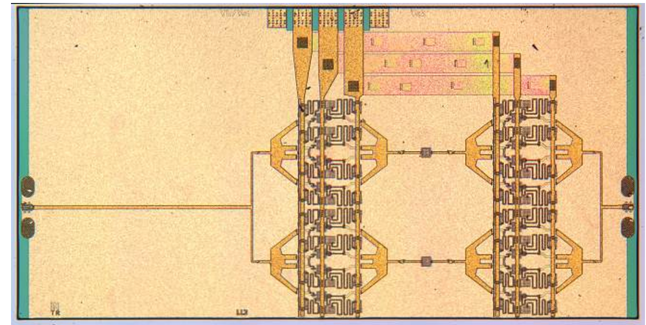

Fig. 1. An IC Micrograph of the 220 GHz, 2-stage, 8-cell InP HBT solid-state power amplifier. Dimensions: 2.42x1.22mm^2.

I. Introduction

Future synthetic aperture radars and high resolution imaging systems will benefit from the continued development of solid-state power amplifiers (SSPA), where recently there has been active interest to increase the saturated power at 220GHz. These high power signals may be used to drive multiplier chains for THz applications or to drive higher power vacuum tube amplifiers around the 220GHz low-loss free space propagation window. For many wireless applications, significant output power will be necessary at 220GHz and above to overcome attenuation due to weather events.

The highest output power reported for a solid-state G-band (140-220GHz) power amplifier is from an InP HEMT technology having 75mW of saturated output power at 210GHz in a waveguide-block package [1]. Recently, advances in InP HBT gain and bandwidth at the 250nm node have made it a viable candidate for much higher power amplification at high mm- and sub-mm-wave frequencies [2]. From these technology advancements, InP HBT SSPA amplifiers have been reported with 48.8mW and 58.4mW P_{out} at 220GHz [3,4].

For a PA cell to have appreciable gain and P_{out} at 220GHz, the transistor finger count and length will be limited by issues associated with device self-heating and interconnect parasitics forming the multi-finger device. At these frequencies, higher P_{out} is achieved through power combining. Careful design of the combiner is necessary to avoid excessive skin-effect loss; no significant increase in P_{out} can come from on-chip combining if the insertion loss exceeds ~ 1.0–1.5dB. 4-Cell and 8-Cell InP HBT SSPA's have been demonstrated using 4:1 Dolph-Chebyshev structures [1,3], as well as /4-wave 2:1 combiners in low-loss thin-film microstrip form at 220GHz [4].

For the 8-cell, single-stage amplifier reported in [3] (which the work here leverages), insufficient source power at 220GHz was available to drive the amplifier into deep saturation. In order to demonstrate the maximum P_{out} available from this 220GHz SSPA amplifier approach and architecture, the output driver must be presented with higher RF power. This necessitates that the overall amplifier have more gain, *and* that the stage preceding the output driver deliver the requisite RF power so that the output driver may operate in deep saturation.

In this paper, a 2-Stage 8-cell InP HBT SSPA is reported using 2:1 and 4:1 low-loss on-wafer microstrip power combining. The SSPA exhibits 14.8dB S_{21} gain at 220GHz and 3-dB small-signal bandwidth from at least 206 to 240GHz. P_{DC} is 4.46W. At 220GHz, 90mW P_{out} (13.6mW P_{in}) with simultaneous 8.2dB power gain has been demonstrated. Over 10GHz bandwidth, at least 75mW P_{out} is observed from 210-220GHz. The work reported here represents a record for P_{out} achieved at these frequencies from any technology using on-wafer power combining.

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II. 250nm Indium Phosphide HBT Process

The power amplifier MMIC reported here use a 250nm InP HBT technology with a ~4.5V breakdown voltage. A single HBT has a peak bandwidth of f_{max} = 700GHz and f_T = 400GHz. At the amplifier's quiescent bias of J_e= 5.5mA/µm^2, f_{max} = 590GHz and f_T =350GHz. The power amplifier MMIC uses common-emitter (CE) and common-base (CB) HBTs to form the cascode cell, with a total emitter periphery of 4-fingers x 6um L_e = 24um for each device. The 4-finger CE HBT exhibits f_{max} = 530GHz and f_T = 333GHz at the amplifier's quiescent bias. This shows that parasitics associated with the device assembly does little to decrease the available gain at 220GHz for the PA cell. The physical sizes of device footprints are 18x7.5µm^2 for CE and 6x9µm^2 for CB configuration. A more complete analysis and reporting of these cells can be found in [5].

A four-metal interconnect stack is used in MMIC fabrication. Compact, stacked interconnect vias provide access from the top layer of metal interconnect for signal (3-µm thick) to the three lower layers (each 1-µm thick). Interconnects are separated by 1-µm BCB interlayer dielectric layers. MIM capacitors are 0.3fF/µm^2 and thin-film resistors are 50-Ohm/square [6,7].

III. MMIC Power Amplifier Design

Amplifier circuits were simulated in ADS using an Agilent-HBT model for the 250nm HBT technology. All interconnects, transmission lines, MIM capacitors, probe pads, and power splitter/combiner structures were simulated using ADS Momentum, a 2.5-D electromagnetic simulator.

Thin film microstrip transmission lines were formed using the lowest metal interconnect layer as ground and the upper three metal interconnect layers for signal transmission. Substrate-shielded, non-inverted thin-film microstrip wiring was selected to minimize interconnect inductance between the ground plane and the emitter terminal for the common emitter (CE) HBT and between the ground plane and the base terminal for the common base (CB) HBT. This is especially

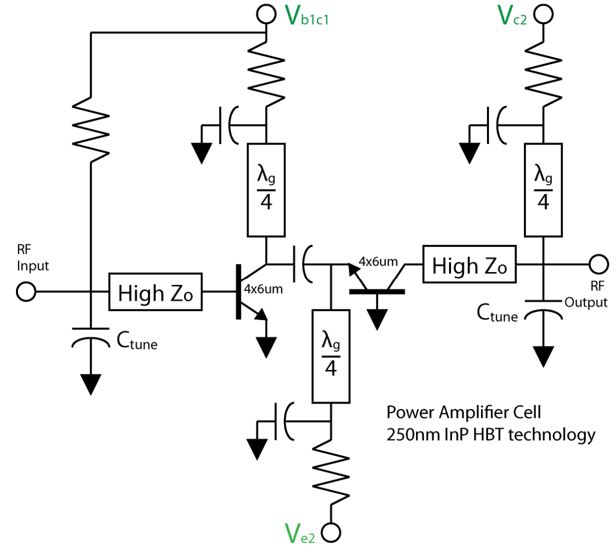


Fig. 2. Schematic of the cascode HBT power amplifier cell.

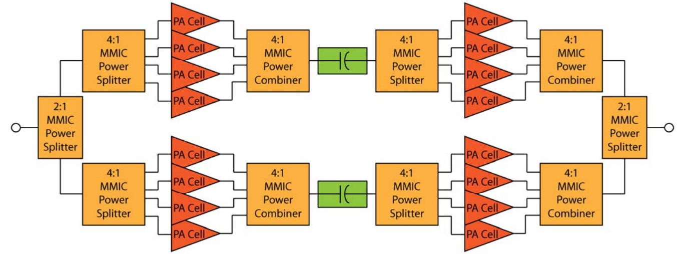
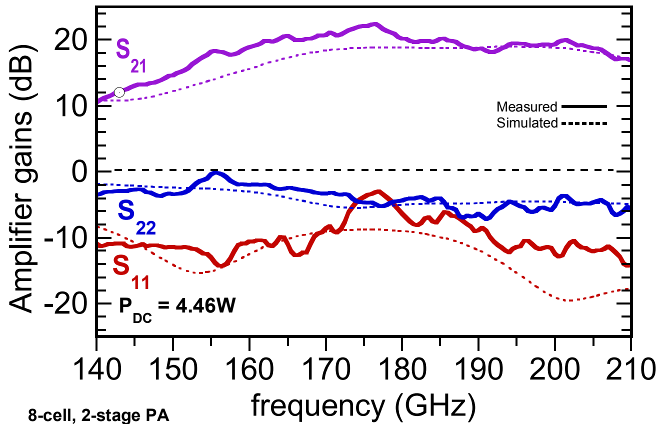


Fig. 3. Circuit Block Schematic of the 2-stage 8-cell SSPA.



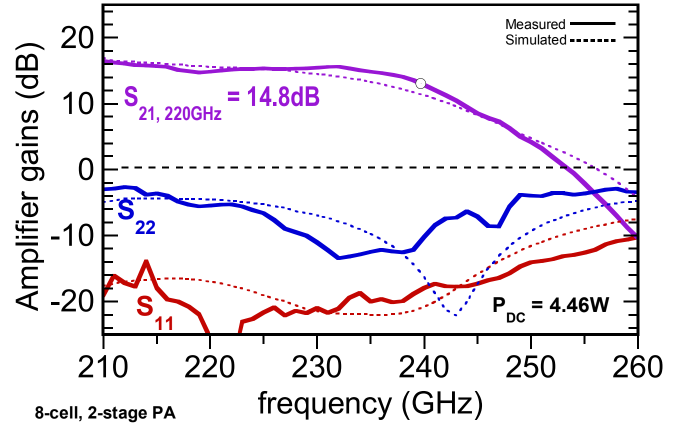


Fig. 4. S-parameters of the 2-stage 8-cell SSPA in two millimeter-wave frequency bands. The SSPA showed 14.8 dB small signal gain at 220 GHz. Input return loss is greater than 10 dB from 190 GHz to 260 GHz and S21 gain is greater than 12 dB from 142 to 240 GHz.

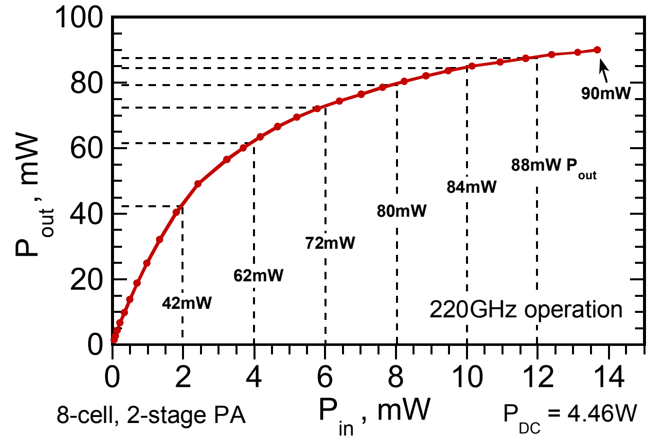
important for the common base HBT, as additional inductance at the base causes significant reduction to amplifier stability margin. Use of a substrate-shielding ground plane keeps signal coupling between PA cells through the 12.8 ε_r InP substrate small. For amplifiers with high gain, unintentional feedback through the substrate to preceding stages can potentially cause the amplifier to oscillate. Minimal ground return inductance of a large, continuous ground plane also helps to make the amplifier more broadband, since additional reactive cancellation is not needed.

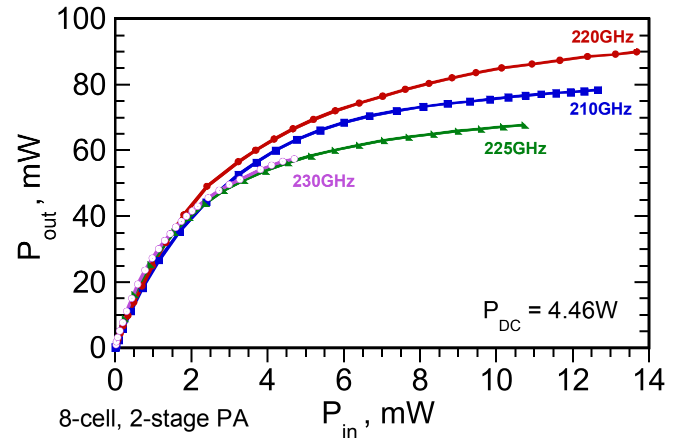
A single power amplifier (PA) cell was designed with a cascode topology using a 4-finger CE HBT and a 4-finger CB HBT as shown in Fig. 2. DC bias was provided to the HBTs using quarter-wave chokes. The input of the amplifier cell was matched for maximum gain to a 50-ohm system Z_o. The output of the amplifier cell was terminated such that the CB collector voltage and current would swing along a class-A load line within the high performance operating area of the device. This operating area is the region of the I_c vs. V_{cb} curves defined by the HBT saturation voltage, Kirk current, safe long term operating power density, CB breakdown voltage, and the variation of MAG/MSG with DC bias. The quiescent DC bias selected was at J_e=5.5mA/μm^2 and V_{cb}= 1.5V.

Multiple levels of on wafer power splitting and combining were used to combine for large output power from multiple PA cells. 2:1 and 4:1 combiners have previously been demonstrated [3,4]. An 8-cell amplifier demonstrated previously could not be driven completely into saturation because of limited source power [4]. To resolve this limitation and increase overall amplifier gain, the PA cells were duplicated to act as a pre-driver for the output cells and cascaded to form the overall 2-stage SSPA as shown in Fig. 3. For DC isolation between stages, a DC blocking capacitor was designed for low insertion loss at 220GHz. From 1-port S-parameter measurements, this structure has 1.1-1.3dB insertion loss. Additionally, for the multi-stage design, bypass capacitors with resistive damping were added to power supply buses to dampen standing waves on the power supply revealed in simulation.

IV. Experimental Results

On-wafer SSPA MMIC S-parameter measurements were performed using 140-220GHz and 220-325GHz OML T/R frequency extender modules, controlled by an Agilent 8510C VNA. GGB WR05 and WR03 waveguide coupled probes were used for wafer probing, respectively. LRRM Probe tip calibration was performed using WinCal XE [8]. The amplifier P_{DC} is 4.46W. At a DC bias of V_{c1} = 2.75V, I_{c1} = 599mA, V_{c2} = 2.3V, I_{c2} = 582mA, V_{e2} = -2.3V, and I_{e2} = 609mA, the measured small signal power gain of the 8-cell SSPA at 220GHz is 14.8dB. Figure 4 shows the measured S-parameters for the amplifier in two bands. The S21 gain is greater than 12dB from 142 to 240GHz and input return loss is greater than 10dB from 190 GHz to 260 GHz.





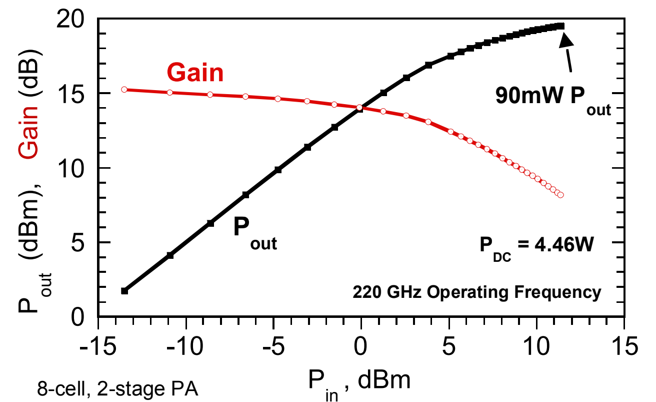


Fig. 5. A 220GHz power sweep (top) shows that the SSPA provides 90mW saturated output power P_{out}. Power sweeps at various frequencies (middle) for the SSPA show greater than 65mW saturated P_{out} from 210-225GHz. In a dB-formatted plot of gain and P_{out} vs. P_{in} (bottom) the SSPA demonstrated 8.2dB gain at 220 GHz when outputting 90mW.

For large signal measurements, a VDI amplifier multiplier chain (AMC 16× multiplier) is used for power-sweep testing of the DUT from 210 to 230GHz. Output power was measured by an Erickson PM4 sub-mm wave power meter. Power data was corrected for measured insertion loss of the components between the probe tips and power meter.

Using identical DC bias conditions from RF testing, the 2-stage 8-cell amplifier demonstrates 90mW output power P_{out} with 8.2dB compressed gain at 220 GHz (13.6mW P_{in}). For an 8mW P_{in} at 220GHz, the amplifier P_{out} is 80mW and the compressed gain is 10dB. From 210-225GHz, the SSPA has greater than 65mW saturated P_{out}, and from 210-220GHz the SSPA shows greater than 75mW saturated P_{out}.

VII. CONCLUSION

A 220GHz Solid State Power Amplifier MMIC has been presented demonstrating 90mW output power P_{out} at 8.2dB compressed gain. From 210-225GHz, the SSPA had greater than 65mW saturated P_{out}, and from 210-220GHz the SSPA showed greater than 75mW saturated P_{out}. This work represents a record for P_{out} achieved at these frequencies from any technology using on-wafer power combining.

VIII. ACKNOWLEDGMENTS

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