InGaAs/InP DHBTs with Emitter and Base Defined through Electron-beam Lithography for Reduced C_{cb} and Increased RF Cut-off Frequency

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High-frequency InP HBTs enable high-speed digital logic, mixed-signal, and sub-mm wave integrated circuits [1]. Increases in RF performance in HBTs can be achieved through epitaxial thinning of the base and collector junction thicknesses, T_b and T_c, lithographic narrowing of the emitter and base mesa widths, W_e and W_b, and reduction of the resistances associated with the emitter and base, R_{ex} and R_{bb}.

We report here InP DHBTs fabricated using a JEOL 6300FS electron-beam lithography system to define W_e = 150 nm emitter junctions and 150 nm base contacts on each side of the emitter, using novel positive and negative tone e-beam photoresist processes. Emitter-base misalignment is < 25 nm, and total base mesa width W_b = 450 nm, the narrowest reported to date. Small base-to-emitter misalignment fosters reductions in both R_{bb} and base-collector capacitance C_{cb} by enabling the formation of narrow mesas with symmetric, two-sided base contacts of width ~ L_T, the transfer length for carriers in the base.

Simultaneous f_τ = 530 GHz and f_{max} = 750 GHz were measured at a bias of I_c = 12.4 mA, V_{ce} = 1.5 V. Current-gain cutoff frequency f_τ is slightly higher than previous devices with record f_{max} [2] due to the thinning of the drift collector from 100 nm to 70 nm. Narrowing the base mesa via e-beam lithography to reduce C_{cb} is largely responsible for increasing f_{max} 33% from previous T_c = 70 nm epitaxial designs with similar base thicknesses [3].

The emitter contact and mesa were formed through blanket refractory metal deposition and dry etch [4]. The emitter n-$In_{0.53}Ga_{0.47}As$ cap doping has been increased from ~ 6.0 to 8.0 × 10^{19} cm^{-3}. The base epitaxial layer has been thinned from 30 nm to 25 nm, with a 1.0-0.5 × 10^{20} cm^{-3} doping grade. The drift collector has been thinned from 100 nm to 70 nm, including a 9.5 nm InGaAs setback region and 12 nm InGaAs/InAlAs chirped superlattice grade. The base contact and base mesa were defined through e-beam lithography, with a lifted-off base contact. Collector and backend formation were formed through liftoff, wet etch, and BCB planarization [4].

DC measurements and biasing were performed with an Agilent 4155 Parameter Analyzer, and 1-67 GHz S-parameter measurements were done with an Agilent E8361A PNA. From DC data, common-emitter current gain β = 14, common-emitter breakdown voltage V_{bceo} = 2.44 V and collector contact resistivity and sheet resistance were $\rho_c = 12\ \Omega\cdot\mu m^2$ and $R_{sh} = 14\ \Omega/\square$. Emitter contact resistivity $\rho_{ex} = 2\ \Omega\cdot\mu m^2$, the lowest reported n-contact resistivity in a real InP HBT to date. $R_{bb} = 40\ \Omega$, and C_{cb} = 3.0 fF were extracted from RF measurements. Peak RF performance of simultaneous f_τ/f_{max} = 530 GHz / 750 GHz was obtained at a bias of I_c = 12.4 mA (J_e = 27.6 mA/μm^2), V_{ce} = 1.5 V (V_{cb} = 0.54 V), and total power density > 40 mW/μm^2. Good fit was obtained between measured S-parameters and simulated S-parameters based on a hybrid-π equivalent circuit model.

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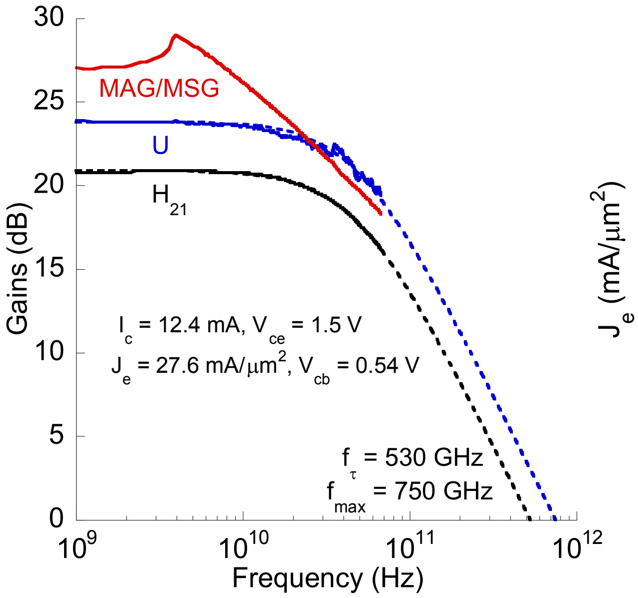

Fig. 1: Measured RF gains from 1-67 GHz at peak performance bias, with extracted cutoff frequencies

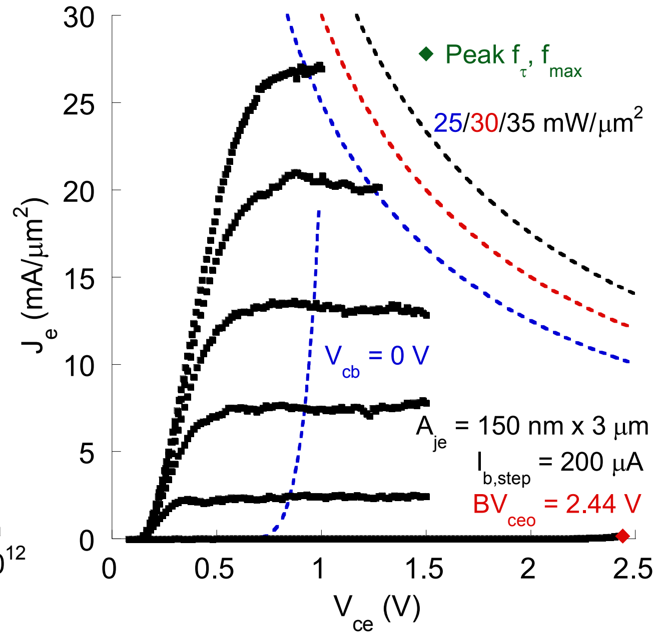

Fig. 2: Common-emitter I-V curves normalized to emitter junction area, with breakdown and peak bias.

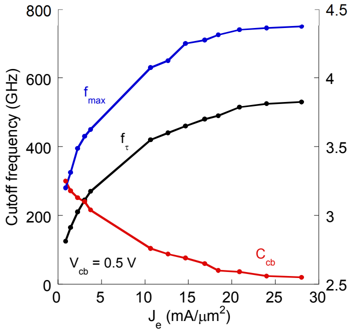

Fig. 3: f_τ, f_{max}, and C_{cb} variation with J_e and V_{cb}

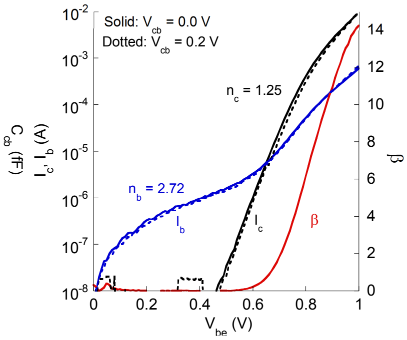

Fig. 4: Gummel plot and DC current gain with extracted ideality factors

T (Å)	Material	Doping (cm^{-3})	Description
100	$In_{0.53}Ga_{0.47}As$	8 × 10^{19} : Si	Emitter cap
150	InP	5 × 10^{19} : Si	Emitter
150	InP	2 × 10^{18} : Si	Emitter
250	InGaAs	1–0.5 × 10^{20} : C	Base
95	$In_{0.53}Ga_{0.47}As$	1 × 10^{17} : Si	Setback
120	InGaAs / InAlAs	1 × 10^{17} : Si	B-C Grade
30	InP	5 × 10^{18} : Si	Pulse doping
455	InP	1 × 10^{17} : Si	Collector
75	InP	1 × 10^{19} : Si	Sub-collector
50	$In_{0.53}Ga_{0.47}As$	4 × 10^{19} : Si	Sub-collector
3000	InP	1 × 10^{19} : Si	Sub-collector
35	$In_{0.53}Ga_{0.47}As$	Undoped	Etch stop
Substrate	SI InP		

Fig. 5: Epitaxial design

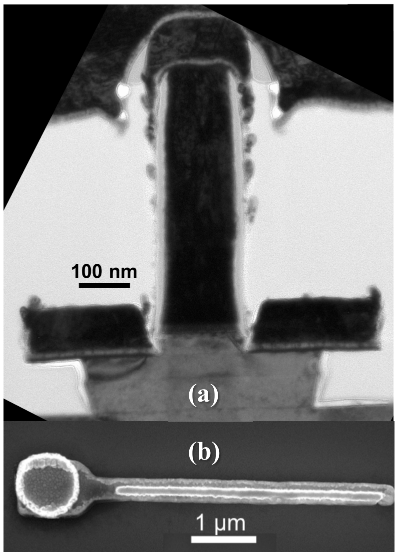

Fig. 7: (a) TEM cross-section and (b) top-down SEM of emitter and base mesa

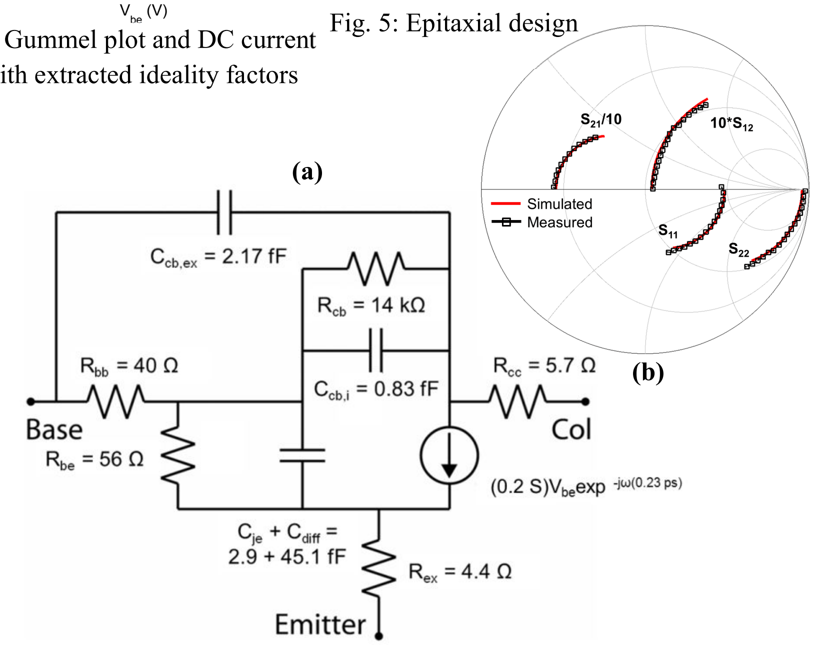

Fig 8: (a) Hybrid-π equivalent circuit and (b) modeled/measured S-parameters from 1-67 GHz at bias of I_c = 12.4 mA, V_{ce} = 1.5 V.