International Symposium on Compound Semiconductors 2012

InGaAs/InP DHBTs with Emitter and Base Defined through Electron-beam Lithography for Reduced C_{cb} and Increased RF Cut-off Frequency

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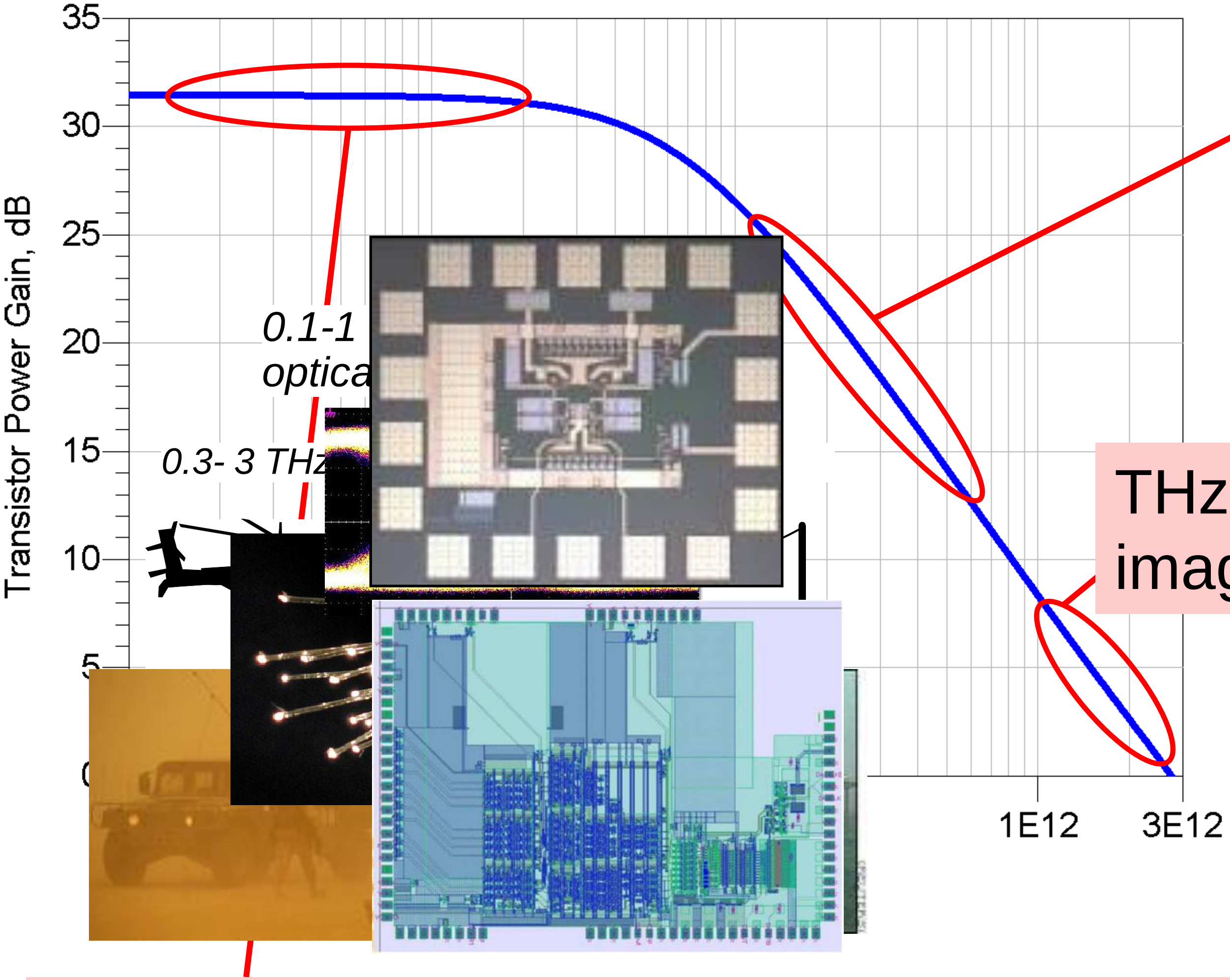
Agilent Technologies

UCSB

Outline

- Motivation
- HBT Design & Scaling
- Fabrication Process & Challenge
- Electrical Measurements
- Conclusion

Why THz Transistors?

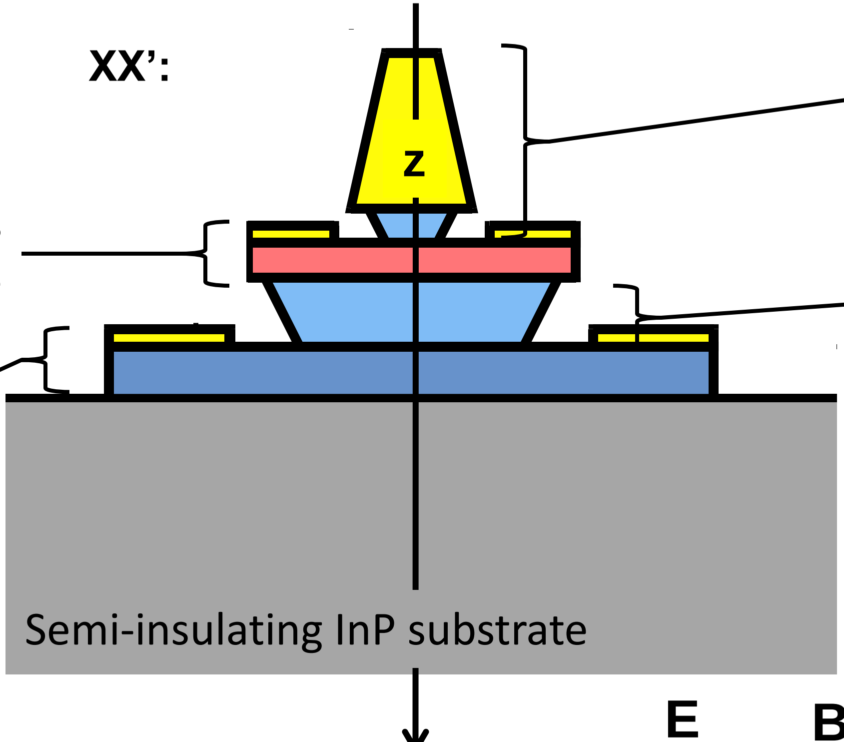


Digital logic for optical fiber circuits

THz amplifiers for imaging, communications

High gain at microwave frequencies:
Precision analog design, high resolution ADCs, DACs

Type-I InP DHBTs at UCSB

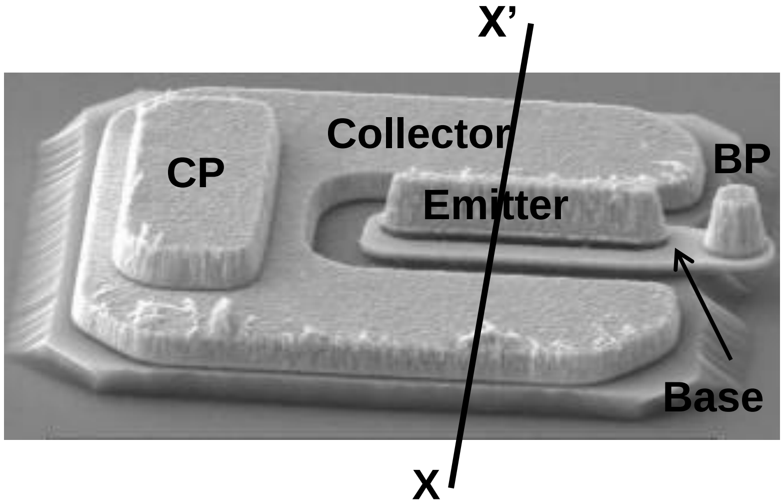


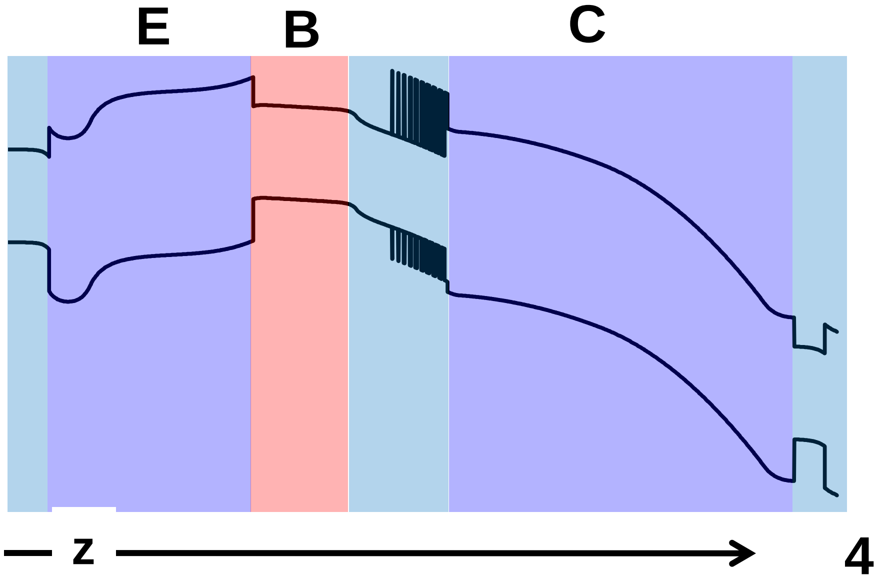
Emitter:
n^{++} InGaAs cap
n InP

Base:
p^{++} InGaAs
Doping grade

Drift collector:
n^{-} InGaAs/InAlAs grade
n^{-} InP

Sub-collector:
n^{++} InGaAs cap
n^{++} InP

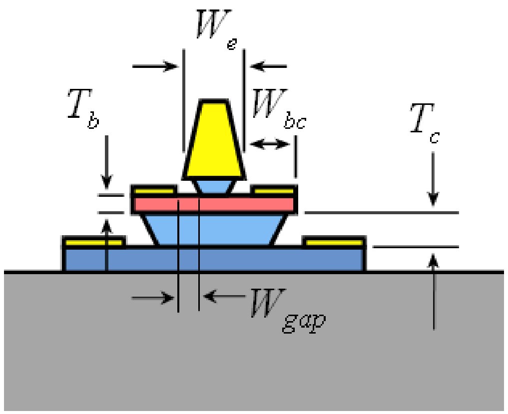




HBT Scaling Laws

To double bandwidth of a mesa DHBT:

Keep ***constant*** all ***resistances*** and ***currents***
Reduce 2:1 all ***capacitances*** and ***transport delays***



(emitter length L_e)

Parameter	Change
collector depletion layer thickness	decrease ***2:1***
base thickness	decrease ***1.41:1***
emitter junction width	decrease ***4:1***
collector junction width	decrease ***4:1***
emitter contact resistivity	decrease ***4:1***
base contact resistivity	decrease ***4:1***
current density	increase ***4:1***

Epitaxial scaling

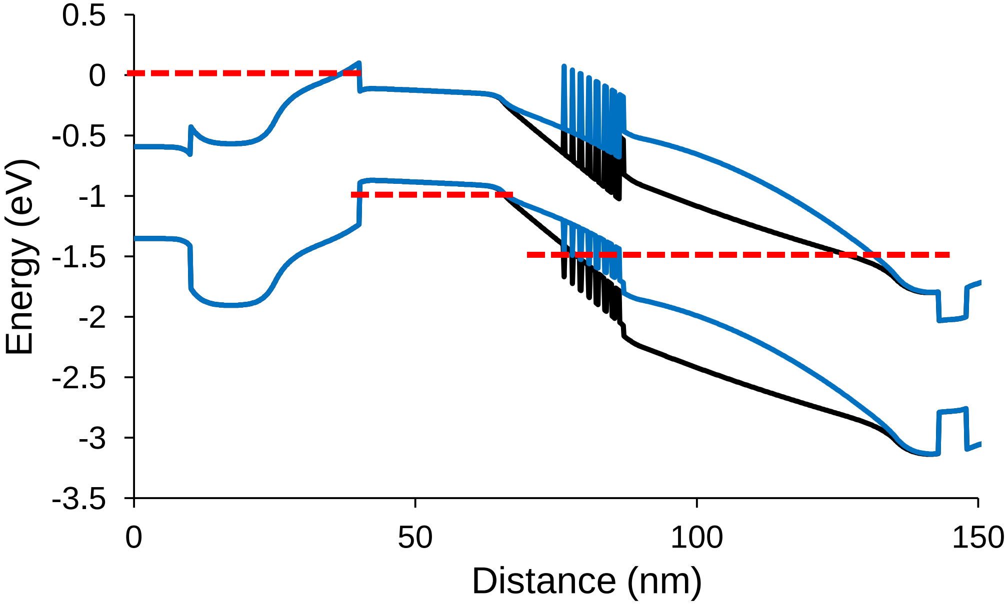
Lateral scaling

Surface prep & doping

Keep lengths the same, reduce widths 4:1 for thermal considerations

Epitaxial Design

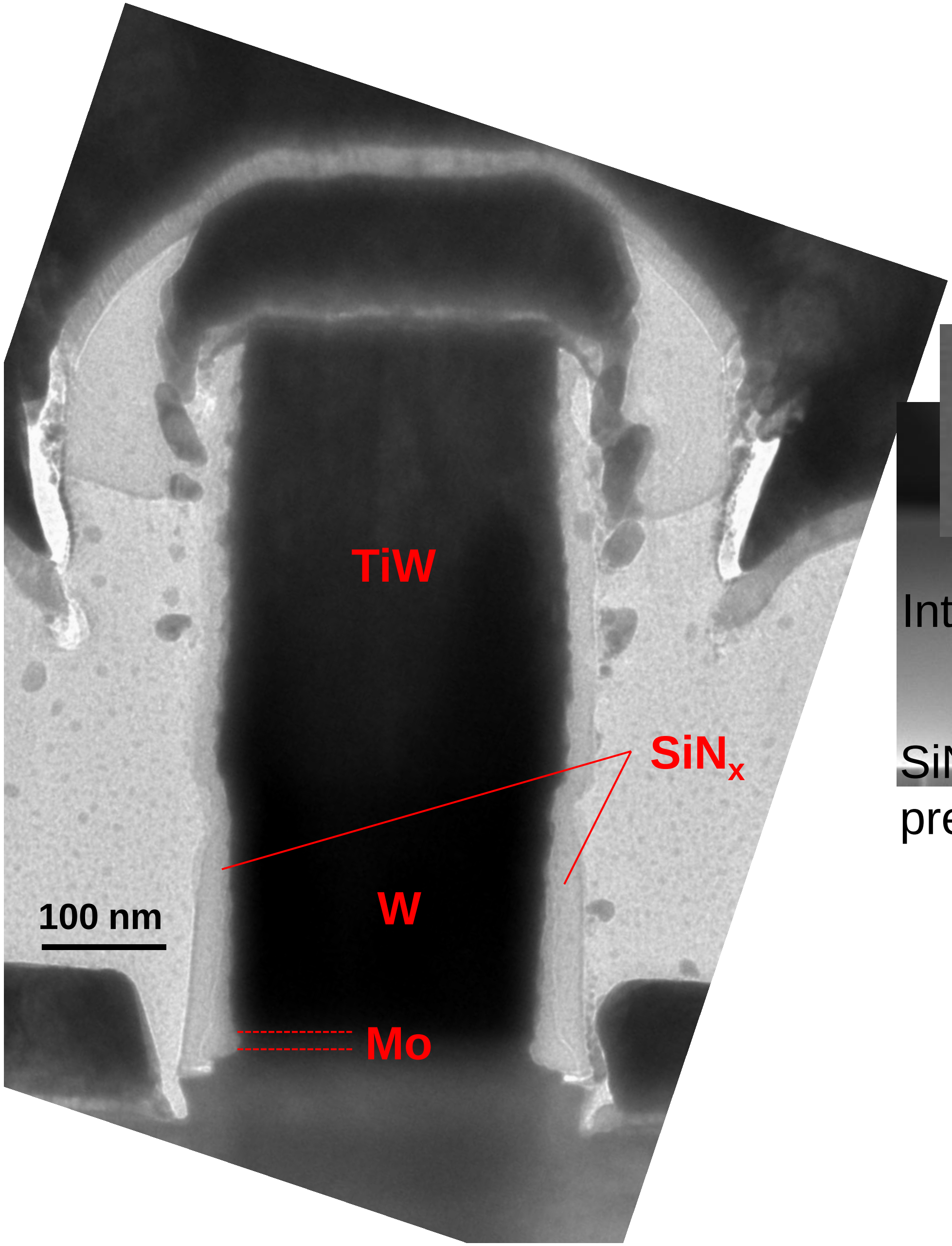
T(nm)	Material	Doping (cm^{-3})	Description
10	$In_{0.53}Ga_{0.47}As$	$8\cdot10^{19}$: Si	Emitter cap
15	InP	$5\cdot10^{19}$: Si	Emitter
15	InP	$2\cdot10^{18}$: Si	Emitter
25	InGaAs	$1\text{-}0.5\cdot10^{20}$: C	Base
9.5	$In_{0.53}Ga_{0.47}As$	$1\cdot10^{17}$: Si	Setback
12	InGaAs / InAlAs	$1\cdot10^{17}$: Si	B-C Grade
3	InP	$5\cdot10^{18}$: Si	Pulse doping
45.5	InP	$1\cdot10^{17}$: Si	Collector
7.5	InP	$1\cdot10^{19}$: Si	Sub Collector
5	$In_{0.53}Ga_{0.47}As$	$4\cdot10^{19}$: Si	Sub Collector
300	InP	$1\cdot10^{19}$: Si	Sub Collector
3.5	$In_{0.53}Ga_{0.47}As$	Undoped	Etch stop
Substrate	SI : InP		

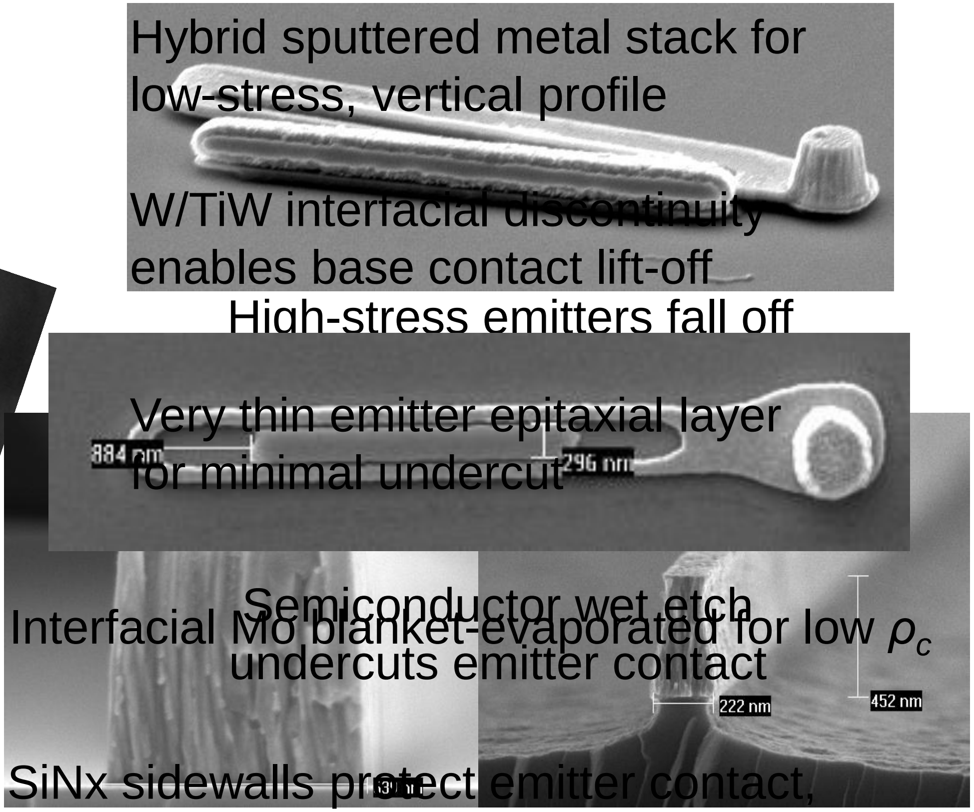


V_{be} = 1.0V, V_{cb} = 0.5V, J_e = 0, 27 mA/µm²

Thin ***(70 nm) collector*** for ***balanced f_τ/f_{max}***
High emitter/base doping for low ***R_{ex}/R_{bb}***

Sub-200 nm Emitter Anatomy





Hybrid sputtered metal stack for low-stress, vertical profile

W/TiW interfacial discontinuity enables base contact lift-off

High-stress emitters fall off

Very thin emitter epitaxial layer for minimal undercut

Interfacial Mo blanket-evaporated for low ρ_c

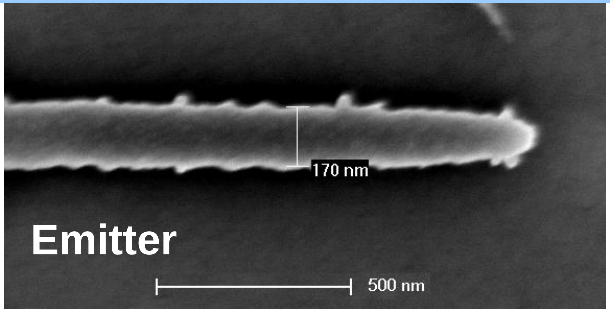
Semiconductor wet etch undercuts emitter contact

SiNx sidewalls protect emitter contact, prevent emitter-base shorts

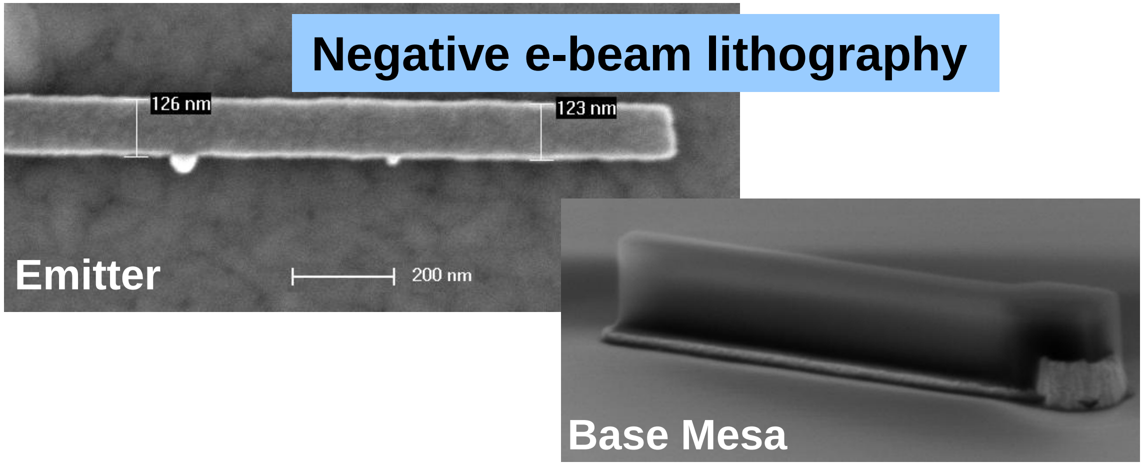
Single sputtered metal has non-vertical etch profile

Lithographic Scaling and Alignment

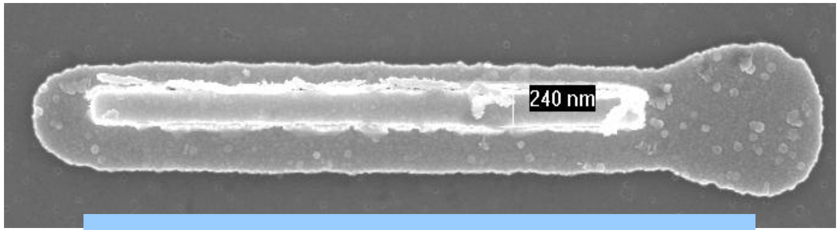
Positive i-line lithography



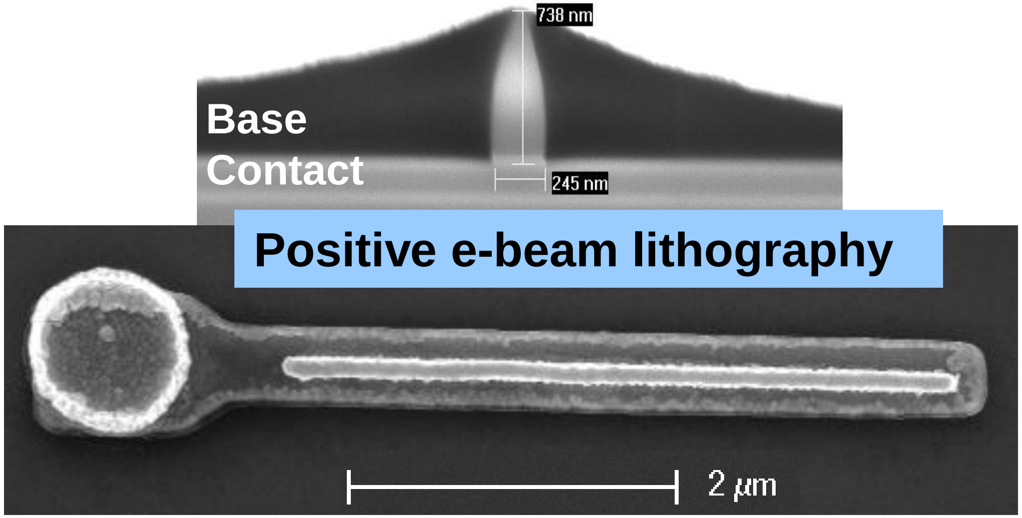
Negative e-beam lithography



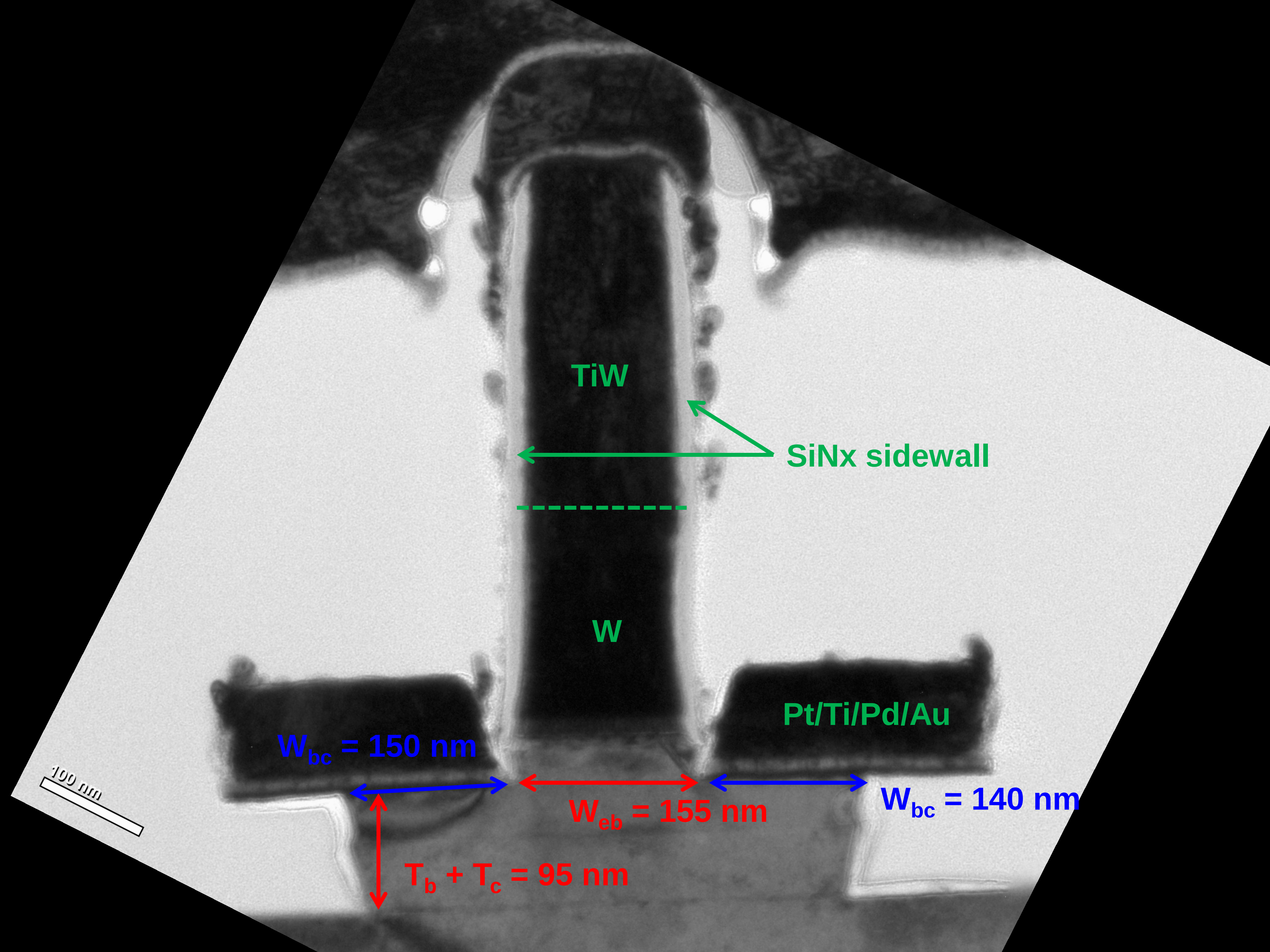
E-beam lithography needed to define < 150 nm emitters and for < 50 nm emitter-base contact misalignment



Negative i-line lithography



Positive e-beam lithography


TiW
SiNx sidewall
W
Pt/Ti/Pd/Au
W_{bc} = 150 nm
W_{eb} = 155 nm
W_{bc} = 140 nm
$T_b + T_c$ = 95 nm
100 nm

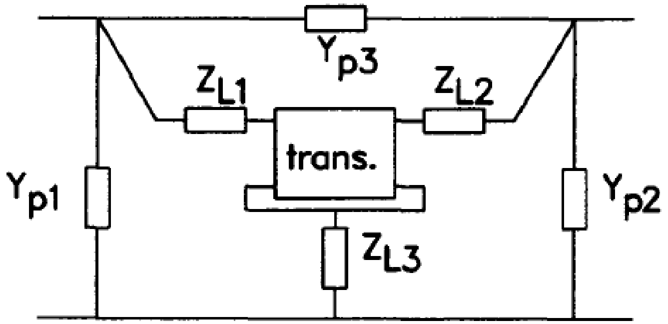
Measurement

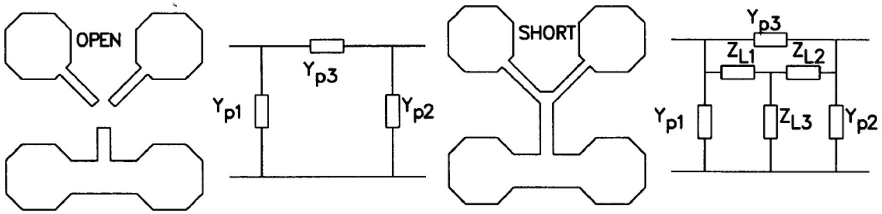
RF measurements conducted using Agilent E8361A PNA from 1-67 GHz

DC bias and measurements made with Agilent 4155 SPA

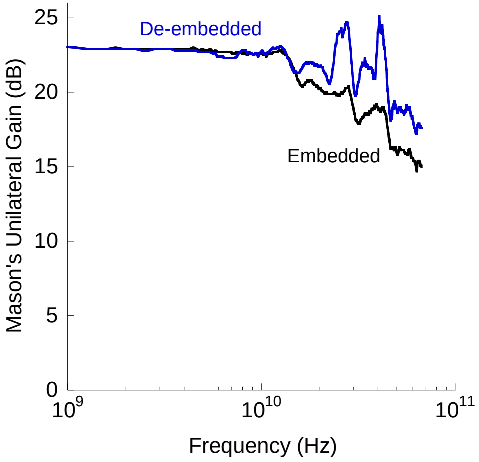
Off-wafer LRRM calibration, ***lumped-element pad stripping*** used to de-embed device S-Parameters

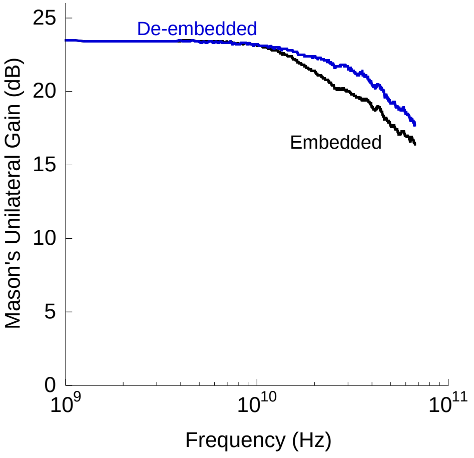
Isolated pad structures used to provide clean RF measurements

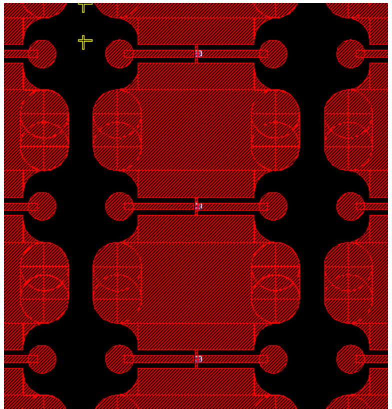


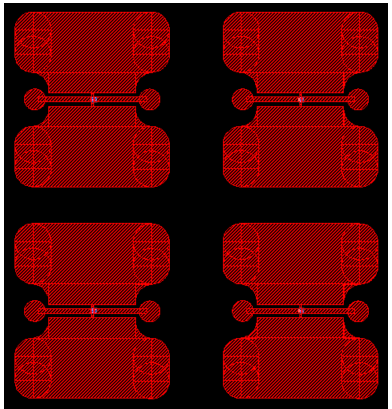


$$Y_{trans} = ((Y_{dut} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1})^{-1}$$

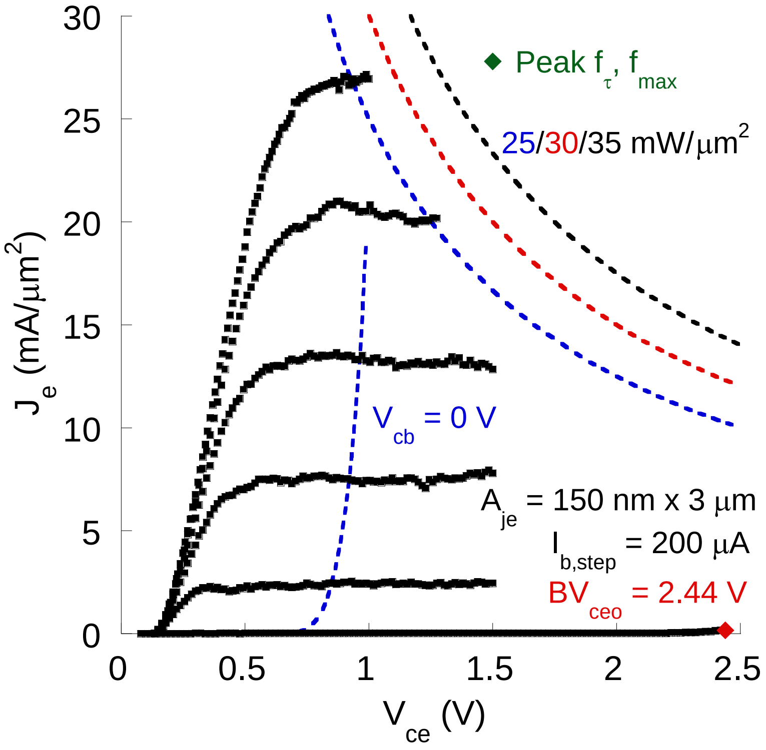


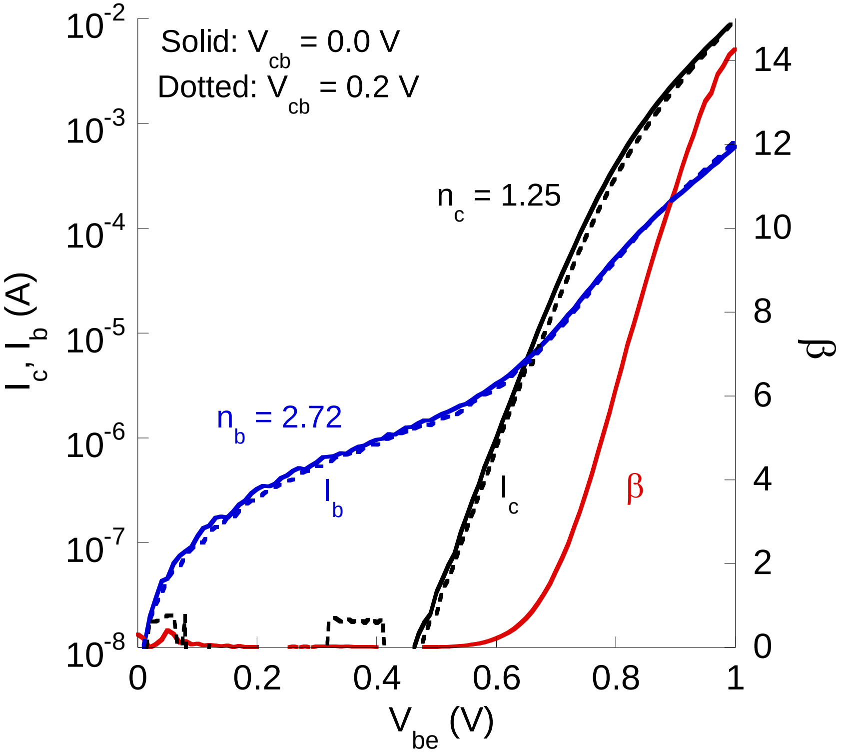






DC Data





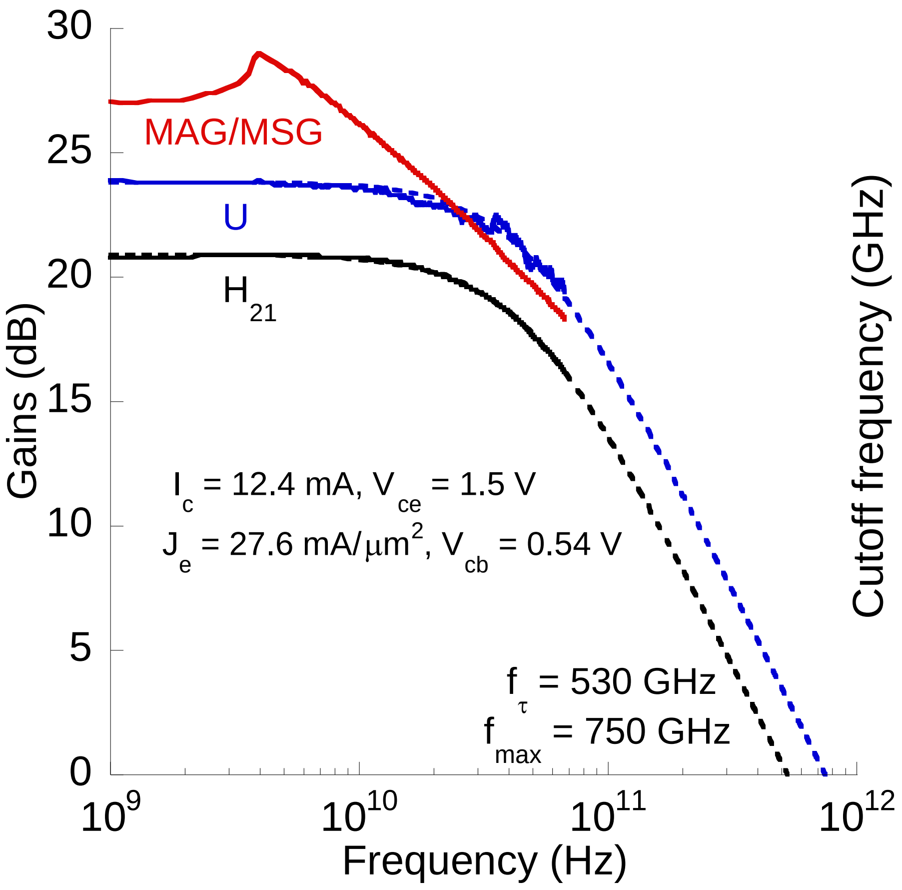
β = ***14*** for 150 nm junction

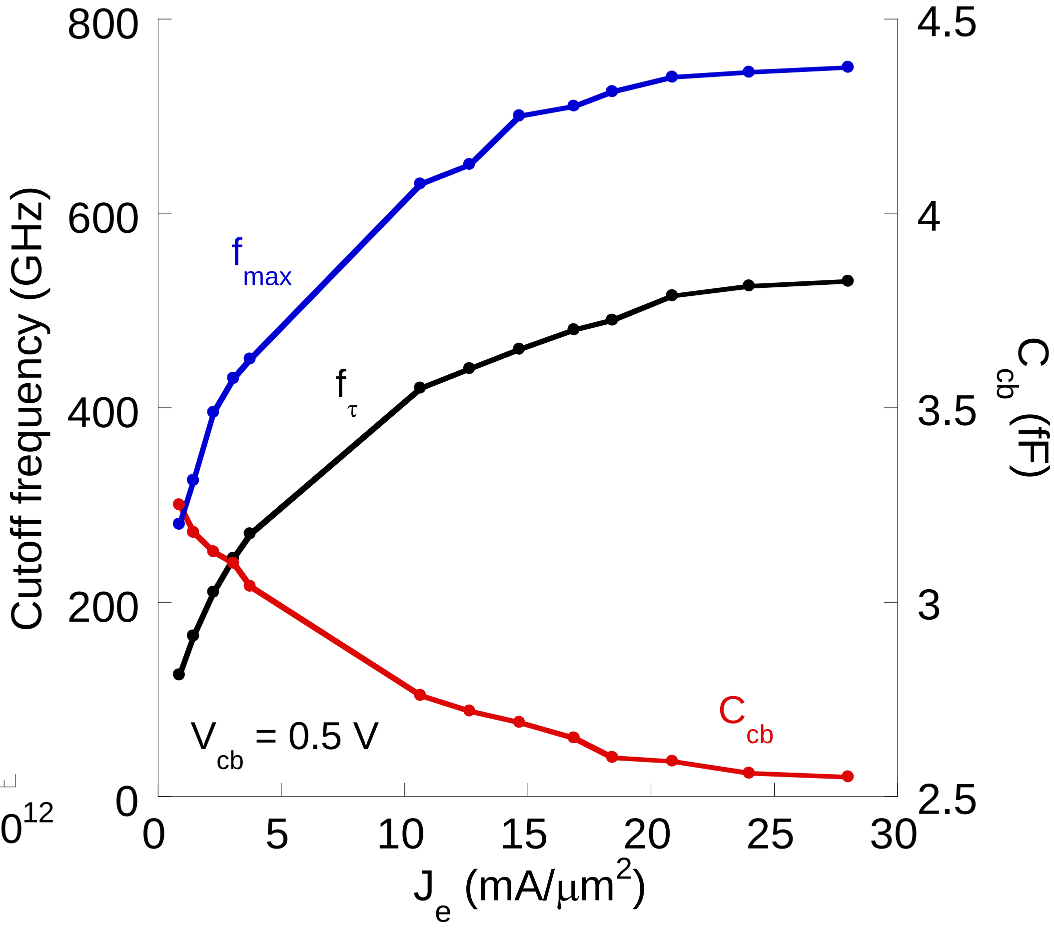
VB_{ceo} = ***2.44 V*** @ J_e = 15 kA/cm^2

R_{ex} ≈ ***2 Ω·μm²*** (RF extraction)

Collector ρ_{sheet} = ***14 Ω/□***, ρ_c = ***12 Ω·μm²***

RF Data





Peak ***RF performance at >40 mW/µm²***

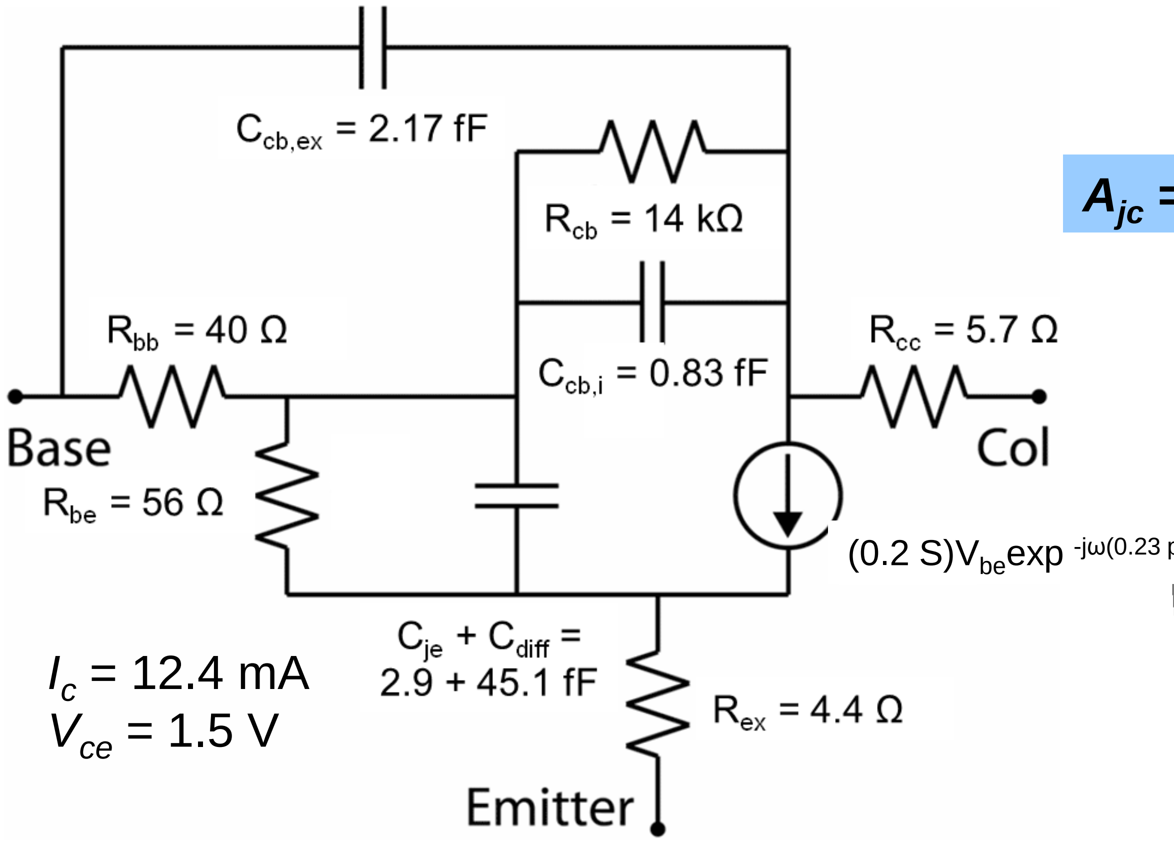
Kirk limit not reached

Equivalent Circuit Model

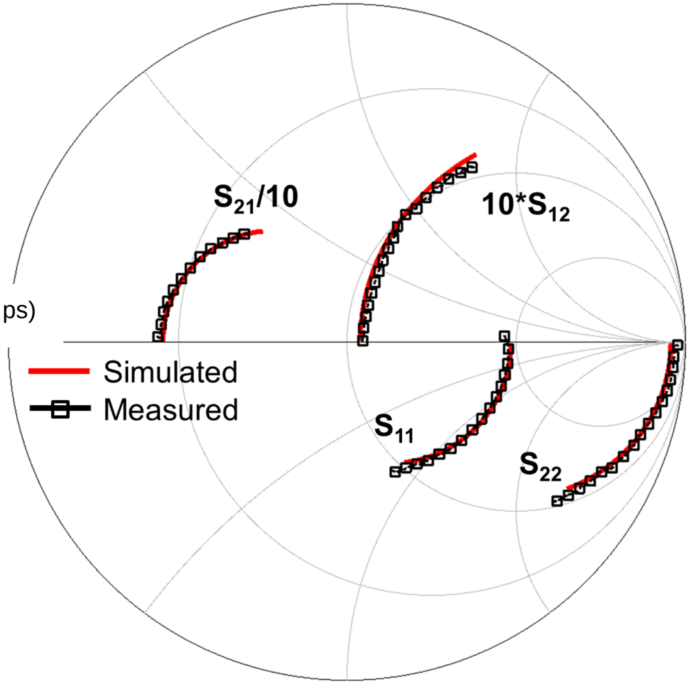
ρ_{ex} = 2 Ω·μm^2

C_{cb} = 3.0 fF

A_{jc} = 1.86 μm^2 ~ 450 nm x 4 μm



I_c = 12.4 mA
V_{ce} = 1.5 V



Lowest ρ_{ex} to date due to Mo contact, highly doped epi

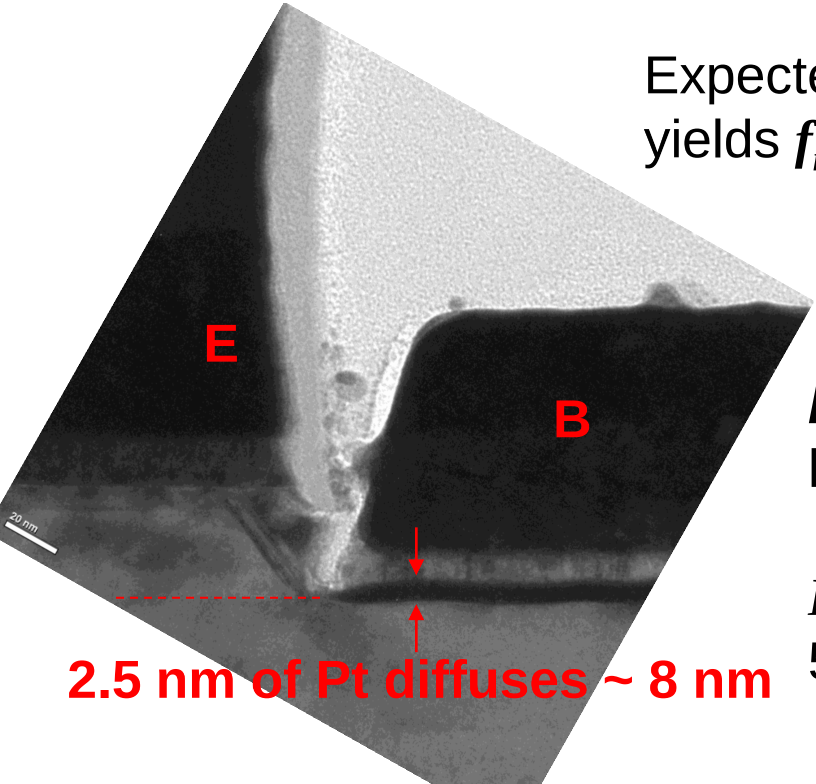
C_{cb} lower than 100 nm collector epi designs due to E-beam litho

Performance Analysis

$$\frac{1}{2\pi f_\tau} = \underbrace{\tau_b + \tau_c}_{230\text{ fs}} + \underbrace{\frac{nk_BT}{qI_c}C_{je}}_{15\text{ fs}} + \underbrace{\left(\frac{nk_BT}{qI_c}+R_{ex}+R_c\right)C_{cb}}_{45\text{ fs}}$$

τ_{ec} dominated by ***transit delays***, high ***ideality factor reduces f_τ ~ 10%***

Expected base ρ_c = 4 Ω·µm^2 and R_{sh} = 800 Ω/□ yields f_{max} ***> 1.0 THz for same f_τ***



Epitaxial design, ***process damage*** explain high η_b, R_{bb}

R_{sh} increased by ***base contacts reacting*** with 5 nm (20 %) of base

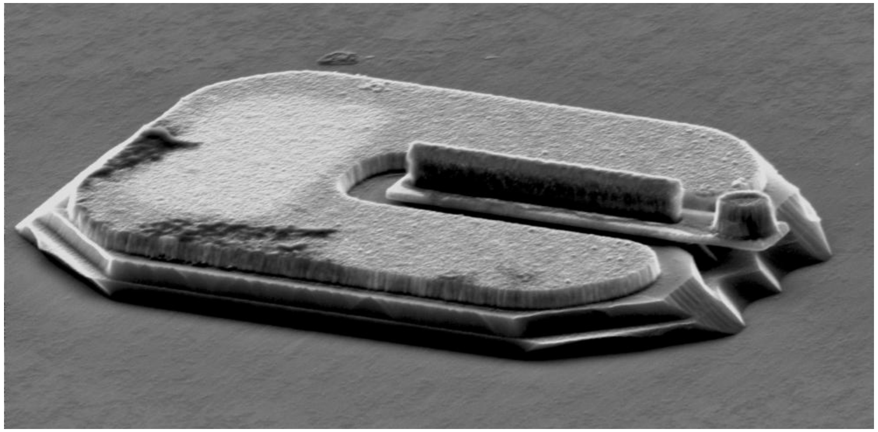
Conclusion

E-beam lithography used to define narrow emitter, ***narrowest base mesa*** reported to date

Narrow mesa, low emitter ρ_c enable 33% increase in f_{max} from previous UCSB results with 70 nm collector thickness

Epitaxial thinning increased f_τ by 10% from 100 nm UCSB designs

1 THz bandwidth possible with improved base contact process



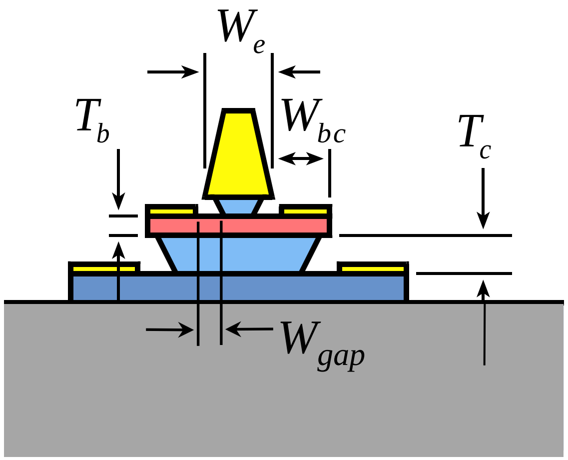
This work was supported by the DARPA CMO Contract No. HR0011-09-C-0060.

Portions of this work were done in the UCSB nanofabrication facility, part of the NSF-funded NNIN network, and the MRL, supported by the MRSEC Program of the NSF under award No. MR05-20415.

Questions?

Extra Slides

Bipolar Scaling Laws



(emitter length L_e)

$$\tau_b \approx T_b^2 / 2D_n$$

$$\tau_c = T_c / 2v_{sat}$$

$$C_{cb} = \varepsilon A_c / T_c$$

$$I_{c,\max} \propto v_{sat} A_e (V_{cb} + V_{bi}) / T_c^2$$

$$\Delta T \propto \frac{P}{L_e}\left[1 + \ln\left(\frac{L_e}{W_e}\right)\right]$$

$$R_{ex} = \rho_{c,e} / A_e$$

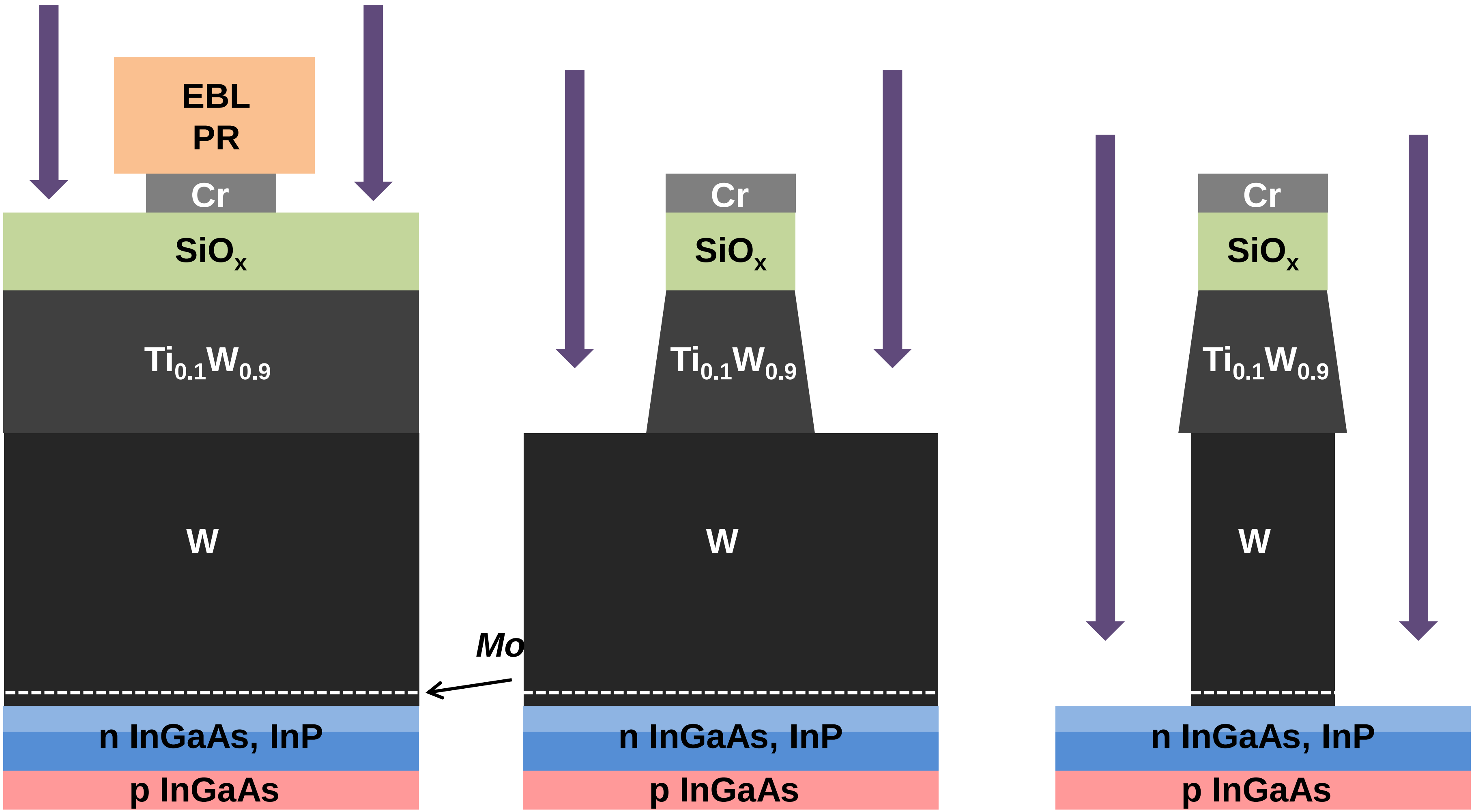
$$R_{bb} = \frac{\rho_{sh}}{L_e}\left(\frac{W_{bc}}{6} + \frac{W_{gap}}{2} + \frac{W_e}{12}\right) + \frac{\rho_{c,b}}{A_{c,b}}$$

Fabrication: Emitter contact

Cl_2/O_2 ICP etch

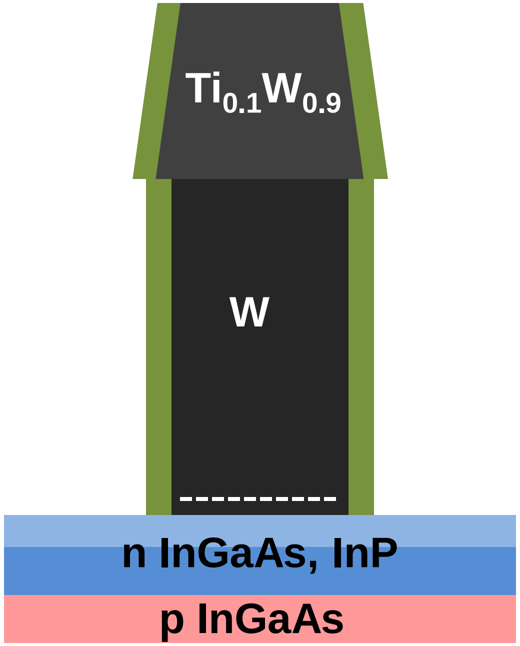
High power
SF_6/Ar ICP etch

Low power
SF_6/Ar ICP etch

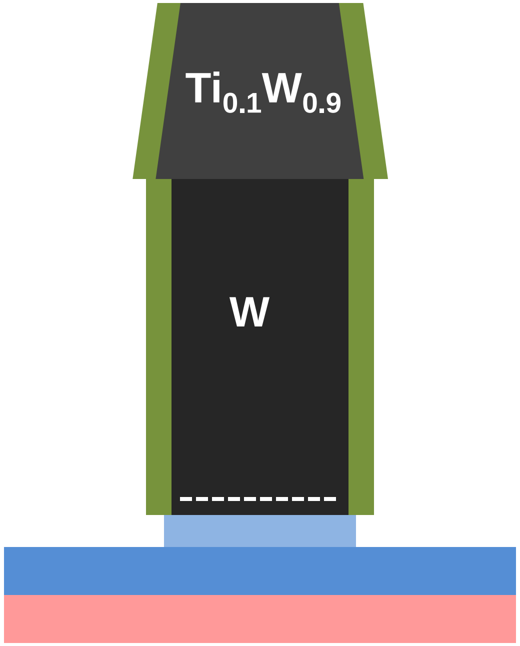


Fabrication: Emitter mesa

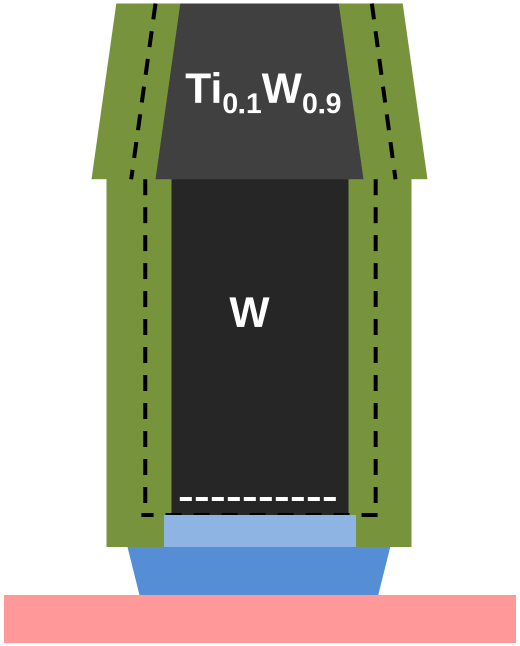
SiN$_x$ PECVD deposition
CF$_4$/O$_2$ ICP etch



InGaAs wet etch



2nd SiN$_x$ sidewall
InP wet etch



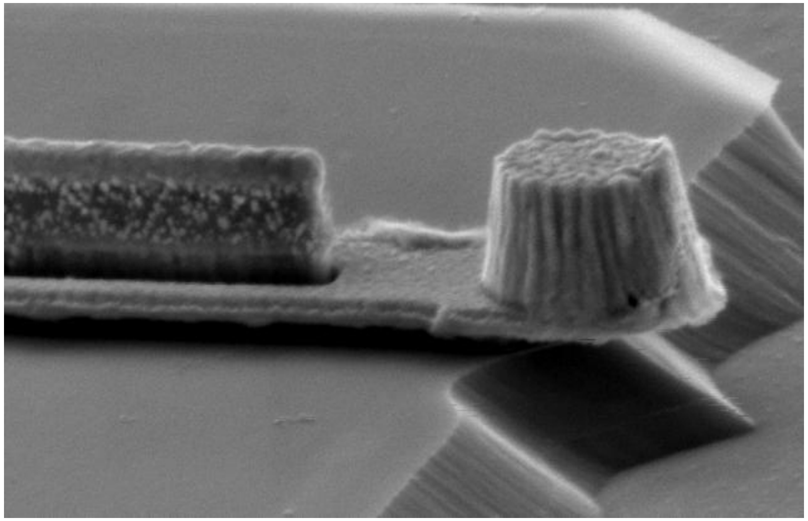
Base Post Cap

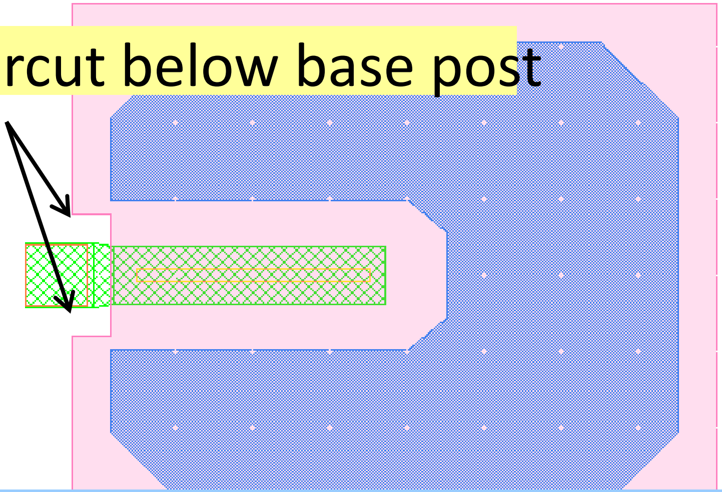
$$C_{cb,post} = \frac{\varepsilon_0 \varepsilon_r \cdot A_{post}}{T_c}$$

$C_{cb,post}$ does not scale with L_e

→ Adversely effects $f_{\max}$ as L_e ↓

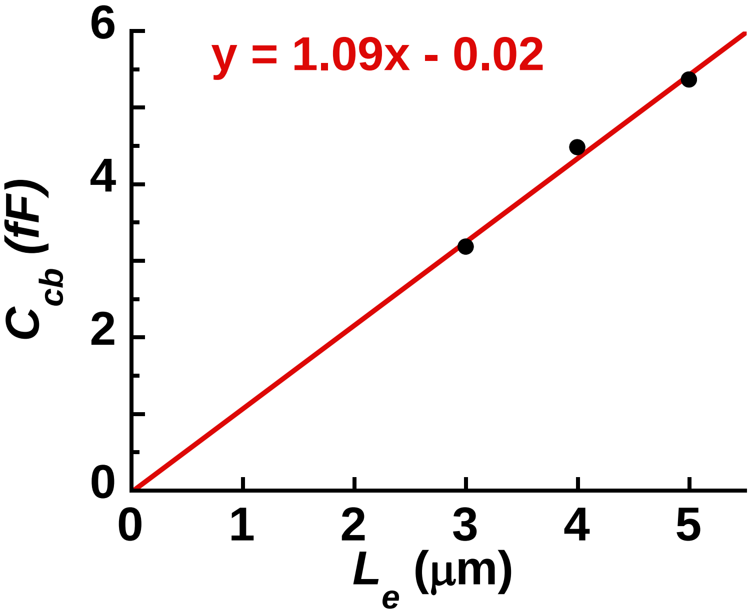
→ Need to minimize the $C_{cb,post}$ value

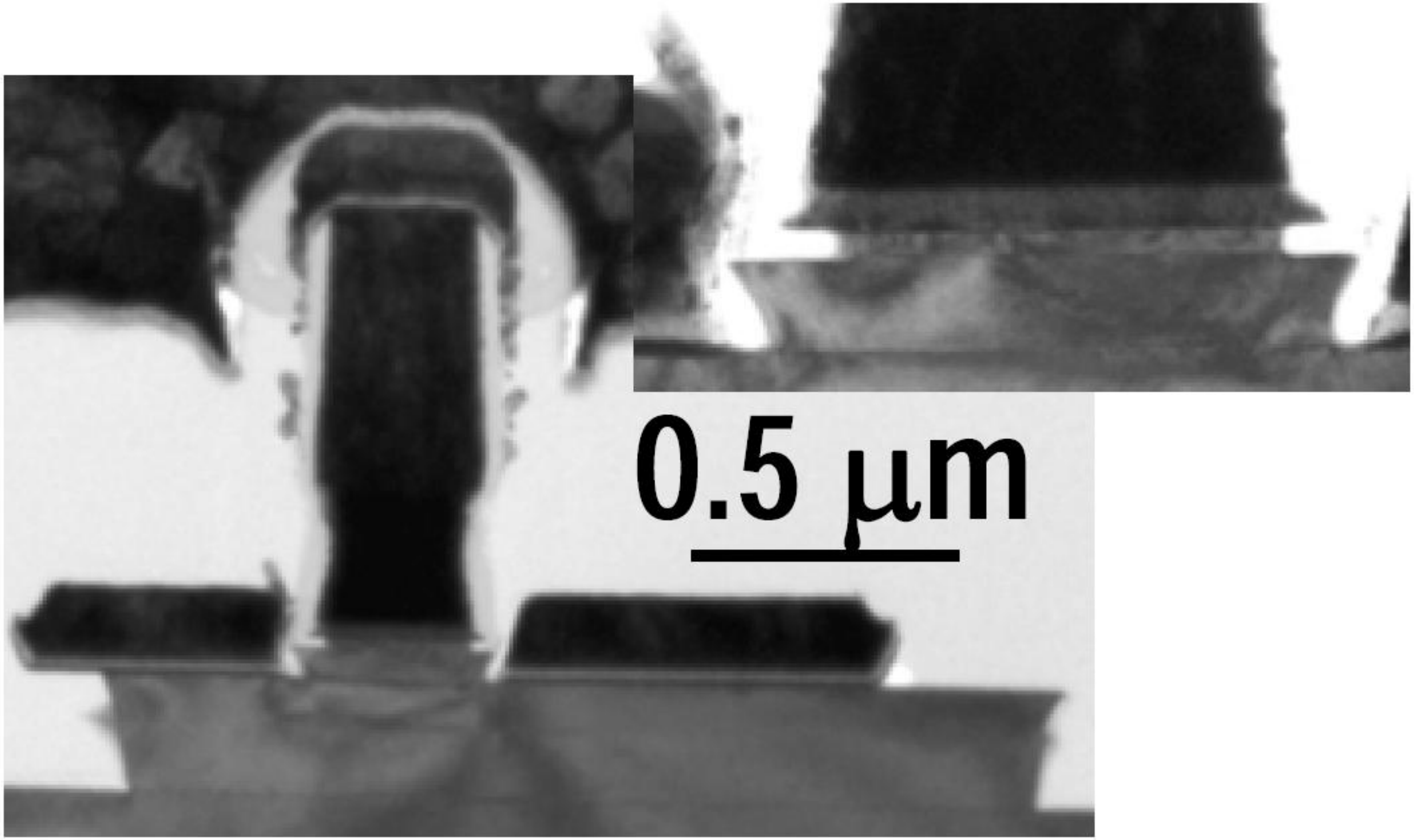




Undercut below base post

No contribution of Base post to C_{cb}



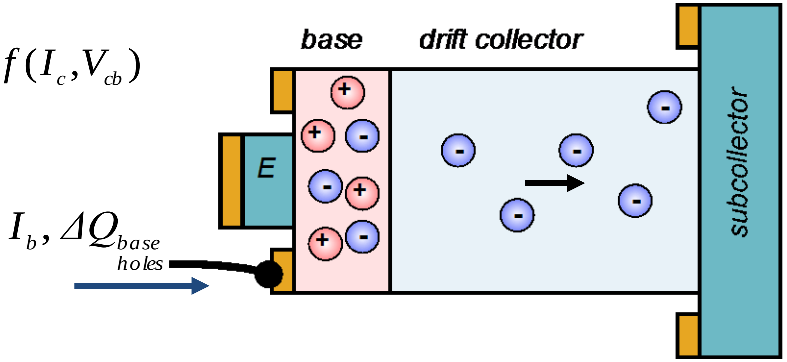

0.5 µm

Transit time Modulation Causes C_{cb} Modulation

$$Q_{\substack{base\\holes}} = \cancel{\text{constant} + Q_{\substack{base\\electrons}} + \int_0^{T_c} qn(x)A(1-x/T_c)dx + V_{bc}\varepsilon A/T_c} = f(I_c, V_{cb})$$

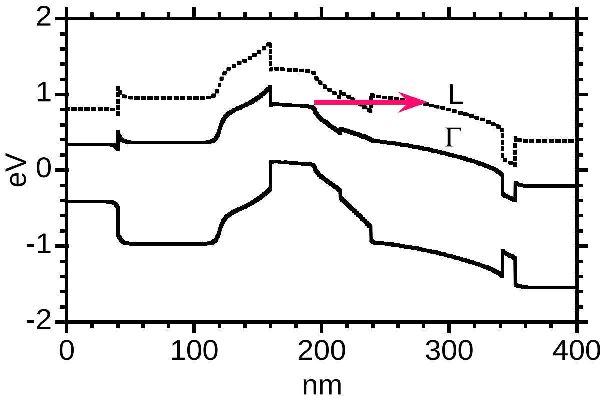
$$C_{cb} \equiv -\frac{\partial Q_{baseholes}}{\partial V_{cb}} \qquad \tau_f \equiv \frac{\partial Q_{baseholes}}{\partial I_c} \Rightarrow \boxed{\frac{\partial C_{cb}}{\partial I_c} = -\frac{\partial \tau_f}{\partial V_{cb}}}$$

Camnitz and Moll, Betser & Ritter, *D. Root*



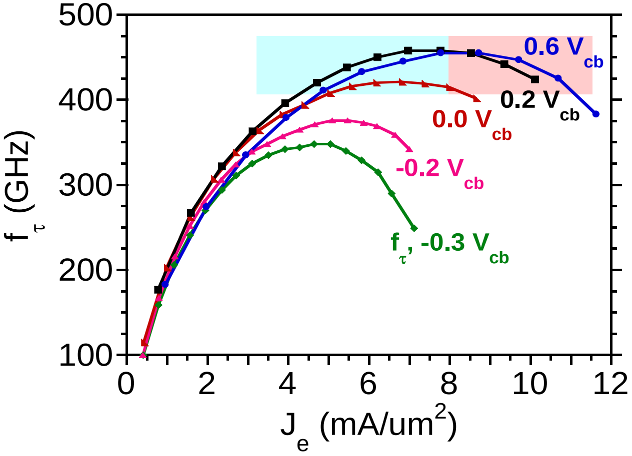
Collector Velocity Modulation:

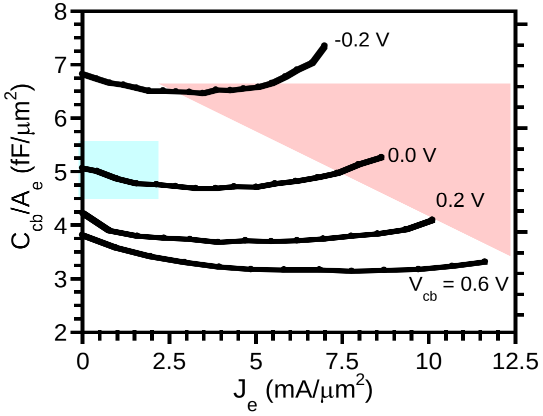
$$\partial \tau_f / \partial V_{cb} > 0 \Rightarrow \partial C_{cb} / \partial I_c < 0$$



Increase in τ_c with $V_{cb} \rightarrow$ reduced C_{cb}

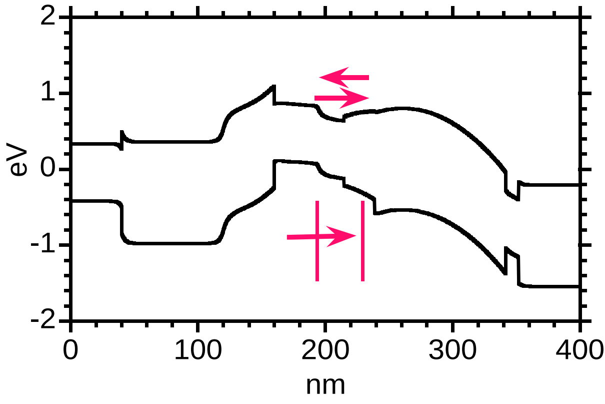
- ***strong effect in InGaAs SHBTs***
- ***weak effect in InP DHBTs***





Kirk Effect:

$$\partial \tau_f / \partial V_{cb} < 0 \Rightarrow \partial C_{cb} / \partial I_c > 0$$



Increase in C_{cb} is due to both

- ***base pushout into collector***
- ***and modulation of τ_b by V_{cb}***