Interface-State Modeling of Al_2O_3–InGaAs MOS From Depletion to Inversion

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***Abstract*—This paper presents a detailed analysis of the multifrequency capacitance–voltage and conductance–voltage data of Al_2O_3/n-InGaAs MOS capacitors. It is shown that the widely varied frequency dependence of the data from depletion to inversion can be fitted to various regional equivalent circuits derived from the full interface-state model. In certain regions, incorporating bulk-oxide traps in the interface-state model enables better fitting of data. By calibrating the model with experimental data, the interface-state density and the trap time constants are extracted as functions of energy in the bandgap, from which the stretch-out of gate voltage is determined. It is concluded that the commonly observed decrease of the 1-kHz capacitance toward stronger inversion is due to the increasing time constant for traps to capture majority carriers at the inverted surface.**

***Index Terms*—Bulk-oxide trap, D_{it}, III–V, interface trap, MOS.**

I. Introduction

A MAJOR task in the development of high-mobility InGaAs MOSFETs is to reduce the interface-state density to a tolerable level. The most common approach to interface-state characterization is to fabricate a MOS capacitor and measure its capacitance–voltage (C–V) and conductance–voltage (G–V) characteristics over a wide range of frequencies. It is often observed that there are "humps" in the low-frequency C–V data of n-type InGaAs and p-type Ge MOS in the weak and strong inversion regions [1]–[6]. An example is shown in Fig. 1.

As pointed out in [7], the conventional "conductance method" for extraction of interface-state density cannot be applied to the weak and strong inversion regions of a MOS device. They proposed a "full conductance method" with a MOSFET-like test structure. By connecting the source and drain regions to the substrate contact, the single-level Y equivalent circuit between the surface, majority carrier contact, and minority carrier contact is reduced to a two-terminal admittance that can be readily integrated for a continuous distribution in trap energy. Fabricating such a structure, however, requires multiple levels of photolithography; thus, it is not economical for a quick and easy evaluation of different dielectrics and surface treatments. More recently [8], interface-state and bulk-oxide trap models are combined to explain the distinct features in different regions of the MOS C–V and G–V characteristics. For the interface-state model, they use a Y circuit in which the capacitance, for a given surface potential, comes solely from the trap density at the Fermi energy. A rigorous treatment of the small-signal interface-state model is to convert the single-energy Y circuit to a Δ circuit then integrate each element with

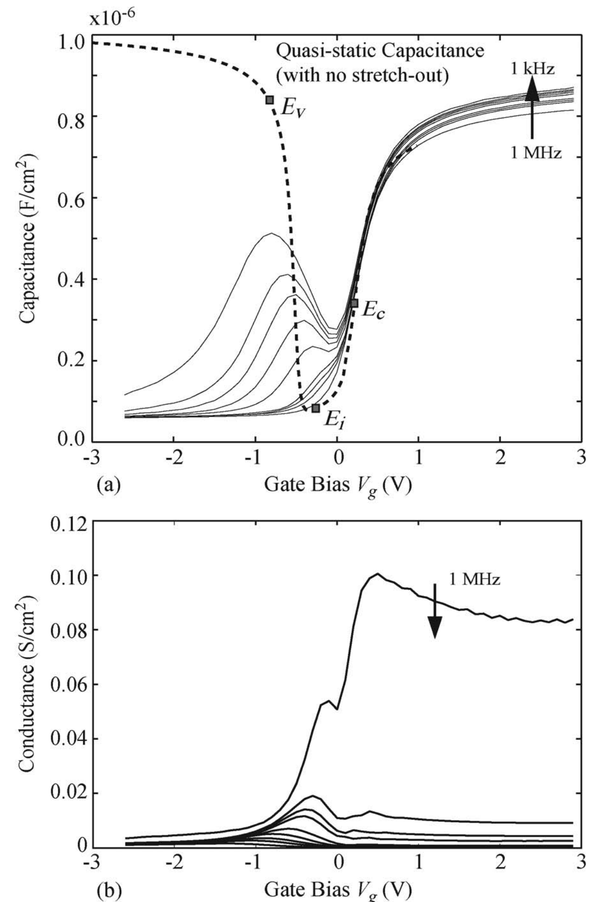

Fig. 1. Experimental (a) C–V and (b) G–V measured at 1 kHz, 2 kHz, 3 kHz, 5 kHz, 10 kHz, 30 kHz, 100 kHz, and 1 MHz. All the data are measured at 300 K, with a small ac signal of 50 mV.

Manuscript received March 5, 2012; revised May 1, 2012 and May 25, 2012; accepted June 15, 2012. Date of publication July 16, 2012; date of current version August 17, 2012. This work was supported in part by the Semiconductor Research Corporation via the Non-classical CMOS Research Center and in part by the Research Collaboration Project with Taiwan Semiconductor Manufacturing Company, Ltd. The review of this paper was arranged by Editor S. Bandyopadhyay.

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Digital Object Identifier 10.1109/TED.2012.2205255

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respect to the trap energy. While the results are more tedious because each element of the Δ circuit becomes a complex frequency-dependent admittance, the full interface-state model is well documented [9].

In this paper, we apply the full interface-state model to analyze the multiple-frequency C–V and G–V data of an Al_2O_3-InGaAs MOS capacitor from depletion to inversion. Detailed step-by-step fitting of both the C–V and G–V data versus frequency enables the extraction of both the interface-state density and the trap time constants as functions of energy. After integrating the dc effect of the interface-state density to obtain the stretch-out of gate voltage in the experimental C–V data, surface potential is determined at every bias point which tells whether strong inversion has been reached. The physical origin of the C–V hump is revealed in the process.

II. Overview of Capacitance and Conductance Data and Modeling Approach

Fig. 1 shows the multiple-frequency C–V and G–V data measured from a Pt/Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOS capacitor. It is fabricated under similar processing procedures as those in [10]. The semiconductor layer structure is 1-μm 2×10^{16} cm^{-3} doped n-$In_{0.53}Ga_{0.47}As$ on 100-nm 5×10^{18} cm^{-3} doped n-$In_{0.53}Ga_{0.47}As$ on n$^+$InP substrate. The Al_2O_3 film is prepared by 50 cycles of atomic layer deposition with trimethyl aluminum precursor and water vapor oxidant. The sample is then annealed in forming gas for 30 min at 400 °C.

Superimposed in Fig. 1(a) is an ideal quasi-static C–V simulated by *Sentaurus* [11] without any traps. The simulation parameters are $C_{\rm ox} = 1.06 \times 10^{-6}$ F/cm^2, $doping\ density = 3.7 \times 10^{16}/\mathrm{cm}^3$, and a gate work function such that the simulated curve crosses over the 1-MHz data at $V_g = 0.2$ V. Labeled on the simulated curve are E_c, E_i, and E_v at gate voltages where the surface potential crosses these energies. It has been shown in [12] and [13] that the dispersions in accumulation, $V_g > 0.2$ V, are due to bulk-oxide traps. The dispersions in depletion and inversion, $V_g < 0.2$ V, i.e., the hump region, however, do not exhibit the same frequency dependence expected of bulk-oxide traps. The low-frequency C–V humps start at $V_g \sim 0.1$ V where the inversion charge capacitance is negligible; hence, they are due to interface states.

In the classic interface-state theory [9], a single-level trap is represented by a Y equivalent circuit consisting of a capacitance C_T and two conductances G_n and G_p connected among the surface, the conduction band, and the valence band. Each of the three elements is proportional to the trap density per unit area and is dependent on the energy of the trap through the Fermi–Dirac distribution function. In practice, there is a continuous distribution of traps as a function of their energy, characterized by $D_{\rm it}$, the interface-state trap density per unit area per unit energy. To integrate the trap contributions for all energies, the Y equivalent circuit must first be converted to a Δ equivalent circuit. The resulting circuit is shown in Fig. 2, where the intrinsic elements are the oxide capacitance $C_{\rm ox}$, the depletion charge capacitance C_d, the inversion charge capacitance C_i, and a conductance G_d representing generation and recombination in the bulk. The C–V data at far negative V_g in Fig. 1(a) show that the inversion capacitance cannot follow the lowest frequency, 1 kHz, indicating that G_d is negligible for our analysis of room-temperature data. This is further discussed in Fig. 11 later.

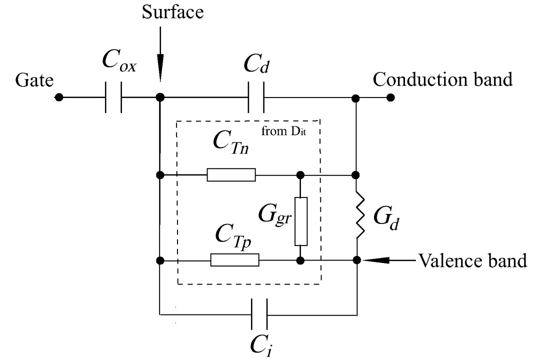

Fig. 2. Equivalent circuit model of MOS (n-type substrate) capacitance with interface state ($D_{\rm it}$) [9].

The interface-state components are C_{Tn}, C_{Tp}, and G_{gr} in Fig. 2. They are given by [9]

$$C_{Tn} = qD_{it}\tau_n^{-1}\int_0^1 df \cdot (1-f) \times \left[j\omega f(1-f) + f\tau_p^{-1} + (1-f)\tau_n^{-1}\right]^{-1} \quad (1)$$

$$C_{Tp} = qD_{\rm it}\tau_p^{-1}\int_0^1 df \cdot f \times \left[j\omega f(1-f) + f\tau_p^{-1} + (1-f)\tau_n^{-1}\right]^{-1} \quad (2)$$

$$G_{gr} = qD_{\rm it}\tau_p^{-1}\tau_n^{-1}\int_0^1 df \cdot \left[j\omega f(1-f) + f\tau_p^{-1} + (1-f)\tau_n^{-1}\right]^{-1} \quad (3)$$

under the assumption that $D_{\rm it}$ varies slowly with energy. Here, f is the Fermi–Dirac distribution function, $\tau_n = (\sigma_n \nu_{\rm th}^n n_s)^{-1}$, and $\tau_p = (\sigma_p \nu_{\rm th}^p p_s)^{-1}$. σ_n and σ_p are the electron and hole capture cross sections of the traps, $\nu_{\rm th}^n$ and $\nu_{\rm th}^p$ are the carrier thermal velocities, and n_s and p_s are the electron and hole densities at the semiconductor surface. Note that, in general, C_{Tn}, C_{Tp}, and G_{gr} are all complex functions of frequency ω. Being in parallel to the bulk generation–recombination conductance, G_{gr} represents generation–recombination via surface states as a stepping stone. At every gate bias or surface potential (ψ_s), the three components are completely specified by parameters $D_{\rm it}$, τ_n, and τ_p, which are chosen in our procedure to fit both the $C_{\rm tot}(\omega)$ and the $G_{\rm tot}(\omega)$ data at that point.

At 100 kHz and 1 MHz, the measured $C_{\rm tot}$ is nearly frequency independent, implying no contribution from the traps. The depletion-charge capacitance C_d is therefore chosen such that the serial combination of $C_{\rm ox}$ and C_d matches the 1-MHz $C_{\rm tot}$ at every gate bias. The inversion charge capacitance C_i is given by the quasi-static C–V simulation (Fig. 1) as a function of ψ_s. To estimate C_i at a given gate voltage V_g, the stretch-out $V_g(\psi_s)$ of the experimental C–V by the dc effect of $D_{\rm it}$ must first be worked out, as described later.

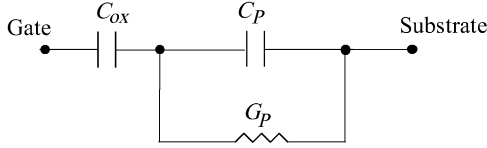

Fig. 3. MOS equivalent circuit by lumping the semiconductor components in Fig. 2 into admittance $G_p + j\omega C_p$.

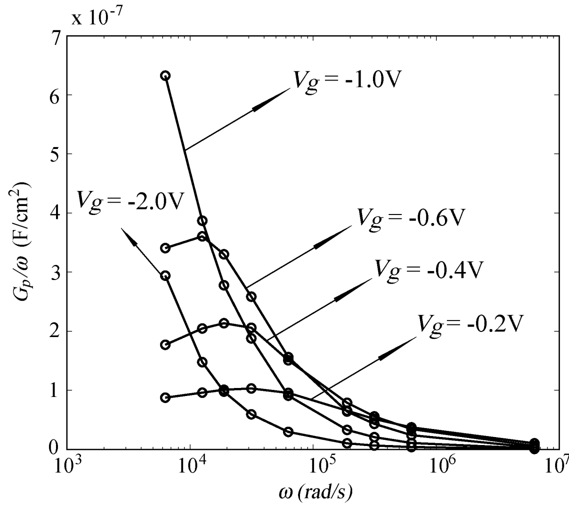

Fig. 4. Extracted G_p/ω data versus ω for different gate biases.

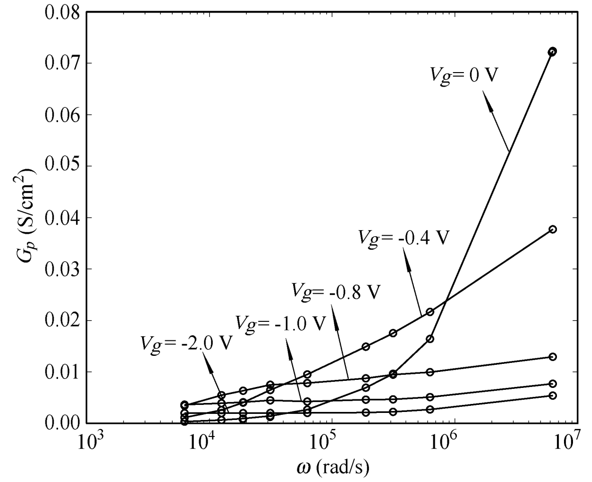

Fig. 5. Extracted G_p data versus ω for different gate biases.

III. Regional Fitting of Data to the Interface-State Model

A numerical program is set up to compute $C_{\text{tot}}(\omega)$ and $G_{\text{tot}}(\omega)$ based on Fig. 2 and (1)–(3). To gain physical insight to the model, it helps to make regional approximations to reduce the model to simple analytical forms. The measured C_{tot} and G_{tot} data are often converted to C_p and G_p defined in Fig. 3 for correlation with analytic models.

A. Depletion Region and Midgap

In the depletion region, $V_g \sim 0$ and $\tau_n \ll \tau_p$, the only significant component from the interface states is C_{Tn}. It is an admittance in parallel with C_d such that [9]

$$C_p = C_d + C_{\text{it}}(\omega\tau_n)^{-1}\tan^{-1}(\omega\tau_n) \quad \text{depletion} \tag{4}$$

$$\frac{G_p}{\omega} = C_{\text{it}}(2\omega\tau_n)^{-1}\ln\left[1 + (\omega\tau_n)^2\right] \quad \text{depletion.} \tag{5}$$

Here, $C_{\text{it}} \equiv qD_{\text{it}}$ (with D_{it} in units of $\text{cm}^{-2}\cdot\text{eV}^{-1}$) is the interface-state capacitance. This is the well-known "conductance method," in which D_{it} is extracted by plotting G_p/ω versus ω and reading the peak, $0.4C_{\text{it}}$ at $\omega\tau_n = 1.98$. Fig. 4 shows the G_p/ω versus ω plots for several V_g biases de-embedded from the $C_{\text{tot}}(\omega)$ and $G_{\text{tot}}(\omega)$ data using $C_{\text{ox}} = 1.06 \times 10^{-6}$ F/cm^2. At $V_g = -0.2$ V, a D_{it} of $2.1 \times 10^{12}\ \text{cm}^{-2}\cdot\text{eV}^{-1}$ and τ_n of 2.8×10^{-5} s are extracted from fitting of the C_{tot} and G_{tot} dispersion data. As V_g becomes more negative, both D_{it} and τ_n increase. The latter is due to further depletion of the electron density at the surface. For V_g more negative than -0.6 V, the G_p/ω peak shifts to a frequency below 1 kHz.

A particular bias point in depletion occurs when $\tau_n = \tau_p = \tau$, close to the midgap position where $n_s = p_s$. For most of the frequency range, $\omega\tau > 1$, and (5) can be approximated as [9]

$$G_p = \frac{C_{\text{it}}}{\tau}\ln(\omega\tau) \quad \text{midgap.} \tag{6}$$

By plotting G_p versus $\ln(\omega)$ for a wide range of V_g in Fig. 5, it is determined that the midgap position is reached near $V_g = -0.4$ V where $\tau_n \approx \tau_p \approx 10^{-4}$ s and $D_{\text{it}} \approx 3.9 \times 10^{12}\ \text{cm}^{-2}\cdot\text{eV}^{-1}$.

B. Weak Inversion Region

In the weak inversion region $(-1.0\ \text{V} \le V_g \le -0.4\ \text{V})$, $\tau_p < \tau_n$. While $\omega\tau_n > 1$ for the entire frequency range, $\omega\tau_p > 1$ at 1 MHz, but $\omega\tau_p < 1$ at 1 kHz. There is no single analytic circuit valid for the entire range. At high frequencies, $\omega C_{Tp} \ge G_{gr}$, the interface-state admittance can be considered as $j\omega C_{Tn}$ in parallel with G_{gr}, with $j\omega C_{Tn}$ dominating. It has been shown to yield [9]

$$C_p = C_d + \frac{\tau_p}{\tau_n}C_{\text{it}} \times (\omega\tau_p)^{-1}\tan^{-1}(\omega\tau_p) \quad \text{weak inversion}, \omega\tau_p > 1 \tag{7}$$

$$G_p = \frac{C_{\text{it}}}{2\tau_n}\ln \times \left[\left(\frac{\tau_n}{\tau_p}\right)^2 + (\omega\tau_n)^2\right] \quad \text{weak inversion}, \omega\tau_p > 1 \tag{8}$$

for the components defined in Fig. 3. At low frequencies, the interface-state contribution is dominated by $j\omega C_{Tp}$ in series with G_{gr} (C_i is negligible in weak inversion), but $j\omega C_{Tn}$ is not completely negligible. For $\omega\tau_p \ll 1$, $C_{Tp} \approx C_{\text{it}}$, and $G_{gr} \approx (C_{\text{it}}/\tau_n)\ln(\tau_n/\tau_p)$. The equivalent circuit and C_p and G_p expressions are similar to the strong inversion case hereinafter.

At $V_g = -0.8$ V near the peak of the hump, parameters C_{it}, τ_n, and τ_p are chosen to fit both the $C_{\text{tot}}(\omega)$ and $G_{\text{tot}}(\omega)$ data (Fig. 6) using the full numerical program.

C. Strong Inversion Region

In strong inversion, $V_g < -1$ V, $\tau_p \ll \tau_n$, and C_{Tn} is negligible. Also, $C_{Tp} \approx C_{\text{it}}$, and C_i becomes appreciable. The equivalent circuit is shown in Fig. 7, where

$$G_{gr} = \frac{C_{\text{it}}}{\tau_n}\ln\left(\frac{\tau_n}{\tau_p}\right) \quad \text{strong inversion.} \tag{9}$$

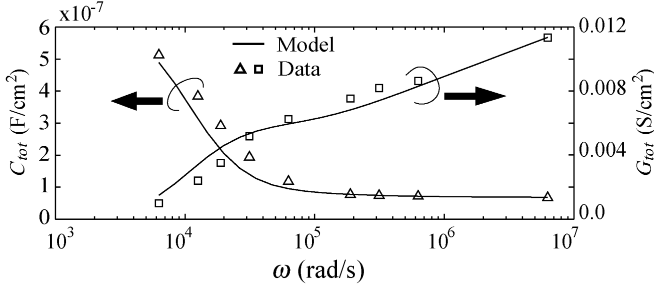

Fig. 6. Model fitting of C and G data at $V_g = -0.8$ V. Model parameters are $C_{\rm it} = 1.312 \times 10^{-6}$ F/cm^2, $C_i = 1.45 \times 10^{-7}$ F/cm^2, $C_d = 7.3 \times 10^{-8}$ F/cm^2, $\tau_n = 8.7 \times 10^{-4}$ s, and $\tau_p = 1.1 \times 10^{-5}$ s.

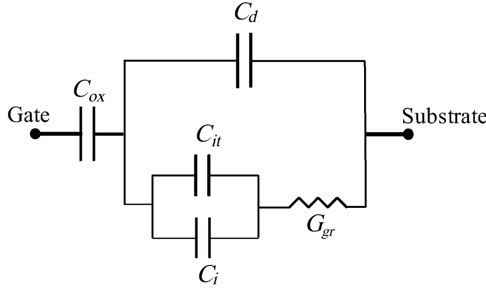

Fig. 7. Simplified MOS equivalent circuit in strong inversion.

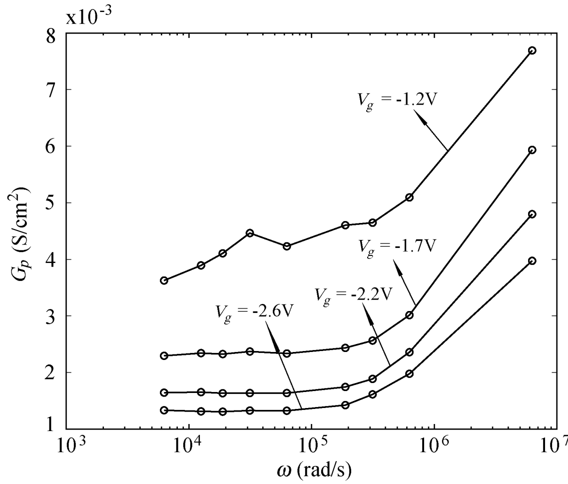

Fig. 8. Extracted G_p data versus ω for different gate biases in inversion.

For this circuit, C_p and G_p are

$$C_p = \frac{(C_i + C_{\rm it})G_{gr}^2}{\omega^2(C_i + C_{\rm it})^2 + G_{gr}^2} + C_d \quad \text{strong inversion} \tag{10}$$

$$G_p = \frac{\omega^2(C_i + C_{\rm it})^2 G_{gr}}{\omega^2(C_i + C_{\rm it})^2 + G_{gr}^2} \quad \text{strong inversion.} \tag{11}$$

Fig. 8 plots the $G_p(\omega)$ data for several V_g biases in strong inversion. For frequencies in the low kilohertz range, G_p is independent of frequency, implying that $\omega(C_i + C_{\rm it}) \geq G_{gr}$, and $G_p = G_{gr} = (C_{\rm it}/\tau_n)\ln(\tau_n/\tau_p)$. G_p or G_{gr} decreases as V_g becomes more negative. This is a reflection of the longer τ_n as the MOS is biased into stronger inversion. Physically, the surface electron density in the conduction band becomes so low that it takes much longer for a trap to capture an electron. The increase of G_p toward 1 MHz cannot be explained by the interface-state model alone. It will be addressed in a later section.

Under the aforementioned condition, $\omega(C_i + C_{\rm it}) \geq G_{gr}$, the interface-state contribution to C_p in (10) is $(G_{gr}/\omega)^2/(C_i + C_{\rm it})$, inversely proportional to $C_i + C_{\rm it}$. It is counterintuitive that, in this regime, C_p actually goes down as the inversion capacitance C_i goes up. The combination of decreasing G_{gr} and increasing C_i accounts for the observed drop of the 1-kHz $C_{\rm tot}$ beyond the peak of the hump. Note that the drop of $C_{\rm tot}$ does not imply that $C_{\rm it}$ (or $D_{\rm it}$) is decreasing toward more negative V_g.

IV. Overall Model Fitting With Gate Voltage Stretch-Out

From the quasi-static simulation [Fig. 1(a)], the intrinsic capacitance C_i can be extracted as a function of surface potential ψ_s. To apply it to the model for a given V_g, ψ_s needs to be determined, taking the stretch-out of V_g by the dc effect of $D_{\rm it}$ into account. The starting point is $V_g = 0.2$ V where the surface potential is obtained by matching the measured 1-MHz capacitance to the simulated capacitance. As V_g goes negative, the incremental stretch-out is calculated by

$$\Delta V_g = \Delta\psi_s \times \left(\frac{C_{\rm ox} + C_{\rm it} + C_i + C_d}{C_{\rm ox}}\right) \tag{12}$$

point by point, where $C_{\rm it}$ is the interface-state capacitance extracted from the dispersion at that point. In other words, the increment of surface potential of the next bias point is calculated from the ΔV_g step using the aforementioned equation. A $\psi_s{-}V_g$ relation with stretch-out is then generated by integrating the $C_{\rm it}$ contributions of all previous bias points.

The extraction results of $D_{\rm it}$, τ_n, and τ_p for the range of -2.6 V $\leq V_g \leq 0.2$ V are summarized in Fig. 9 versus ψ_s. $D_{\rm it}$ rises from $\sim 10^{12}$ cm$^{-2} \cdot$ eV^{-1} near the flatband to $\sim 10^{13}$ cm$^{-2} \cdot$ eV^{-1} into the valence band. Its value on the far left of the range is estimated since only the ratio $C_{\rm it}/\tau_n$ can be accurately determined from the G_{gr} data. $D_{\rm it}$ varies slowly on the scale of kT/q, justifying the earlier assumption. τ_n and τ_p exhibit the expected trend reflecting several-orders-of-magnitude change in the electron and hole densities at the surface. While they by and large vary exponentially with ψ_s, the slopes are much slower than $\exp(\pm q\psi_s/kT)$.

The overall fitting of the multiple-frequency $C_{\rm tot}$–V_g and $G_{\rm tot}$–V_g data by the full interface-state model with the extracted parameters of Fig. 9 is shown in Fig. 10. Also plotted in Fig. 10(a) is the inversion layer capacitance C_i based on the stretched out ψ_s–V_g relation mentioned earlier. Beyond the peak of the hump toward more negative V_g, the 1-kHz $C_{\rm tot}$ decreases, while C_i increases sharply and $C_{\rm it}$ stays more or less flat. The fall of the $C_{\rm tot}$ is attributed to the increasing τ_n, as stated before. It is informative to use the model to find out how the C–V changes from the high-frequency to the low-frequency or quasi-static characteristics, either by intrinsic generation and recombination in the bulk or by interface states. Consider the strong inversion circuit in Fig. 7 with $C_i > C_{\rm ox} > C_d$. In the high-frequency limit, $\omega C_d \geq G_{gr}$, $C_{\rm tot}$ equals $C_{\rm ox}$ in series with C_d. In the low-frequency limit, $\omega C_i \ll G_{gr}$, $C_{\rm tot} \approx C_{\rm ox}$. For intermediate frequencies, $G_{gr}/C_i \ll \omega \ll G_{gr}/C_d$, $C_{\rm tot}$ is

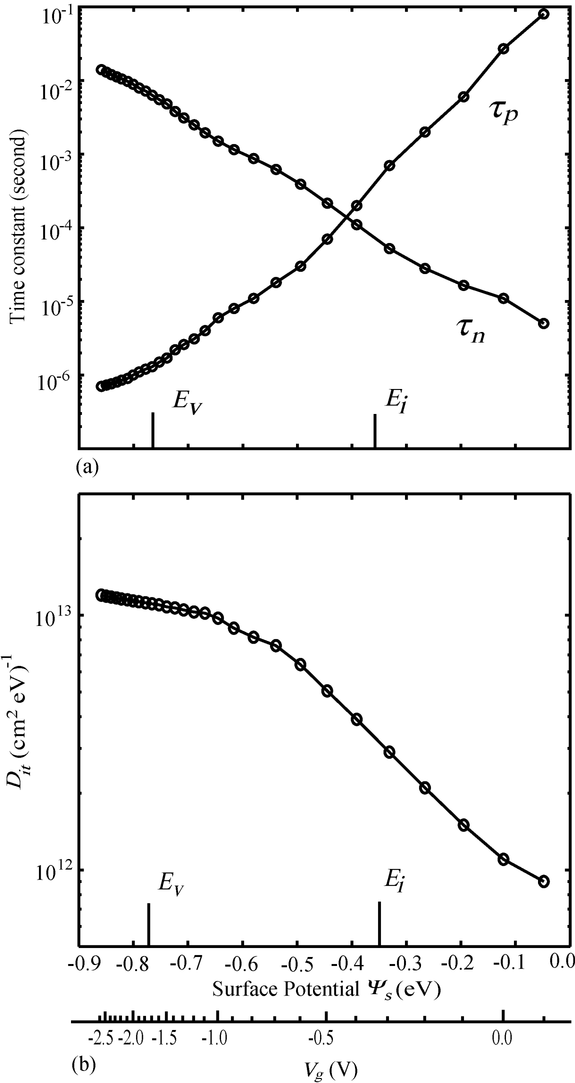

Fig. 9. (a) Extracted τ_n and τ_p versus (bottom x-axis) surface potential ψ_s and V_g. (b) Extracted interface-state density $(D_{\rm it})$ versus (bottom x-axis) surface potential ψ_s and V_g.

approximately the capacitive component of the serial combination of $C_{\rm ox}$ and G_{gr}, i.e.,

$$C_{\rm tot} = \frac{C_{\rm ox} G_{gr}^2}{\omega^2 C_{\rm ox}^2 + G_{gr}^2}. \quad (13)$$

Fig. 11 shows two sets of model-generated $C_{\rm tot}$–V_g plots in the intermediate-frequency range. The solid curves use the $D_{\rm it}$ parameters in Fig. 9 and extend the frequency to below 1 kHz. The dashed curves are for an intrinsic MOS with $C_{\rm it} = 0$ but at elevated temperature, for which we assume a constant $G_d = 0.002$ S/cm^2 replacing G_{gr} in Fig. 7. Basically, the slope of the $C_{\rm tot}$–V_g curves reflects the dependence of G_{gr} or G_d on V_g. The conductance G_d from generation and recombination in the bulk is independent of V_g; hence, the intrinsic $C_{\rm tot}$–V_g curves (dashed) are flat. Examples of such characteristics can be found in the literature [5]. On the other hand, $C_{\rm tot}$ of the $D_{\rm it}$ case (solid) decreases toward stronger inversion because G_{gr} decreases in that direction. A positive- then negative-going slope of $C_{\rm tot}$–V_g characteristics in inversion is thus a telltale sign of interface states. At elevated temperatures, G_d increases sharply, and full inversion capacitance is observed above 1 kHz [6].

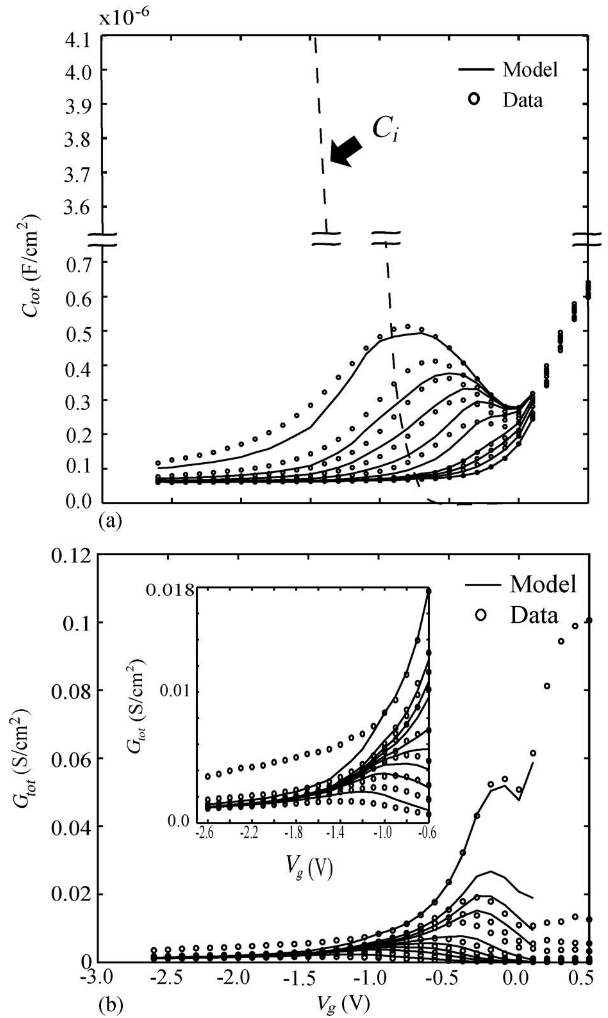

Fig. 10. Overall model fitting of experimental (a) $C_{\rm tot}$–V_g and (b) $G_{\rm tot}$–V_g data.

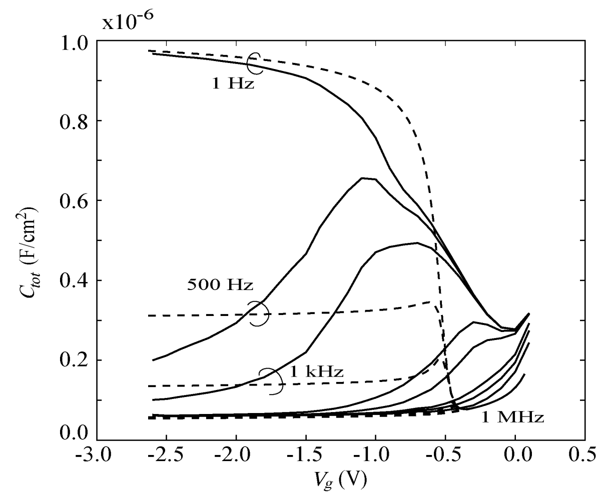

Fig. 11. Model extension of C–V to low frequencies. Solid curves assume $G_d = 0$ and use the τ_n, τ_p, and $D_{\rm it}$ parameters in Fig. 9. Dashed curves assume $D_{\rm it} = 0$ and $G_d = 0.002$ S/cm^2.

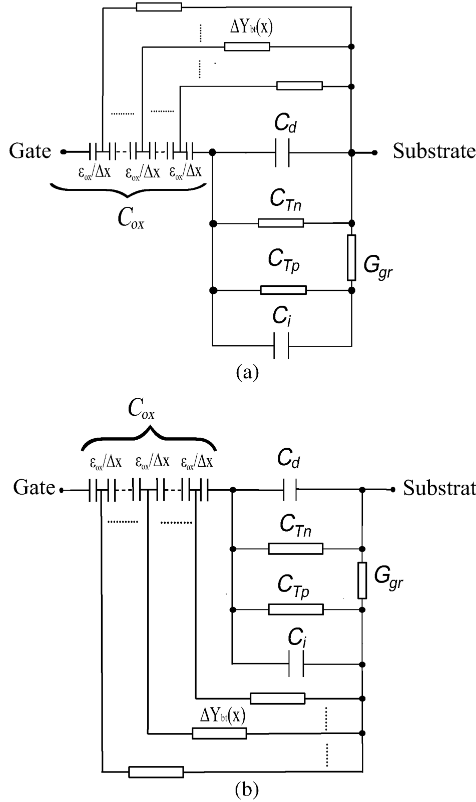

Fig. 12. Equivalent circuits with (a) the bulk-oxide electron trap full interface-state model and (b) the bulk-oxide hole trap full interface-state model.

V. Refinement of Fitting by Incorporating Bulk-Oxide Traps

While the C_{tot}–V_g and G_{tot}–V_g data for most of the $-2.6\ \mathrm{V} \leq V_g \leq 0.2\ \mathrm{V}$ range are fitted rather well by the interface-state model, the fitting at either end of the range can be further improved by incorporating bulk-oxide traps in the interface-state model. Low-frequency C_{tot} near $V_g = 0.2$ V fits better by adding electron bulk-oxide traps, and high-frequency G_{tot} near $V_g = -2.6$ V fits better by adding hole bulk-oxide traps.

The combined bulk-oxide trap [12], [13] and interface-state equivalent circuits are shown in Fig. 12. The distributed electron traps in the bulk oxide are connected to the n-type substrate in Fig. 12(a). The distributed hole traps in the bulk oxide are connected through G_{gr}, along with C_i in Fig. 12(b). The incremental trap elements are [13]

$$\Delta Y_{bt} = \frac{q^2 N_{bt} \ln(1 + j\omega\tau_n e^{2\kappa x})}{\tau_n e^{2\kappa x}} \Delta x \tag{14}$$

where N_{bt} is the bulk-oxide trap density per unit volume and κ is the attenuation coefficient for electron tunneling. Similar expression applies for hole bulk-oxide traps by replacing τ_n with τ_p and by replacing the electron barrier height with the hole barrier height in the attenuation coefficient κ. The distributed circuit in Fig. 12(a) can be solved numerically by alternating serial and parallel combinations. The circuit in Fig. 12(b) can be solved numerically by successive Δ-to-Y impedance transformations.

The solid curves in Fig. 13 are fittings of the C_{tot} and G_{tot} data at $V_g = 0$ with only the interface-state model. The D_{it}

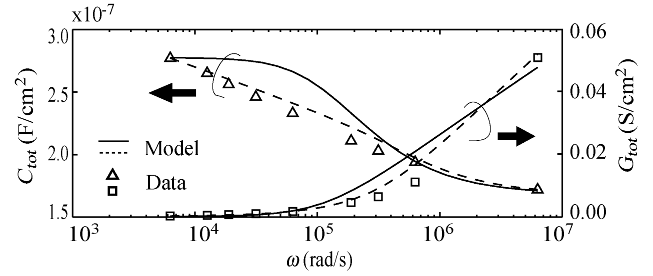

Fig. 13. C_{tot} and G_{tot} fittings at $V_g = 0$ V with and without bulk-oxide electron traps. For solid lines without bulk-oxide traps, $C_{\mathrm{it}} = 1.76 \times 10^{-7}$ F/cm^2, $C_i = 9.00 \times 10^{-15}$ F/cm^2, $C_d = 2.0 \times 10^{-7}$ F/cm^2, $\tau_n = 1.1 \times 10^{-5}$ s, and $\tau_p = 2.7 \times 10^{-2}$ s. For dashed lines with bulk-oxide traps, $C_{\mathrm{it}} = 4.00 \times 10^{-8}$ F/cm^2, $C_i = 9.30 \times 10^{-15}$ F/cm^2, $C_d = 2.0 \times 10^{-7}$ F/cm^2, $\tau_n = 3.0 \times 10^{-6}$ s, $\tau_p = 2.7 \times 10^{-2}$ s, $N_{bt} = 2 \times 10^{19}$ cm^{-3}, and $\kappa = 6.4 \times 10^7$ cm^{-1}.

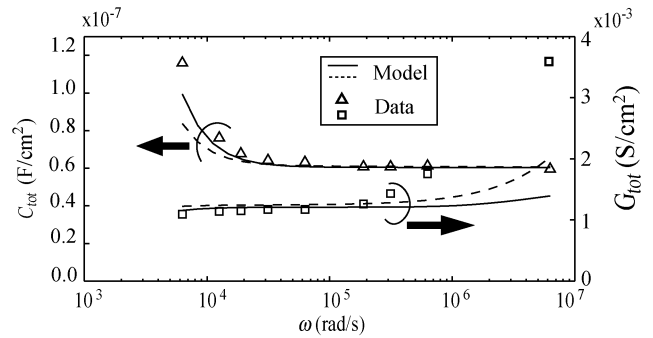

Fig. 14. C_{tot} and G_{tot} fittings at $V_g = -2.6$ V with and without bulk-oxide hole traps. For solid lines without bulk-oxide traps, $C_{\mathrm{it}} = 1.92 \times 10^{-6}$ F/cm^2, $C_i = 8.80 \times 10^{-6}$ F/cm^2, $C_d = 6.4 \times 10^{-8}$ F/cm^2, $\tau_n = 1.4 \times 10^{-2}$ s, and $\tau_p = 7.0 \times 10^{-7}$ s. For dashed lines with bulk-oxide traps, $C_{\mathrm{it}} = 1.92 \times 10^{-6}$ F/cm^2, $C_i = 4.50 \times 10^{-6}$ F/cm^2, $C_d = 6.4 \times 10^{-8}$ F/cm^2, $\tau_n = 2.8 \times 10^{-2}$ s, $\tau_p = 1.0 \times 10^{-10}$ s, $N_{bt} = 5 \times 10^{20}$ cm^{-3}, and $\kappa = 3.0 \times 10^7$ cm^{-1}.

was chosen for the model to match the 1-kHz C_{tot}, which left significant discrepancies with the next few points. By incorporating electron bulk-oxide traps in the interface-state model, much improved fitting is achieved for the entire frequency range (dashed curves). As noted in the caption, a D_{it} lower than that of the interface-state-only model is used in the combined model. As V_g becomes more negative, D_{it} increases, while the contribution from bulk-oxide traps diminishes due to increasing τ_n. The data can be well fitted with interface states only.

The discrepancy of G_{tot} (1 MHz) from the D_{it}-only model at large negative V_g [inset of Fig. 10(b)] is much more difficult to explain. Fig. 14 shows that inclusion of bulk-oxide hole traps in the interface-state model [Fig. 12(b)] tends to move G_{tot} (1 MHz) up in the right direction. However, to fully account for the observed data, unreasonably low valence band barrier and high hole trap density would have to be assumed in the model.

VI. Conclusion

The full interface-state model with a Δ circuit of three complex elements has been applied to the MOS data of an Al_2O_3–InGaAs capacitor from depletion to inversion. Both the C–V and G–V multiple-frequency data are in detailed agreement with the model, allowing the extraction of interface-state density and trap time constants as functions of the surface potential. It is revealed that the rise of the low-frequency C–V

humps in depletion is due to the increasing $D_{\rm it}$, while the fall of the humps in inversion is due to the increased time constant for electron capture.

Furthermore, it is also shown that some regions of the C–V and G–V data can be better fitted by incorporating distributed bulk-oxide traps in the full interface-state model.

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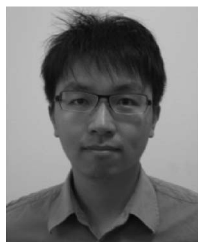

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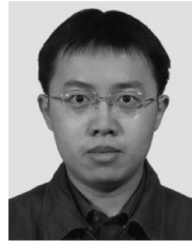

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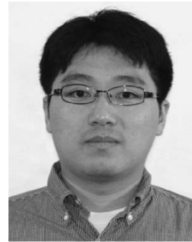

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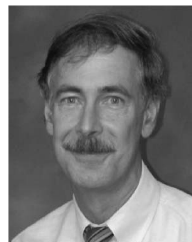

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