

Co-Doping of $\text{In}_x\text{Ga}_{1-x}\text{As}$ with Si and Te for Ultra-Low Contact Resistance

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Introduction

- III-V transistors are being developed for use in large scale integrated circuits¹
- Scaling requirements dictate that as device areas scale by 1:2, absolute resistance must remain constant, requiring a 1:2 decrease in resistivities
- ~ 9 nm L_g MOSFETs would need access resistivities of less than $10 \text{ } \Omega/\text{mm}$ to suffer a 10 % degradation in performance²
- HBTs and optoelectronic devices also require lower parasitic resistivities in order to operate at increasing frequency³
- MBE can be used to make low-resistance, highly doped ohmic contact to InGaAs⁴
- We show that we can dope $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ with Te from $2 \cdot 10^{17}$ to $2.6 \cdot 10^{19} \text{ cm}^{-3}$
- We show that in incorporation of Te as a co-dopant lowers semiconductor sheet resistance and metal-semiconductor contact resistance in regrown $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and InAs
- Te likely acts as a surfactant⁵ which improves material quality

Experiment

Hall Samples

- Samples were growth by solid source MBE lattice matched to (100) semi-insulating InP
- Hall Samples:
 - 500 nm n^+ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ Si doped (Figure 1 (a)), Te doped (Figure 1 (b)), and Si and Te co-doped (Figure 1 (c)); 150 nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$; S. I. InP substrate
 - Top 500 nm grown at 400 °C
- Indium dots were manually places on the sample surface
- Hall measurement by Van der Pauw technique

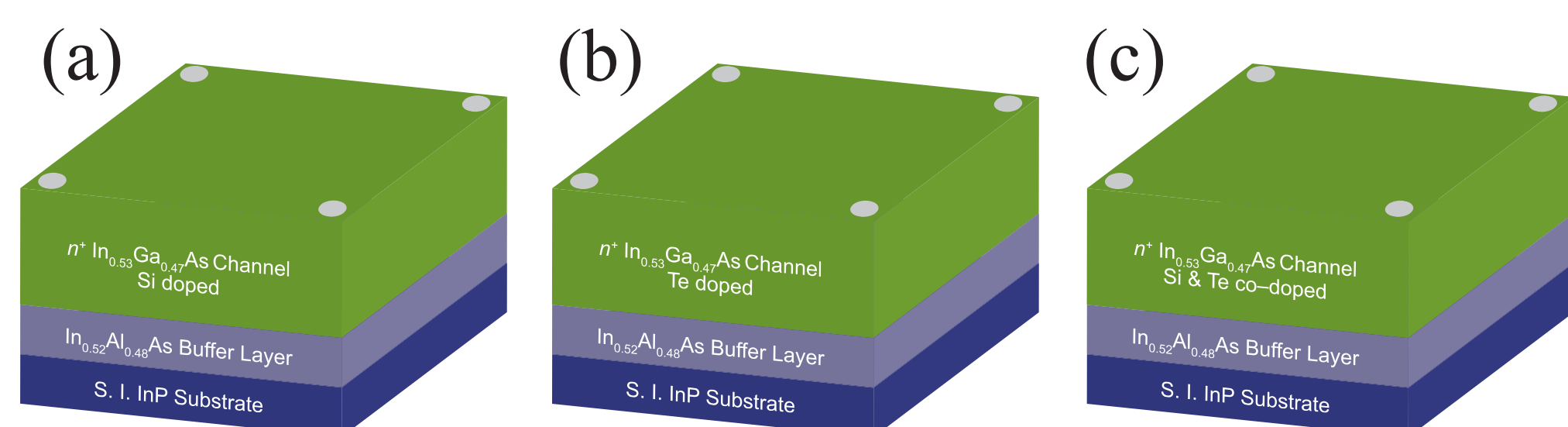


Figure 1: Illustration of Hall sample structures used to measure sheet resistance, carrier concentration, and mobility of (a) Si doped, (b) Te doped, and (c) Si & Te co-doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$.

TLM Samples

- Samples were growth by solid source MBE lattice matched to (100) semi-insulating InP
- TLM Samples:
 - Figure 2 (a): 60 nm n^+ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ Si doped or Si + Te co-doped; 7 nm $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, 3 nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ Si doped $1.3 \cdot 10^{19} \text{ cm}^{-3}$; 400 nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$; S. I. InP substrate
 - Figure 2 (b): 60 nm n^+ InAs Si doped or Si + Te co-doped; 10 nm $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, 3 nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ Si doped $1.3 \cdot 10^{19} \text{ cm}^{-3}$; 400 nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$; S. I. InP substrate
 - Top 60 nm of n^+ material was regrown via a quasi-migration-enhance-epitaxy technique (MEE)⁶ on air exposed samples.
- Sample cleaning prior to regrowth
 - UV Ozone and 10 H_2O : 1 HCl dipv
 - Hydrogen cleaning ($1.0 \cdot 10^{-6}$ Torr partial pressure) at 420 °C for 40 minutes
- TLM samples were mesa isolation and Ti/Pd/Au metalized, Figure 2 (a) and (b)

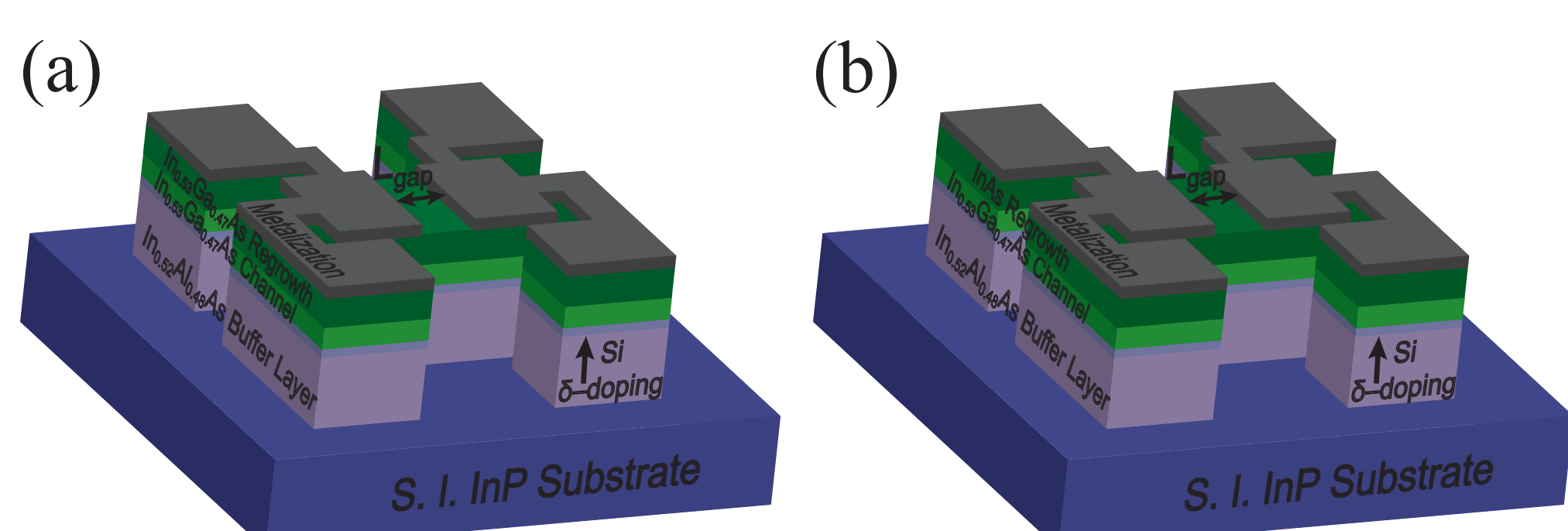


Figure 2: Illustration of TLM sample structures used to measure sheet resistance and contact resistance of (a) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, and mobility of (a) Si doped, (b) Te doped, and (c) Si & Te co-doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$.

Results

Hall Measurement

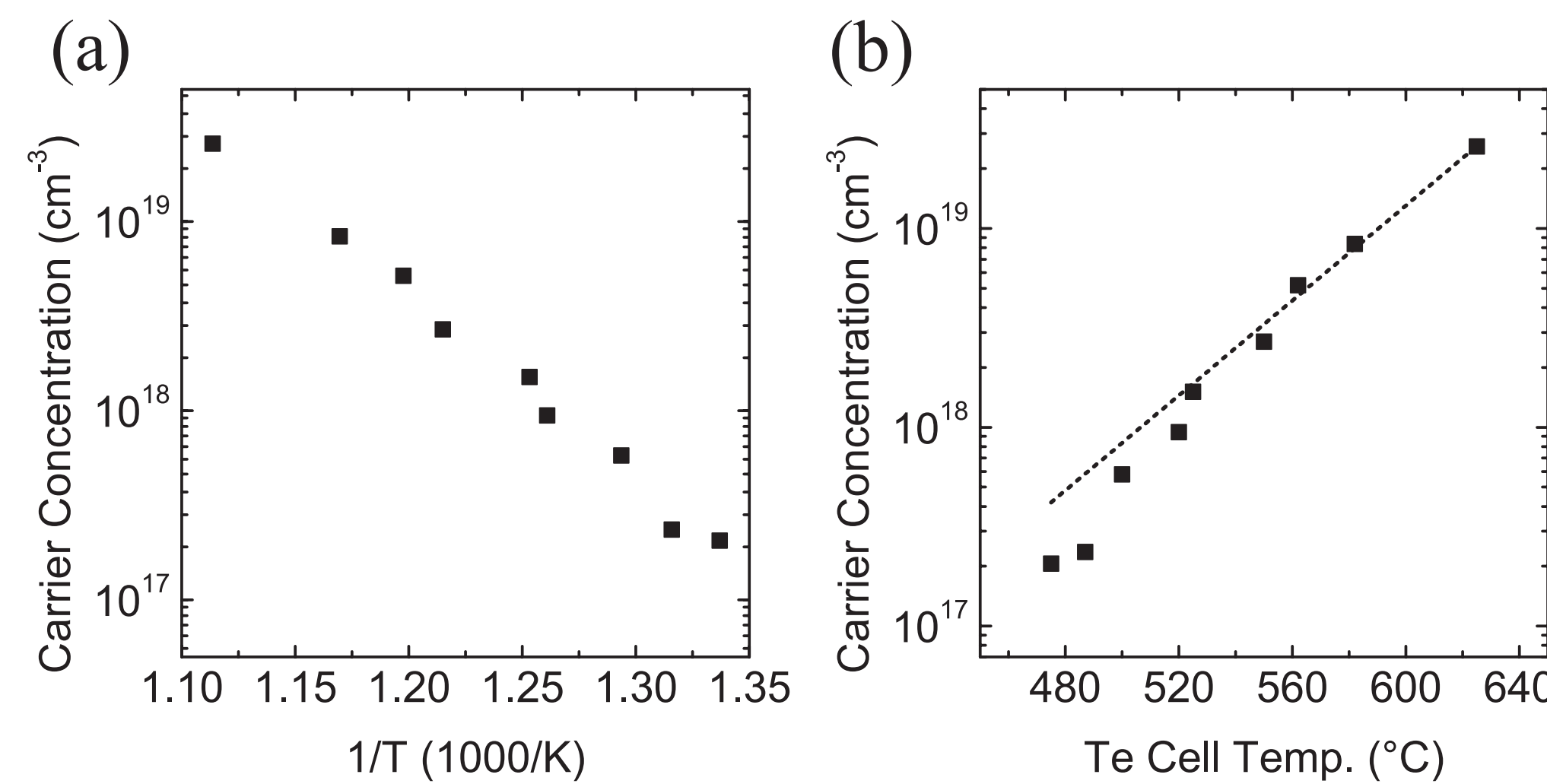


Figure 3: (a) Arrhenius plot of inverse GaTe cell temperature (abscissa) versus active carrier concentration (ordinate) and (b) GaTe cell temperature versus active carrier concentration with exponential fit (linear on log scale) of Te doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$.

- Hall measurement showed exponential dependence of active electron concentration on GaTe cell temperatures from 475 °C ($2.1 \cdot 10^{17} \text{ cm}^{-3}$) to 625 °C ($2.6 \cdot 10^{19} \text{ cm}^{-3}$)
- No saturation effects evident in log plot of GaTe cell temperature versus active electron concentration
- Further experiments under way to determine saturated electron concentration at higher GaTe cell temperatures

	Si doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	Te doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	Si & Te co-doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$
$R_{SH} (\Omega)$	3.65	3.62	2.95
$\mu (\text{cm}^2/\text{V}\cdot\text{s})$	780	1601	1111
$n_d (\text{cm}^{-3})$	$4.39 \cdot 10^{19}$	$2.16 \cdot 10^{19}$	$3.81 \cdot 10^{19}$

Table 1: Summary of Hall measurements taken on Si doped, Te doped, and Si and Te co-doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$.

- Si cell temperature of 1392 °C, Te cell temperature of 625 °C
- Lowest sheet resistance from Si and Te co-doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$
- Incorporation of Te with Si lowers overall active carrier concentration but increases mobility when compared to Si only
- Improved material quality by incorporating Te
- Te could act as a surfactant⁵ helping to improve material quality of heavily Si doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$

Atomic Force Microscopy

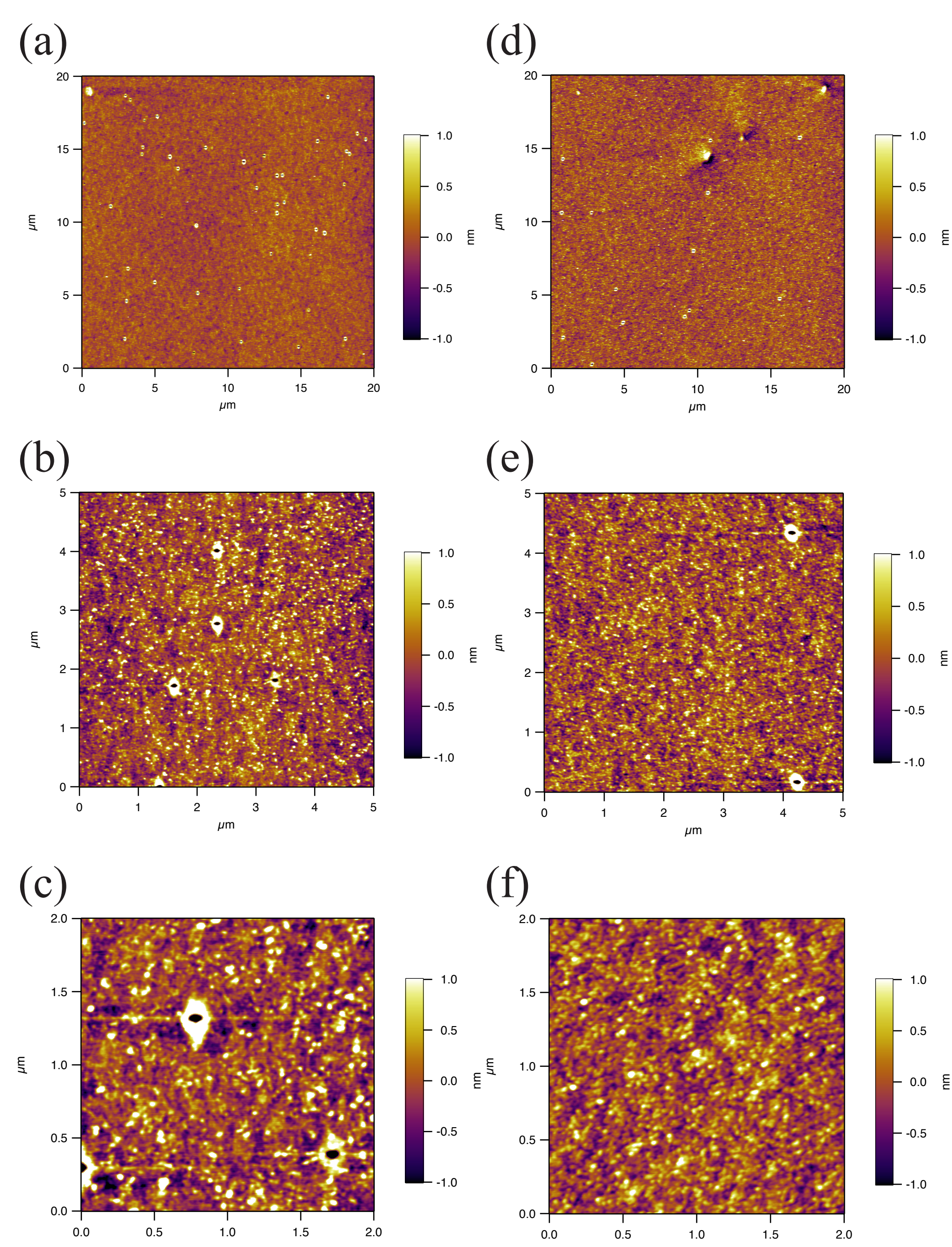


Figure 4: AFM images of Si doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ regrowth (a)-(c) and of Te doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ regrowth (d)-(f). (a) and (d) are $20 \times 20 \text{ } \mu\text{m}^2$, (b) and (e) are $5 \times 5 \text{ } \mu\text{m}^2$, and (c) and (f) are $2 \times 2 \text{ } \mu\text{m}^2$.

- AFM images show a reduction in the number of surface defects from 1.10×10^7 to $4.75 \times 10^6 \text{ cm}^{-2}$ for the Si and Si + Te doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ regrown sample
- Areas without cat-eye defects in the co-doped sample have lower density of mico dots, as seen in Figures 2 (c) and (e)
- The surface morphology of the co-doped sample is superior to that of the Si doped sample

X-Ray Diffraction

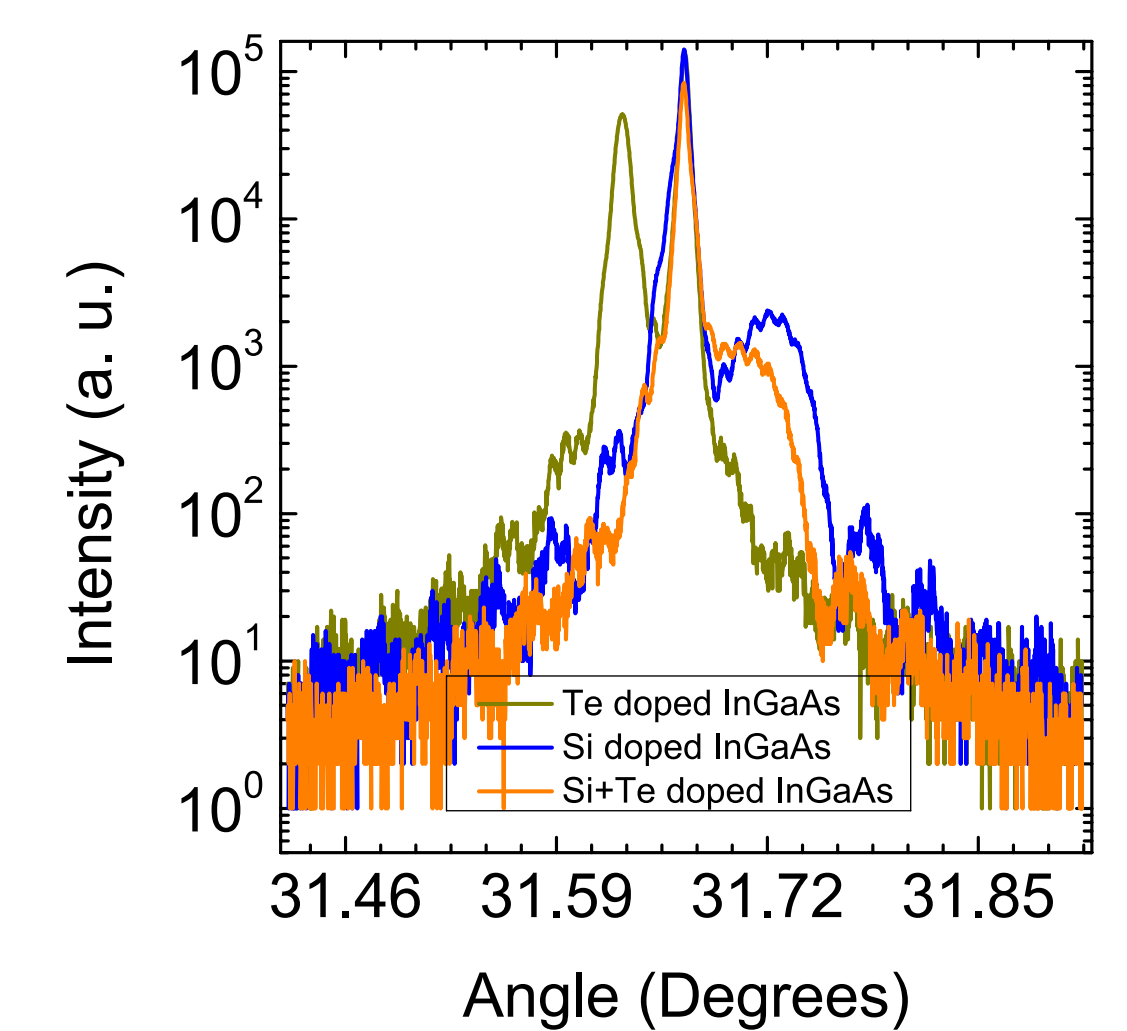


Figure 5: (a) Rocking curve scans of Te doped (olive), Si doped (blue), and Si and Te co-doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$.

- XRD shows more narrow substrate peak and more narrow shoulder peak for Si and Te co-doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ than for Si doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$
- Te doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ shows large (> 1% alloy concentration) lattice mismatch yielding no conclusions

Transmission Line Measurement

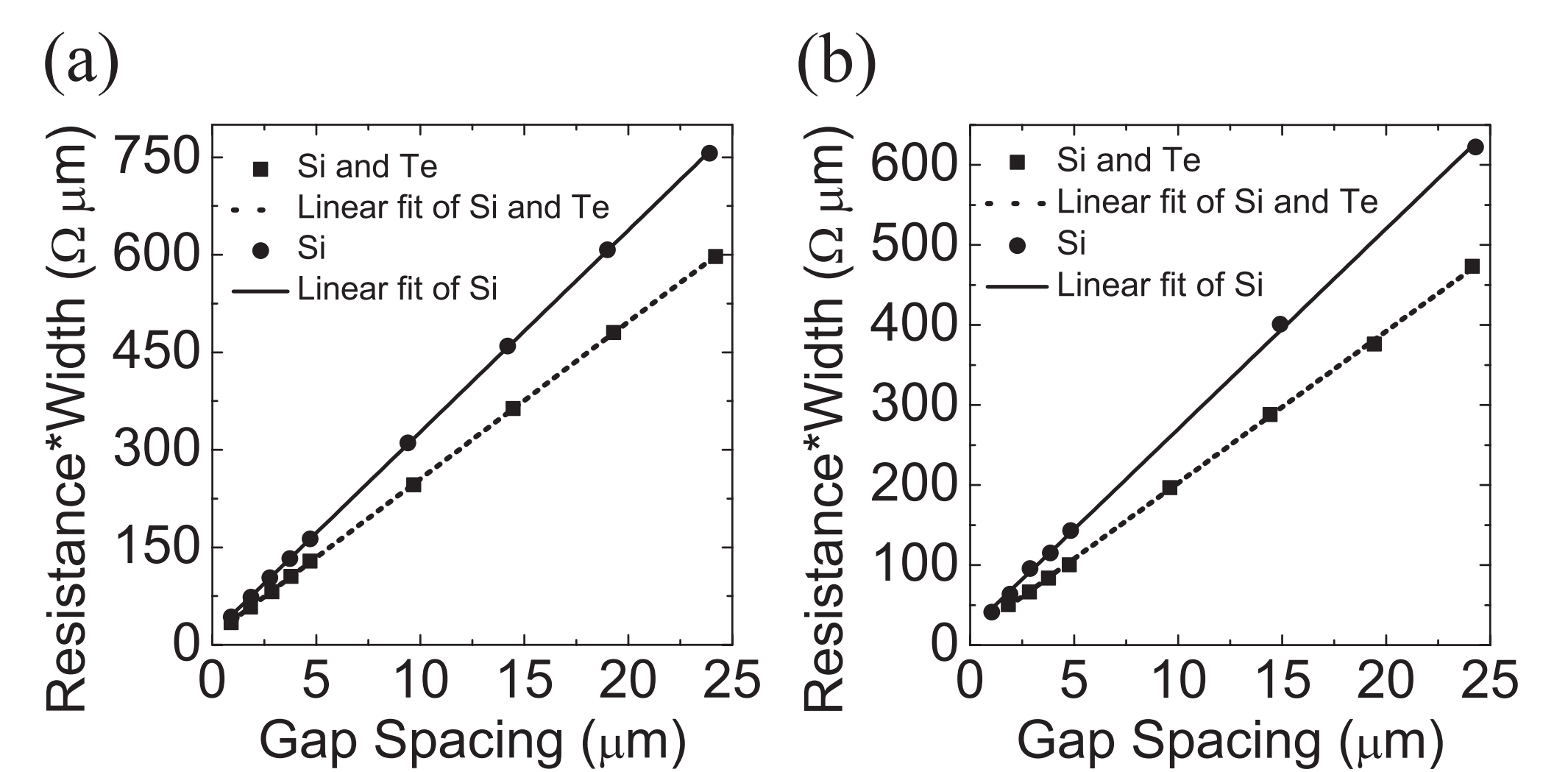


Figure 6: Resistance versus gap spacing for (a) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ TLM and (b) InAs TLM structures.

- Inclusion of Te lowers sheet resistance for both $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and InAs
- Inclusion of Te lowers contact resistance for both $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and InAs

	Si doped InAs	Si & Te co-doped InAs	Si doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	Si & Te co-doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$
$R_{SH} (\Omega)$	25.3	18.9	31.0	24
$R_c (\Omega-\mu\text{m})$	9.9	6.6	8.5	6.8
$\rho (\Omega-\mu\text{m}^2)$	3.9	2.3	2.3	1.9

Table 2: Summary of contact resistance data extracted from Figure 6 (a) and (b).

Conclusion

- Inclusion of Te as a co-dopant with Si lowers contact and sheet resistance for both $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and InAs
- Te likely improves contact and sheet resistance by improving material quality as seen in improved Hall mobility and sharpened x-ray peaks
- Te is an effective n -type dopant of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ up to $2.6 \times 10^{19} \text{ cm}^{-3}$

References

1. M. J. W. Rodwell, U. Singiseti, M. Wistey, G. Burek, A. C. Gossard, C. J. Palmstrom, E. Arkun, P. Simmonds, S. Stemmer, R. Engel-Herbert, Y. Hwang, Y. Zheng, P. Asbeck, Y. Taur, C. Sachs, A. Kummel, P. McIntyre, C. Van de Walle, and J. Harris, "Technology Development and Design for 22 nm InGaAs/InP-Channel MOSFETs," 2008 IEEE Indium Phosphide and Related Materials Conference, Versailles, France, 2008.
2. M. J. W. Rodwell, M. A. Wistey, U. Singiseti, G. J. Burek, E. Kim, A. Baraskar, J. Cagnon, Y. -J. Lee, S. Stemmer, P. C. McIntyre, A. C. Gossard, B. Yu, P. Asbeck, and Y. Taur, "Process Technologies for Sub-100 nm InP HBTs and InGaAs MOSFETs," 8th Topical Workshop on Heterostructure Microelectronics, Nagano, Japan, 2009.
3. M. J. W. Rodwell, E. Loisser, M. Wistey, V. Jain, A. Baraskar, E. Lind, J. Koo, Z. Griffith, J. Hacker, M. Urteaga, D. Mensa, R. Pierson, and B. Brar, "THz Bipolar Transistor Circuits: Technical Feasibility, Technology Development, Integrated Circuit Results," 2008 IEEE Compound Semiconductor IC Symposium, Monterey, CA, 2008.
4. A. K. Baraskar, M. A. Wistey, V. Jain, U. Singiseti, G. J. Burek, B. J. Thibeault, Y. J. Lee, A. C. Gossard, M. J. W. Rodwell, Journal of Vacuum Science and Technology B, 27 (2009) 2036.
5. N. Grandjean, J. Massies, Journal of Crystal Growth, 134 (1993) 51.
6. U. Singiseti, M. A. Wistey, G. J. Burek, A. K. Baraskar, B. J. Thibeault, A. C. Gossard, M. J. W. Rodwell, IEEE Electron Device Letters, 30 (2009) 1128.