A 107 GHz 55 dBΩ InP Broadband Transimpedance Amplifier IC for High-Speed Optical Communication Links

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***Abstract* — We report a 107 GHz baseband differential transimpedance amplifier IC for high speed optical communication links. The amplifier, comprised of two Darlington resistive feedback stages, was implemented in a 500 nm InP HBT process and demonstrates 55 dBΩ differential transimpedance gain, 30 ps group delay, P_{1dB} = -1 dBm, and is powered by a -5.2 V supply. Differential input and output impedances are 50Ω. The IC interfaces to -2V DC at the input for connections to high-speed photodiodes and -450 mV DC at the output for interfaces to Gilbert-cell mixers and to ECL logic.**

Index Terms* — *Broadband amplifiers, Heterojunction bipolar transistors, Indium phosphide, MMICs, Optical fiber communication, Optical receivers, Very high speed integrated circuits.

I. Introduction

The ever-growing demand for high data-rates in the consumer market imposes new challenges for optical communication links. In the 1980's, a large body of promising research in coherent optical communication was cast aside in favor of traditional incoherent communication that became attractive again due to the development of optical amplifiers. The relatively simple modulation and demodulation schemes of direct-detection methods made them the economically default choices.

Nevertheless, in the past decade optical communications has increasingly shifted to coherent techniques because of their superior spectral efficiency and noise. Though most such systems today use free-running optical local oscillators (LOs) with post-detection LO phase-recovery in DSP, we recently reported a 40 Gbs coherent optical receiver using a phase-locked optical local oscillator [1]. Extensive work on photonic integrated circuits [2] boosts the feasible complexity of such systems.

WDM super-channel communication [3] further improves the spectral efficiency of coherent optical systems. Wavelength channel spacing can be set precisely by optical wavelength synthesis [4]. Reducing cost, many WDM channels can be received by a single receiver IC, where each optical WDM channel appears in the receiver as a separate electrical RF subcarrier [5].

To support coherent optical communication while supporting complex modulation formats and/or multiple subcarriers, a wideband *linear* electrical front-end must be introduced. Linearity, high input dynamic range, wideband matching, low noise and a good interface with the optical IC are the key properties of such a front-end.

Recently reported broadband front-ends can be divided into two main groups: limiting and non-limiting (linear). The limiting front ends usually employ the g_m-Z_t (Cherry-Hooper) topology [6]. The g_m stage limits the signal while keeping the transimpedance stage in linear operation, thus maintaining the values of the input/output impedances. Gain-bandwidth products of g_m-Z_t amplifiers are poorer than those of linear differential amplifiers. Limiting amplifiers serve as combined gain blocks and decision circuits in BPSK and QPSK receivers.

In a given technology, non-limiting, linear amplifiers can deliver a higher bandwidth than limiting amplifiers. Linear amplifiers are necessary given more complex modulation formats (multiple RF subcarriers, 16QAM, etc.). A 3-dB bandwidth of 102 GHz is reported in [7].

The linear transimpedance amplifier (TIA) reported in this work comprises two-stage linear differential resistive-feedback amplifier (RFA) biased by a negative, -5.2 V, source. Due to a self-biased -2 V input voltage, the TIA directly interfaces to a photonic integrated circuit (PIC) [2], reverse-biasing the photodiodes by 2V. Diodes level-shift the output to -450 mV, permitting 50Ω-terminated connections to other linear circuits, such as Gilbert-cell mixers (GCM) for frequency conversion. The output interface is also compatible with ECL. The TIA demonstrates 107 GHz 3-dB bandwidth, 16 dB differential gain, -1dBm output at 1-dB gain compression, 30 ps group delay, and 675 GHz gain-bandwidth product with a power consumption of 365 mW. The gain-bandwidth is particularly high given the mature status of the 0.5 μm InP HBT IC technology employed. The TIA has been integrated into single-chip 2-channel [5] and 6-channel WDM optical receiver ICs.

II. Indium Phosphide HBT Technology

The IC was implemented using InP HBT 0.5 μm emitter width technology [8, 9] with cut-off frequencies f_τ = *300 GHz* and f_{max} = *300 GHz*. A 4-metal interconnect stack was used with 0.3 fF/μm^2 MIM capacitors

implemented between metal 1 and metal 2. A 50 Ω/sq thin film deposition forms resistors.

III. Resistive-Feedback amplifier

A. Background

In resistive feedback amplifiers (Fig. 1), emitter/source degeneration is added to a single-ended or differential stage, producing a stage having transconductance $g_m = (kT/qI + R_E/2)^{-1}$ (Fig. 2a). The transconductance stage has high input and output impedances; adding a feedback resistor of value $R_f = (1 - A_v)Z_0$ and selecting the stage transconductance according to $g_m = (1 - A_v)Z_0^{-1}$ results in a gain block of the desired gain $A_v = V_{out}/V_{in}$ and having input and output impedances $R_{in} = R_{out} = Z_0$. Both gain-bandwidth and noise are better than that of simple resistively-loaded amplifiers.

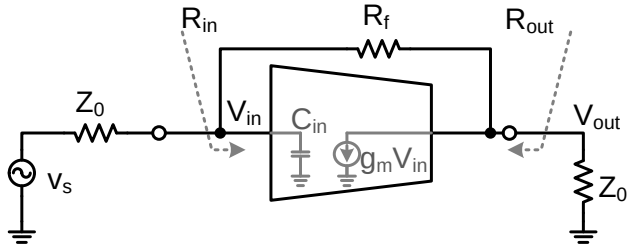

Fig. 1. Resistive feedback g_m stage driven loaded by a Z_0 impedance and driven by a Z_0 source.

B. Circuit Design

The g_m stage is an differential pair having emitter-followers which both buffer the stage input capacitance and increase the V_{CE} of the common-emitter transistors [10], *both effects* benefiting bandwidth. Detailed analysis is beyond our scope, but we note that with extrinsic transconductance constrained to $g_m = (1 - A_v)Z_0^{-1}$ and with emitter current density selected for peak f_t and f_{max}, the emitter junction areas of Q_1 and Q_3 are the only free design variables and are set to 2.5 μm^2 each. Increasing Q_1 and Q_3 junction areas increases capacitances and g_m but reduces parasitic resistances. Optimization by hand calculation minimizes the total $\sum R_i C_j$ first-order time constant. C_f adjusts damping.

Fig. 2 shows a full schematic and Fig. 2a a single stage in floor-plan orientation. The IC draws 70 mA from a -5.2 V supply. All transistors are biased at the optimum f_t, f_{max} current density of 3-4 mA/μm^2. Transistors $Q_{1\text{-}2}$ form the emitter follower stage of the Darlington with R_1=300 Ω. Transistors Q_3 are part of the differential degenerated common emitter stage with R_E=10 Ω. The differential pair current tail was implemented using resistors (R_2=165 Ω), instead of current mirrors as this gives lower noise and less capacitance. The feedback resistor R_f is 150 Ω.

The grey frame on Fig. 2b presents the two-stage full RFA within a receiver front end. The stages are directly cascaded. Via DC negative feedback through the resistances R_f of stage-1, the voltage drop across R_C (230 Ω), establishes a -2V DC input bias voltage which biases the input photodiodes. The large DC drop also permits R_C to be large, minimizing its loading of stage 1. The stage-2 DC output current, together with the level-shift diodes and the 50 Ω loads, establishes the stage-2 collector DC bias at -2V and the amplifier DC output at -450 mV

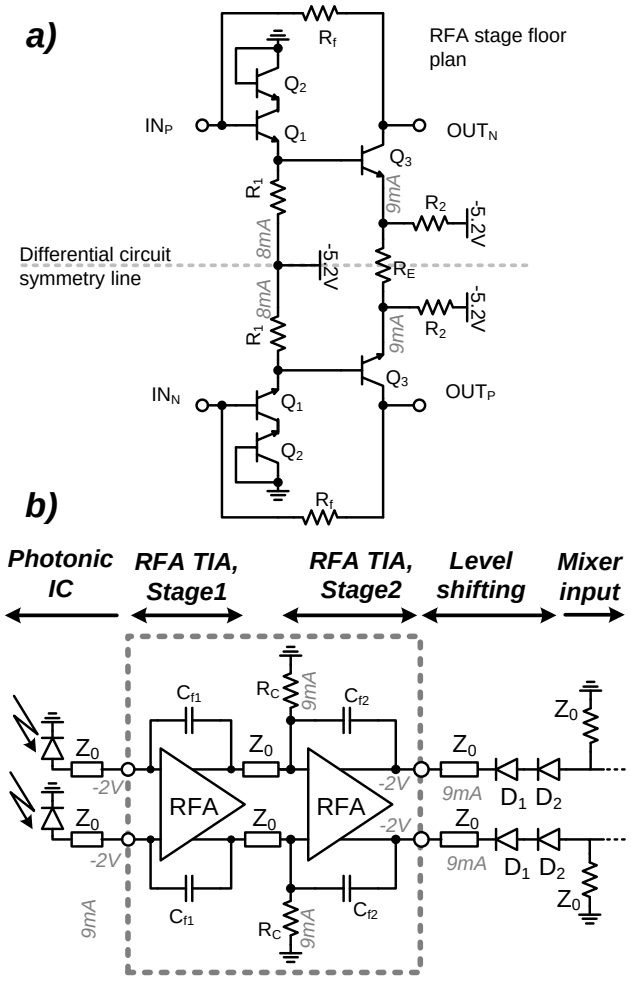

Fig. 2. RFA full schematics. a) single stage RFA floor plan schematic, b) full two stage RFA TIA block diagram (dashed frame) and its integration into a receiver front-end.

B. Layout

Signal lines are metal 1 and metal 2 inverted microstrip interconnects with a metal 3 ground plane. This allows controlled impedances on *all* IC interconnects. Metal 4 is

the power grid. This avoids cross-over capacitances between signal lines and power conductors, improving signal integrity and simplifying layout. Inverted microstrip allows narrow line spacing (approximately two times the line-to-ground distance, i.e. 6-10 μm), and a continuous unbroken ground-plane, maintaining ground integrity and avoiding ground-bounce.

A small overlap capacitance arises wherever M1 and M2 transmission-lines (with an M3 ground plane) cross. At the expense of added via inductance, this crossover capacitance can be avoided by transitioning one line in the crossover region to an M4 microstrip line with an M3 ground-plane. Though used in the larger (WDM) receiver ICs, this technique was not necessary in the amplifier itself.

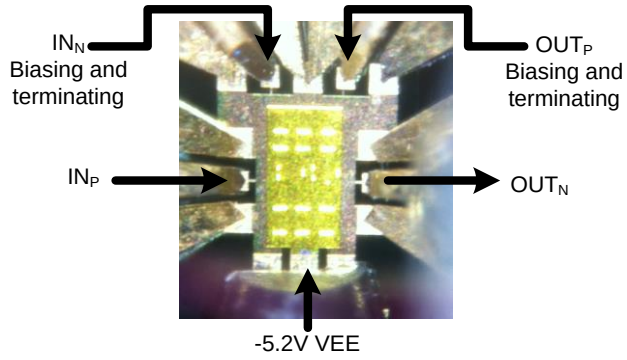

Fig. 3. RFA die photo.

All transmission-lines and passive components were individually EM-modeled by Agilent Momentum. The RFA test layout, Fig. 3, was designed in a single-ended fashion to permit measurements beyond 67 GHz. The remaining two ports are connected to bias Tees and RF terminations. The differential layout is fully symmetric, following the floor plan of Fig. 2a, and interconnects are kept short. The active IC area is 220x80 μm^2.

V. Measurement Results

Measurements include small-signal S-parameters, gain compression, and 30-44 Gb/s eye patterns.

A. Small-signal S-parameters

The S-parameter measurements were performed using an Agilent PNA-X N5257A for the 1-50 GHz band and OML millimeter wave extenders, controlled by an Agilent N5257A PNA-X 50-110 GHz, for the 50-75 GHz and 75-110 GHz bands. The input power was -24 dBm. Given the extended frequency range, only single-ended measurements were feasible. The remaining two ports were terminated in 50Ω connected through 65 GHz bias tees. Reflections from these bias tees and terminations are not corrected for in the two-port calibration, and produce ripple in the S-parameter data.

The low frequency single-ended gain is 9.8 dB with 2 dB gain ripple (Fig. 4). Adding 6 dB for a differential operation results in a 16 dB differential gain – a 55 dBΩ equivalent, with 107 GHz bandwidth. The gain-bandwidth product of the IC is 675 GHz. The measured group delay is 30ps. A -10 dB input/output return loss was measured up to 80 GHz, increasing to -5 dB at higher frequencies. In a fully differential operation the return losses are expected to improve due to balanced operation. S-parameters were measured for 1–3 mA input DC currents (to emulate photodiode DC bias currents) with less than 0.3 dB observed variation in the amplifier gain.

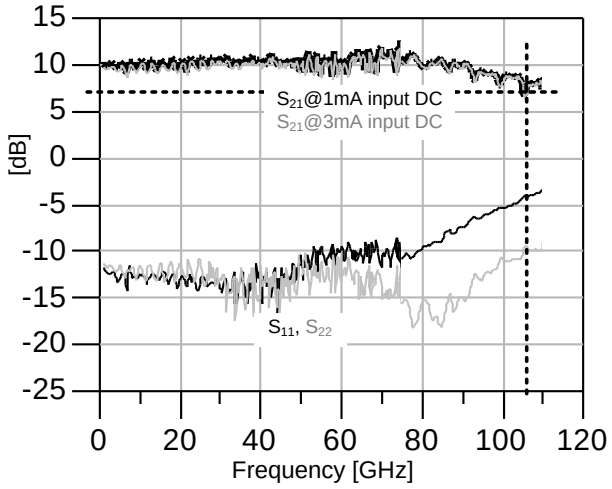

Fig. 4. Measured single-ended S_{21} and input/output insertion losses for the two-stage amplifier. Given two outputs, the differential gain should exceed the single-ended S_{21} by 6 dB.

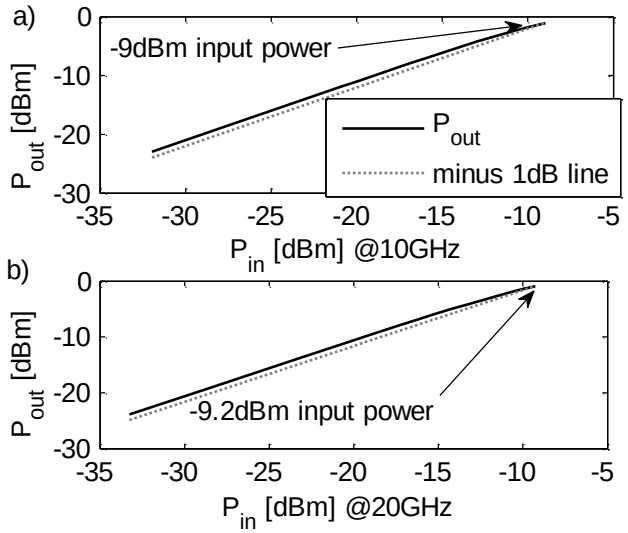

Fig. 5. P1dB measurement at a) 10 GHz input signal, b) 20 GHz input signal

B. Power compression and linearity

The gain compression measurements were performed using an R&S 100A 22 GHz signal generator to provide the input power and R&S FSU46 spectrum analyzer for output spectral measurement. The 1dB compression was measured up to 20 GHz. According to Fig. 5, the maximum input power for linear operation is -9 dBm (equivalent to 2.25 mA-amplitude input current), resulting in an output 1dB gain compression point of -1 dBm. With a simulated input referred current noise of 44 pA/√Hz, the estimated input dynamic range, for SNR>10 dB, is 33 dB.

C. Time domain measurements

While the amplifier's bandwidth should be sufficient to support even 160 Gb/s operation, equipment was available for testing only to 44 Gb/s. The data was generated by a Centellax TG1P4A 2^{31}-1 PRBS generator with 430 mV output amplitude. This was reduced 10 dB using coaxial attenuators. The IC output signal was sampled using an Agilent DCA-X 86100D oscilloscope with an Agilent 86118A 70 GHz remote sampling head.

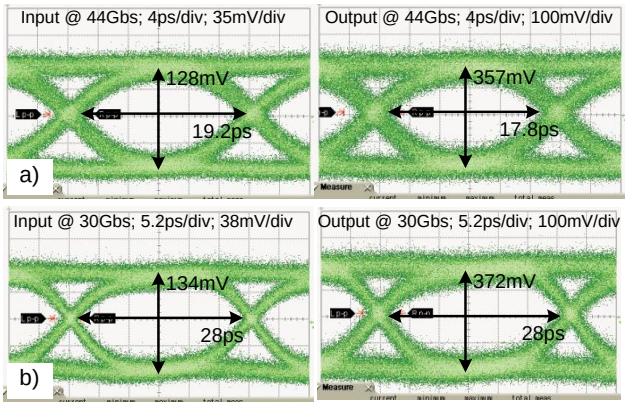

Fig. 6. Input/output eye diagram. a) 44 Gb/s, input amplitude of 128 mV, b) 30 Gb/s, input amplitude of 134 mV

The measurement results, Fig. 6, demonstrate a gain of 10dB, with peak-peak jitter addition of 2.5 ps at 44 GHz. The lack of ringing proves robust phase margin and stable design. The displayed rise/fall times are limited by the instrumentation.

V. Conclusions

A 107 GHz, 16 dB differential gain broadband two-stage Darlington resistive-feedback amplifier IC has been designed and demonstrated. The IC, fabricated on InP 500 nm HBT technology, has, to the authors' knowledge, the highest 3-dB bandwidth for fully differential topologies. Power consumption of 360 mW, compression point of -1 dBm and a gain-bandwidth product of 657 GHz were reported.

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References

[1] H. Park, M. Lu, E. Bloch, T. Reed, Z. Griffith, L. Johansson, L. Coldren and M. Rodwell, "40Gbit/s coherent optical receiver using a Costas loop," Opt.Express, vol. 20, pp. B197-B203, Dec, 2012.

[2] M. Lu, H. Park, E. Bloch, A. Sivananthan, J. Parker, Z. Griffith, L. A. Johansson, M. J. Rodwell and L. A. Coldren, "A photonic integrated circuit for a 40 Gbaud/s homodyne receiver using an optical Costas loop," in IEEE Photon. Conf., Post-Deadline PD. 1.4, 2012, .

[3] E. Torrengo, R. Cigliutti, G. Bosco, G. Gavioli, A. Alaimo, A. Carena, V. Curri, F. Forghieri, S. Piciaccia, M. Belmonte, A. Brinciotti, A. L. Porta, S. Abrate and P. Poggiolini, "Transoceanic PM-QPSK terabit superchannel transmission experiments at baud-rate subcarrier spacing," in Optical Communication (ECOC), 2010 36th European Conference and Exhibition on, 2010, pp. 1-3.

[4] E. Bloch, H. Park, M. Lu, T. Reed, Z. Griffith, L. A. Johansson, L. A. Coldren, D. Ritter and M. J. Rodwell, "A 1–20-GHz All-Digital InP HBT Optical Wavelength Synthesis IC," Microwave Theory and Techniques, IEEE Transactions on, vol. 61, pp. 570-580, 2013.

[5] H. Park, M. Piels, E. Bloch, M. Lu, A. Sivananthan, Z. Griffith, L. Johansson, J. Bowers, L. Coldren and M. Rodwell, "Integrated circuits for wavelength division de-multiplexing in the electrical domain," in Submitted in European Conference on Optical Communications, 2013,

[6] C. H. Fields, T. Tsen, C. McGuire, Yeong Yoon, D. Zehnder, S. Thomas, M. Montes, I. Valles, J. Duvall and T. Hussain, "110+ GHz Transimpedance Amplifier in InP-HBT Technology for 100 Gbit Ethernet," Microwave and Wireless Components Letters, IEEE, vol. 20, pp. 465-467, 2010.

[7] Joohwa Kim and J. F. Buckwalter, "A DC-102GHz broadband amplifier in 0.12µm SiGe BiCMOS," in Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE, 2009, pp. 53-56.

[8] M. Rodwell, E. Lind, Z. Griffith, A. M. Crook, S. R. Bank, U. Singisetti, M. Wistey, G. Burek and A. C. Gossard, "On the feasibility of few-THz bipolar transistors," in Bipolar/BiCMOS Circuits and Technology Meeting, 2007. BCTM '07. IEEE, 2007, pp. 17-21.

[9] M. Urteaga, R. Pierson, P. Rowell, M. Choe, D. Mensa and B. Brar, "Advanced InP DHBT process for high speed LSI circuits," in Indium Phosphide and Related Materials, 2008. IPRM 2008. 20th International Conference on, 2008, pp. 1-5.

[10] D. Mensa, Q. Lee, J. Guthrie, S. Jaganathan and M. J. W. Rodwell, "Baseband amplifiers in transferred-substrate HBT technology," in Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1998. Technical Digest 1998., 20th Annual, 1998, pp. 33-36.