A DC-100 GHz Bandwidth and 20.5 dB Gain Limiting Amplifier in 0.25μm InP DHBT Technology

Saeid Daneshgar[1], Zach Griffith[2] and Mark J. W. Rodwell[1]
[1]Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA, 93106, USA. Email: saeiddaneshgar@ece.ucsb.edu
[2]Teledyne Scientific and Imaging, 1049 Camino Dos Rios, Thousand Oaks, CA, 91360, USA. Email: Zachary.Griffith@teledyne.com

***Abstract*—A DC-100 GHz limiting amplifier is designed and fabricated in a 0.25 μm InP DHBT technology. The amplifier is designed in two stages using a modified Cherry-Hooper architecture proceeding an emitter-follower at each stage. Consuming 145 mW of power from a -2.5 V supply, it achieves 20.5 dB differential S_{21} gain with less than 1 dB gain ripple and better than 20 dB and 15 dB input and output return losses, respectively. The group delay of S_{21} is 9 psec with a variation less than ± 5.5 psec around that. Time domain large signal measurements verifies a single-ended output swing of 260 mV.**

***Index Terms*—Cherry-Hooper architecture, broadband amplifier, Limiting Amplifier, Indium Phosphide (InP), monolithic microwave integrated circuit (MMIC), optical fiber communications.**

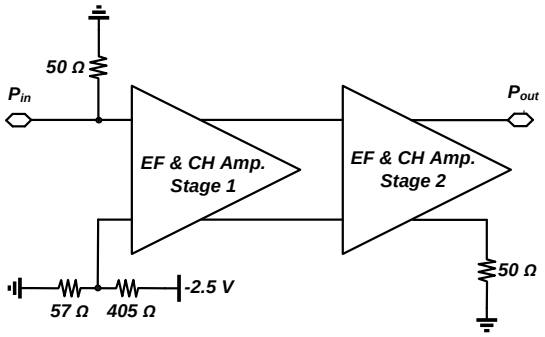

Fig. 1. Block level diagram of the limiting amplifier.

I. Introduction

The recent popularity of broadband services such as video on demand, cloud-based computing and storage has created a rapid growth of data traffic and consequently a high demand for high-rate communication systems. 100 Gb/s optical communication systems are now emerging in the long haul communications in order to respond this demand. Limiting amplifiers are the key components in these optoelectronic communication systems. The role of these amplifiers are: a) firstly, to have a low input sensitivity and sufficient gain to achieve saturated output levels from small-signal inputs which enables reliable decision making; b) secondly, to have a wide bandwidth to achieve short rise and fall times in order to provide an output signal with minimum distortion.

Cherry-Hooper limiting amplifiers are designed by cascading G_m and Z_t cells and operate with a saturated output level over a wide input dynamic range. They are suitable for applications such as NRZ BPSK or QPSK where the decision making is performed based on the large digital signal levels. On the other hand, applications using complex modulation formats such as multiple RF subcarriers and 16 QAM need broadband transimpedance amplifiers (TIAs) which are consisted of cascaded Z_t cells (resistive feedback amplifiers) and designed to operate in a linear regime with smaller output dynamic range compare to Cherry-Hooper limiting amplifiers. However, the broadband TIAs have wider bandwidth compare to Cherry-Hooper limiting amplifiers in a given technology.

A variety of broadband amplifiers (limiting and/or transimpedance) have been reported in the literature for high speed applications. These amplifiers have been fabricated in CMOS [1] or in different III/V technologies such as SiGe HBTs [2]-[8] or InP HBTs [9]-[14]. The amplifier presented in this paper has been designed using a modified Cherry-Hooper architecture ([2], [3] and [15]) and achieves 20.5 dB flat differential gain over its 3-dB bandwidth range of 0-100 GHz yielding a gain bandwidth product (GBW) of 1.06 THz. The ratio of amplifier's GBW to its power consumption is the highest among the other similar broadband amplifiers reported in the literature (Table I). The amplifier's input and output impedances are well-matched to 50 Ω which leads to input and output return losses better than 20 dB (1.22:1 VSWR) and 15 dB (1.43:1 VSWR), respectively. Careful design and layout of the amplifier have minimized the gain ripple in the frequency response to ± 0.5 dB. In Section II, we briefly describe InP DHBT process used in this work. Then, the circuit design is explained in Section III. Finally, the measurement results and comparison are presented in Section IV.

II. 0.25 μm Indium Phosphide DHBT Process

The limiting amplifier reported in this paper uses a 0.25 μm InP DHBT technology with a $\sim$4.5 V breakdown voltage. A single HBT has a peak bandwidth of $f_{max} = 700$ GHz and $f_T = 400$ GHz.

A four-metal interconnect stack is used in the fabrication of the circuit. Compact, stacked interconnect vias provide access from the top layer of metal interconnect for signal (3 μm thick) to the three lower layers (each 1 μm thick). Interconnects are separated by 1 μm BCB interlayer dielectric layers. MIM capacitors are 0.3 fF/μm^2 and thin-film resistors are 50 Ω/square.

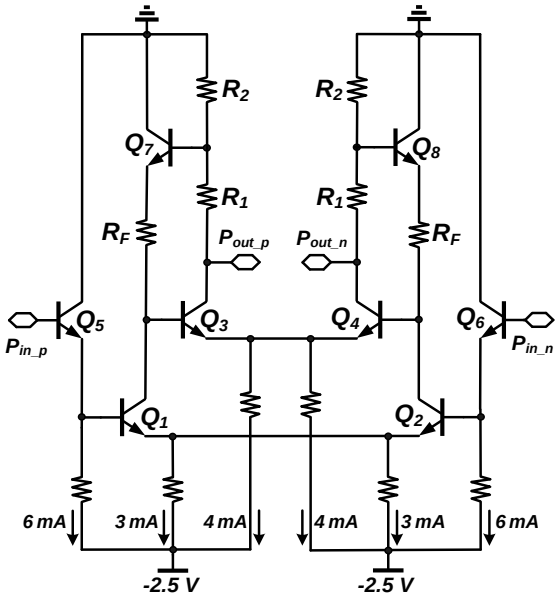

Fig. 2. Circuit schematic of each stage in the block diagram of Fig. 1.The value of resistances are: $R_1 = 30\,\Omega$, $R_2 = 50\,\Omega$ and $R_F = 40\,\Omega$. The emitter length of $Q_{1\text{-}8}$ is $3\,\mu$m.

III. Circuit Design and Layout

Fig. 1 shows the block level diagram of the limiting amplifier which has been designed by cascading two differential stages. Due to the unavailability of 4-port network analyzer for frequencies more than $67\,$GHz, gain and bandwidth measurements of the amplifier must be performed with single-ended measurements. Then, a $6\,$dB gain is added if the two outputs are balanced. Therefore, we have intentionally terminated one port in both input and output sides of the amplifier to $50\,\Omega$ in order to facilitate the single-ended measurements.

Each stage in Fig 1 has been consisted of a modified Cherry-Hooper amplifier proceeding an emitter-follower. The design methodology of the modified Cherry-Hooper amplifier has been explicitly reported in [3] and [15]. Transistor sizes and their corresponding emitter currents are selected based on noise consideration, power budget and biasing each transistor at its peak f_T current density. The choice of the resistors R_1, R_2 and R_F will determine the gain, bandwidth, output swing and output insertion loss. One of the main options to increase the gain is increasing R_2 in the range of $0 < R_2/R_1 < 2.5$ which has a little effect on the bandwidth [2].

Inverted thin-film microstrip wiring (M4 as a ground plane) has been selected for the layout of the amplifier in order to have a continuous ground plane without breaks, maintaining ground integrity and avoiding ground bounce. All the interconnects have been modeled using Agilent Momentum computer-aided design (CAD) tool in order to minimize the parasitic series inductance of interstage connections which causes gain ripple in the frequency response. In order to have a symmetric layout, the resistor in the emitter of each differential pair has been laid out using two parallel double-sized resistors.

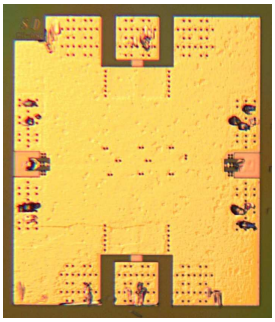

Fig. 3. Die-photo of the limiting amplifier ($0.425 \times 0.500\,\mathrm{mm}^2$)

IV. Measurement Results

The microphotograph of the limiting amplifier chip is shown in Fig. 3 which has a total area of $0.212\,\mathrm{mm}^2$ and an active area of $0.0144\,\mathrm{mm}^2$. The chip consumes $58\,$mA from a $-2.5\,$V power supply.

A. Small signal RF measurements

2-port RF measurements of the amplifier have been performed over the following three ranges of frequencies: a) $100\,$MHz to $50\,$GHz using an Agilent PNA-X N5245 network analyzer, b) 50-75 GHz and 75-110 GHz using OML T/R frequency extender modules, controlled by an Agilent N5242A PNA-X network analyzer. LRRM Probe tip calibration has been performed for all the measurements. Fig. 4 shows the simulated and measured single-ended S_{21} gain of the amplifier. Low frequency S_{21} gain is $14.5\,$dB with a gain ripple of $\pm 0.5\,$dB and a 3-dB bandwidth of $100\,$GHz. Considering a $6\,$dB higher differential gain, the GBW of the amplifier is calculated as $1.06\,$THz.

The simulated and measured input and output return losses are presented in Fig. 5. The input return loss is better than $20\,$dB over the 3-dB bandwidth while it remains better than $30\,$dB below $75\,$GHz. The output return loss is also better than $15\,$dB over the 3-dB bandwidth. The measured stability is plotted in Fig. 6 which indicates that the amplifier is unconditionally stable at all frequencies.

The measured phase of S_{21} has been extracted and shown in Fig. 7 which varies linearly at all the frequencies indicating small variations in the group delay as shown in Fig. 7. The amplifier has a nominal group delay of $9\,$psec and group delay variation of $\pm 5.5\,$psec over the 3-dB bandwidth.

B. Time-domain measurements

Due to the unavailability of a pattern generator operating above $40\,$Gb/s, we have performed time domain measurements using a Centellax TG1P4A pulse pattern generator with small $(47\,\mathrm{mV_{pp}})$ and large $(430\,\mathrm{mV_{pp}})$ amplitudes of the input signal at 30 and 40 Gb/s, $2^{31}-1$ PRBS. The eye diagrams are captured using an Agilent DCA-X 86100D wide-bandwidth oscilloscope with the Agilent 86118A remote sampling head directly connected to the output $67\,$GHz RF probe. The input eyes applied to the circuit are first measured using a through line and shown in Fig. 8(a)-(d). Bandwidth limitations due to

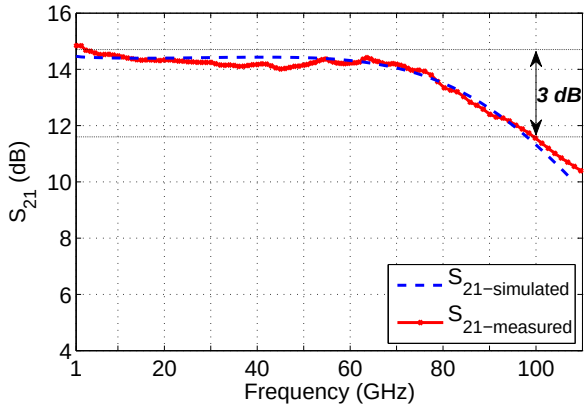

Fig. 4. Measured single-ended insertion loss (S_{21}) of the amplifier. Hence, the differential gain is $6\,\mathrm{dB}$ higher.

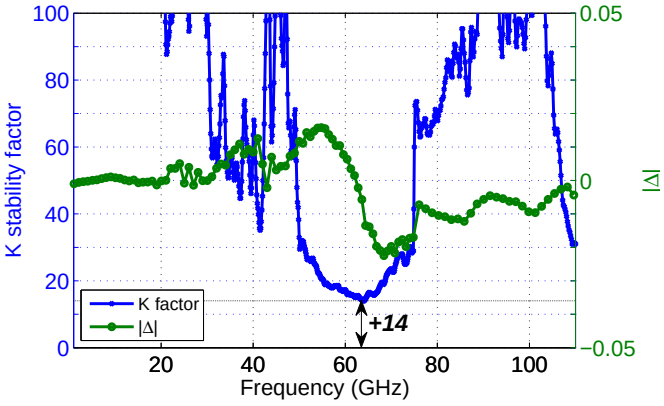

Fig. 6. Measured stability factors indicate unconditional stability across the entire bandwidth

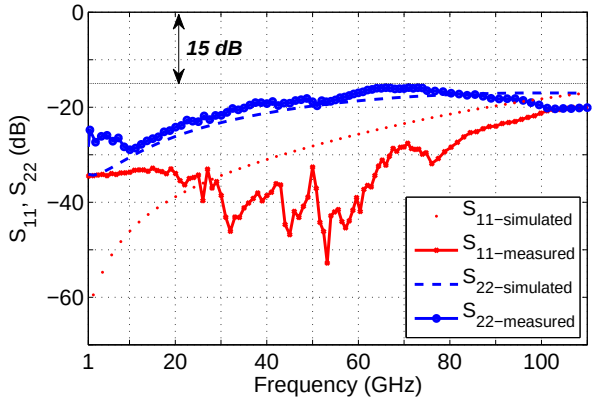

Fig. 5. Simulated and measured single-ended input and output return losses of the amplifier.

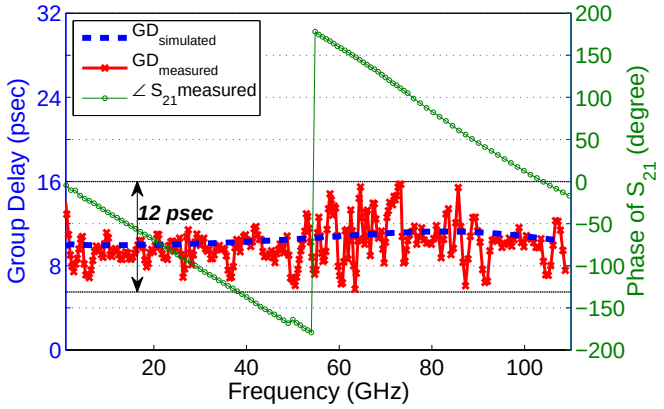

Fig. 7. Simulated and measured group delay variation of S_{21} (left axis) and measured phase of S_{21} (right axis) versus frequency.

the V-band bias-tee connected to the input side, have created an extensive amount of jitter specially in the rising edge of the eyes at large signal 40 Gb/s PRBS shown in Fig. 8(d). We could eliminate this effect by removing the bias tee, however having the bias tee was inevitable for the amplifier output eye measurements.

The captured 30 and 40 Gb/s eye diagrams corresponding to the input eyes of Fig. 8(a)-(d) are presented in Fig. 9(a)-(d). The amplifier achieves output signal amplitudes of $220\,\mathrm{mV_{pp}}$ and $260\,\mathrm{mV_{pp}}$ for small and large input signals, respectively. The rise and fall times of the 40 Gb/s data eye are $6\,\mathrm{psec}$ which is due to the bandwidth limitation of sampling head. The amplifier shows a peak-to-peak jitter of 3.4 and $4.8\,\mathrm{psec}$ for 40 Gb/s small and large input signals, respectively.

C. Performance comparison

Table I compares the performance of the presented limiting amplifier with the similar state of the art broadband amplifiers. The second column indicates the measured single-ended S_{21} gain of each amplifier while its correspodning inferred S_{21} gain is indicated $6\,\mathrm{dB}$ higher in the case the active circuit is differential.

V. Conclusion

A DC-$100\,\mathrm{GHz}$ limiting amplifier has been designed and fabricated in a $0.25\,\mu\mathrm{m}$ InP DHBT technology. The reported amplifier achieves a record GBW/P_{DC} as well as the best input and output return losses among the reported similar amplifiers in the literature.

Acknowledgments

This work was supported by the Defense Advanced Research Projects Agency (DARPA) under the HiFive Program. Additional thanks to Hyun-chul Park for his support and help on measurements.

References

[1] J. Kim *et al.*, "A 12 dBm 320 GHz GBW distributed amplifier in a $0.12\,\mu$m SOI CMOS, in *Proc. of IEEE ISSCC 2004*, pp. 478-540.

[2] Y. M. Greshishchev *et al.*, "A 60-dB gain, 55-dB dynamic range, 10-Gb/s broad-band SiGe HBT limiting amplifier," *IEEE JSSC*, vol.34, no.12, pp. 1914-1920, Dec. 1999.

[3] K. Ohhata *et al.*, "Design of a 32.7-GHz bandwidth AGC amplifier IC with wide dynamic range implemented in SiGe HBT," *IEEE JSSC*, vol.34, no.9, pp. 1290-1297, Sep. 1999.

[4] O. Wohlgemuth *et al.*, "SiGe broadband amplifiers with up to 80 GHz bandwidth for optical applications at 43 Gbit/s and beyond," in *Proc. 33rd EuMC*, vol. 3, pp. 1087-1090, Oct. 7-9, 2003.

TABLE I

COMPARISON TO SIMILAR BROADBAND AMPLIFIERS REPORTED IN THE LITERATURE.

Ref.	Gain$_S$ [*] (dB)	Gain$_D$ [**] (dB)	BW[†] (GHz)	GBW[‡] (GHz)	IRL[⊥] (dB)	ORL[⊤] (dB)	GR[◊] (dB)	GD[§] (psec)	Supply (V)	Power (mW)	Area (mm^2)	GBW/P$_{DC}$ (GHz/mW)	Architecture	Process
[1]	11	-	90	320	>5	>7	2.4	-	2.5	210	1.28	1.52	DA[1]	0.12μm SOI CMOS
[4]	7	13	81	362	>7	>7	>5	-	5.5	495	1.17	0.73	DA[1]	SiGe f_T=200 GHz
[5]	10	16	62	391	>11	>3	>3	-	-5	775	0.3	0.51	EF & DP[2]	SiGe f_T=200 GHz
[6]	14	20	84	840	>7	>7	4	±32	-5.5	990	0.63	0.85	EF & CA[3]	0.18μm SiGe
[7]	-1	5	62	110	>14	-	>3	-	2.5	125	-	0.88	EF & CH[4]	0.13μm SiGe
[8]	10	-	102	323	>8	>9	<2	±6	2	73	0.29	4.42	DF & CW[5]	0.12μm SiGe
[9]	24	30	43	1360	>7	>7	>2	±10	-4	500	0.7	2.72	EF & CH[4]	1μm InP SHBT
[11]	15	21	44	494	>6	>10	<2	-	5.2	458	0.66	1.08	EF & CH[4]	InGaAs-InP HBT
[12]	15	-	67	729	>7	>10	>2	±10	3.5	133	0.09	5.50	-	0.5μm InP DHBT
[13]	21	-	120	1350	-10	-10	3	±15	-	610	2	2.21	DA[1]	InP DHBT
[14]	10	16	110	694	>5	>5	>3	-	-4	304	0.95	2.28	EF & CH[4]	0.25μm InP HBT
This work	14.5	20.5	100	1060	>20	>15	1	±5.5	-2.5	145	0.21	7.31	EF & CH[4]	0.25μm InP DHBT

[*] Measured single-ended S_{21} gain, [**] Inferred differential S_{21} gain, [†] 3-dB bandwidth of S_{21}, [‡] Inferreded differential S_{21} gain $\times$ its 3-dB bandwidth, [⊥] Input return loss, [⊤] Output return loss, [◊] Total S_{21} gain ripple, [§] Group delay variation of S_{21}, [1] Distributed amplifier, [2] Emitter follower & differential pair, [3] Emitter follower & cascode stage, [4] Emitter follower & Cherry-Hooper stage, and [5] Darlington feedback amplifier & constructive wave amplifier.

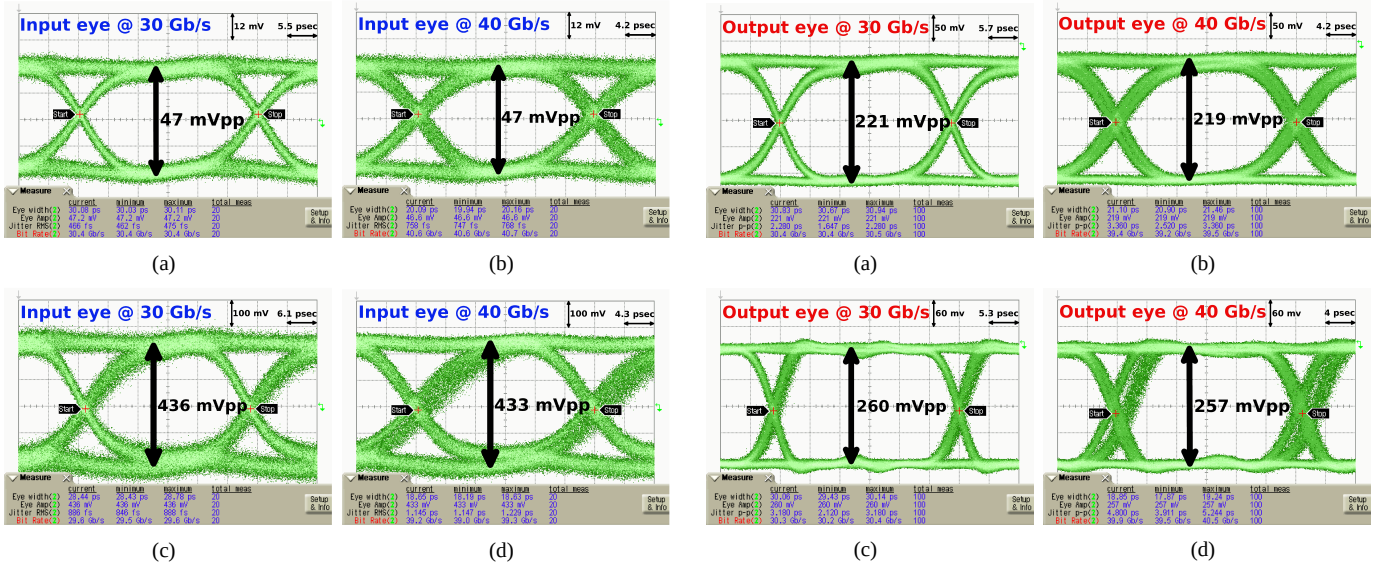

Fig. 8. Measured input eyes using a through line at (a) 30 Gb/s PRBS with 47 mV$_{pp}$ input amplitude; (b) 40 Gb/s PRBS with 47 mV$_{pp}$ input amplitude; (c) 30 Gb/s PRBS with 433 mV$_{pp}$ input amplitude; (d) 40 Gb/s PRBS with 433 mV$_{pp}$ input amplitude.

Fig. 9. Measured output eyes applying the input eyes of Fig. 8 to the amplifier. (a) 30 Gb/s PRBS with 221 mV$_{pp}$ output amplitude; (b) 40 Gb/s PRBS with 219 mV$_{pp}$ output amplitude; (c) 30 Gb/s PRBS with 260 mV$_{pp}$ output amplitude; (d) 40 Gb/s PRBS with 257 mV$_{pp}$ output amplitude.

[5] W. Perndl *et al.*, "A 60 GHz broadband amplifier in SiGe bipolar technology," in *Proc. of IEEE BCTM 2004*, pp.293-296, 13-14 Sept. 2004.

[6] S. Trotta *et al.*, "An 84 GHz bandwidth and 20 dB gain broadband amplifier in SiGe bipolar technology," *IEEE JSSC*, vol.42, no.10, pp. 2099-2106, Oct. 2007.

[7] T. S. Mukherjee *et al.*, "A wide bandwidth sige broadband amplifier for 100 Gb/s Ethernet applications," in *Proc. of IEEE ISCAS 2009*, pp. 1835-1838, 24-27 May 2009.

[8] J. Kim *et al.*, "Staggered Gain for 100+ GHz Broadband Amplifiers," *IEEE JSSC*, vol.46, no. 5, pp. 1123-1136, May. 2011.

[9] Z. Lao *et al.*, "A DC-43GHz-Bandwidth 30dB-Gain Amplifier," in *Proc. of IEEE MTT-S IMS 2006*, pp. 1664-1667, 11-16 June 2006.

[10] J. Dupuy *et al.*, "A 6 Vpp, 52 dB, 30-dB Dynamic Range, 43 Gb/s InP DHBT Differential Limiting Amplifier," in *Proc. of IEEE CSICS, 2011*, pp. 1-4, 16-19 Oct. 2011.

[11] J. S. Weiner *et al.*, "An InGaAs-InP HBT differential transimpedance amplifier with 47-GHz bandwidth," *IEEE JSSC*, vol. 39, no. 10, pp. 1720-1723, Oct. 2004.

[12] V. E. Houtsma *et al.*, "InP Single-Ended Transimpedance Amplifier with 92-GHz Transimpedance Bandwidth," in *Proc. of IEEE CSICS 2007*, pp. 1-4, 14-17 Oct. 2007.

[13] V. Hurm *et al.*, "InP DHBT-based distributed amplifier for 100 Gbit/s modulator driver operation," *Electronics Letters*, vol.44, no.12, pp.705,706, June 2008.

[14] C. H. Fields *et al.* , "110+ GHz Transimpedance Amplifier in InP-HBT Technology for 100 Gbit Ethernet," *IEEE MWCL*, vol. 20, no. 8, pp. 465-467, Aug. 2010.

[15] C. D. Holdenried *et al.*, "Analysis and design of HBT Cherry-Hooper amplifiers with emitter-follower feedback for optical communications," *IEEE JSSC*, vol.39, no.11, pp. 1959-1967, Nov. 2004.