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High performance raised source/drain InAs/$In_{0.53}Ga_{0.47}As$ channel metal-oxide-semiconductor field-effect-transistors with reduced leakage using a vertical spacer

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We demonstrate raised source/drain InAs/$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect-transistors incorporating a vertical spacer in the high-field region between the channel and the drain. The spacer significantly reduces off-state leakage at a high drain bias (V_{DS}) without increasing the source/drain contact pitch. Subsequently, thinning the InAs layer within the channel further reduces the off-state leakage and subthreshold swing (SS). At ~60 nm gate length and $V_{DS} = 0.5$ V, devices with a 6 nm/3 nm InAs/$In_{0.53}Ga_{0.47}As$ channel show 2.7 mS/μm peak transconductance (g_m) and 125 mV/dec SS, while devices with a 4.5 nm/3 nm InAs/$In_{0.53}Ga_{0.47}As$ channel show 2.4 mS/μm peak g_m and 96 mV/dec SS. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4838660]

InAs/InGaAs and indium-rich $In_xGa_{1-x}As$ ($x > 0.53$) have been widely evaluated as the metal-oxide-semiconductor field-effect transistor (MOSFET) channel for high-performance very large scale integration (VLSI) applications.[1–6] These materials have small bandgap, and high leakage can arise from band-to-band tunneling or from impact ionization in the high-field gate-drain region, degrading off-current and subthreshold swing (SS).[7] In metal-oxide-semiconductor high-electron-mobility transistor (MOS-HEMT)[2,3] structures (Figure 1(a)), under bias, the drain depletion edge moves laterally away from gate edge, reducing the drain field, and thereby reducing band-band tunneling, impact ionization, and drain-induced barrier lowering (DIBL). To accommodate this lateral depletion region, the N+ source/drain (S/D) separation must significantly exceed the gate length and contact pitch, which reduces the transistor packing density in VLSI. Using epitaxial regrowth processes,[5,10] a raised N+ source and drain can be aligned within a few nm of the gate edges (Figure 1(b)), enabling the small S/D contact pitch necessary for VLSI, but the gate-drain depletion distance is small and the drain field is large. This increases both leakage and short-channel effects at a given gate length (L_g).[5]

Here, we report raised S/D InAs/$In_{0.53}Ga_{0.47}As$ MOSFETs using an undoped vertical spacer (Figure 1(c)) in the high-field region between the channel and the N+ drain. Without increasing the S/D contact pitch, the vertical spacer reduces the drain field, and therefore off-state leakage significantly decreases at a high drain bias (V_{DS}). For a short channel (60 nm-L_g), a 6 nm/3 nm InAs/ $In_{0.53}Ga_{0.47}As$ channel device with an 8 nm vertical spacer shows 2.7 mS/μm peak transconductance (g_m) and 125 mV/dec SS at $V_{DS} = 0.5$ V. By then thinning the InAs channel (Figure 1(d)) we further improve the off-state characteristics through increased quantized bandgap and through better gate control, at 55 nm-L_g, a 4.5 nm/3 nm InAs/ $In_{0.53}Ga_{0.47}As$ channel device with an 8 nm vertical spacer shows 2.4 mS/μm peak transconductance (g_m), 130 mV/V DIBL and 96 mV/dec SS, again at $V_{DS} = 0.5$ V.

The epitaxial layers for *sample A*, grown on semi-insulating InP by solid source molecular beam epitaxy, include a 50 nm unintentionally doped (U.I.D) InAlAs buffer, a 250 nm $1.0 \times 10^{17}\,cm^{-3}$ P-doped InAlAs barrier, a 100 nm U.I.D InAlAs barrier, a 2 nm N-doped ($2.0 \times 10^{12}\,cm^{-2}$) InAlAs pulse-doping layer, a 5 nm U.I.D InAlAs setback, a 3 nm $In_{0.53}Ga_{0.47}As$ sub-channel, a 6 nm InAs channel (strained), a 3 nm $In_{0.53}Ga_{0.47}As$ upper cladding, and a 5 nm $5 \times 10^{19}\,cm^{-3}$ N-type doped $In_{0.53}Ga_{0.47}As$ cap. For *samples B and C* the cap is 5 nm U.I.D. $In_{0.53}Ga_{0.47}As$. To form dummy gates, ~150 nm hydrogen silsesquioxane (HSQ) was spun and patterned by e-beam lithography. To form the N+ S/D, 60 nm Si-doped ($4 \times 10^{19}\,cm^{-3}$) $In_{0.53}Ga_{0.47}As$ was then selectively regrown by metal organic vapor deposition (MOCVD) on the cap layer. Device mesas were isolated and the dummy gates removed in buffered oxide etch. For all samples, in the gate region, the exposed cap and upper cladding layers were then removed by digital etching.[5,8] For *sample C* the upper 1.5 nm of the InAs channel was also removed by digital etching. The samples were then immediately transferred into the atomic layer deposition (ALD) chamber, and pre-cleaned/passivated by alternating cycles of N_2 plasma and of trimethylaluminum (TMA). HfO_2 gate dielectric was then deposited.[9] The samples were then annealed at 400 °C in forming gas (5% H_2/95% N_2) for 15 min. Ni/Au was thermally deposited as the gate electrode, and Ti/Pd/Au S/D contacts defined by liftoff. Figure 2(a) illustrates a device schematic cross-section. Defining the vertical distance between the N+ S/D and the InAs channel as the spacer, the spacer and the InAs thicknesses for *sample A, B,* and *C* are listed in the table of Figure 2(a).

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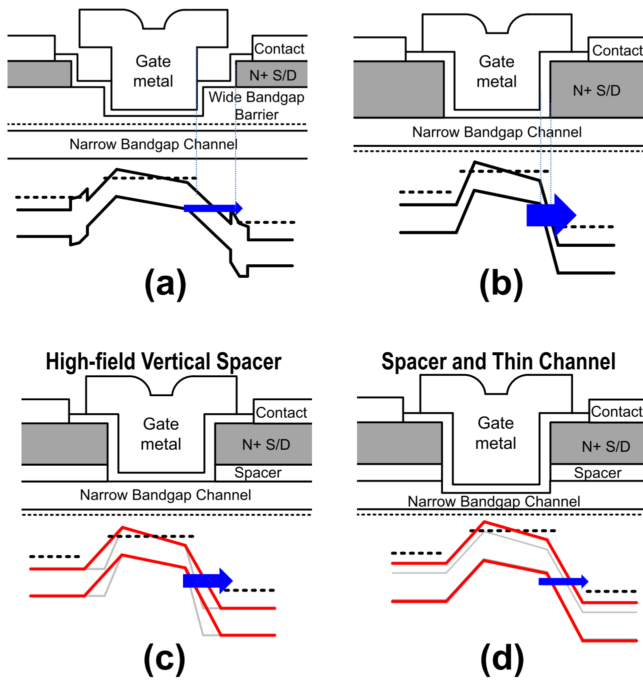
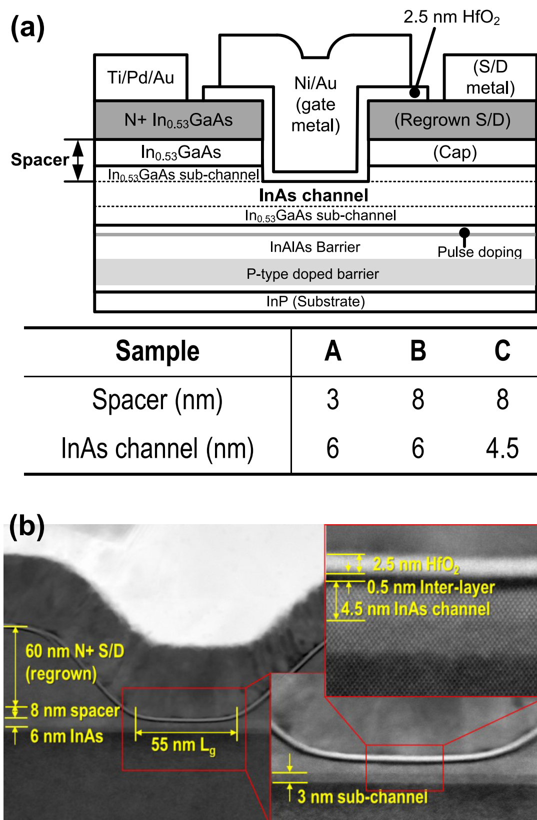


FIG. 1. Structures and energy band diagrams of a III-V MOS-HEMT (a) and of a raised S/D MOSFET (b). Leakage is reduced using vertical spacers (c) and thinner channels (d). The dotted lines indicate electron quasi-Fermi level. The band-to-band tunneling rate is qualitatively illustrated with the thicknesses of arrows.

Figure 2(b) shows a cross-sectional HAADF-STEM of a 55 nm-L_g device (*sample C*). The STEM inset shows 2.5 nm HfO_2, a 0.5 nm interfacial layer formed by the *in-situ* N_2/TMA pre-treatment, a 4.5 nm InAs channel (not relaxed) and an 3 nm $In_{0.53}Ga_{0.47}As$ sub-channel.



Sample	A	B	C
Spacer (nm)	3	8	8
InAs channel (nm)	6	6	4.5

FIG. 2. (a) The schematic cross-section of the device structure. The table defines the differences between the three experimental samples. (b) HAADF-STEM cross-sections of a 55 nm-L_g device of *sample C*.

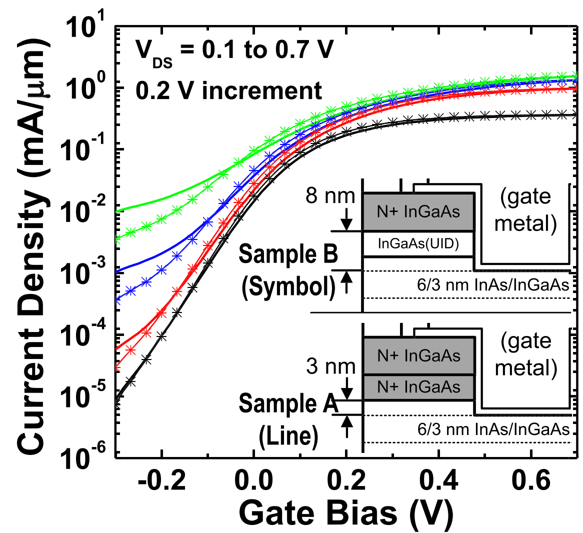


FIG. 3. I_D-V_{GS} characteristics of Samples A and B at ~75 nm L_g. Line plus symbol refers to *sample* B and just line refers to *sample* A

We first compare *samples A and B*. In the transfer characteristics at ~75 nm L_g (Figure 3), the 8 nm spacer in the drain high-field region reduces the off-state leakage by 5:1 at $V_{DS} = 0.5$ V and $V_{GS} = -0.3$ V when compared to the 3 nm spacer. Figures 4(a) and 4(b) show transfer and output characteristics for a 60 nm-L_g device of *sample B*. Its peak g_m is 2.7 mS/μm at $V_{DS} = 0.5$ V and its R_{on} is 268 Ω μm at $V_{GS} = 1.0$ V. Figure 4(c) shows SS versus L_g for *samples A* and *B*. At $V_{DS} = 0.5$ V, *sample B* shows 10%–15% improved SS at all gate lengths. Figure 4(d) compares peak g_m versus L_g for *samples A* and *B*; spacers as thick as 8 nm only negligibly affect the peak g_m. Figure 5(a) shows on-resistance (R_{on}) in terms of gate length for *sample A* and *B*. On-resistances for

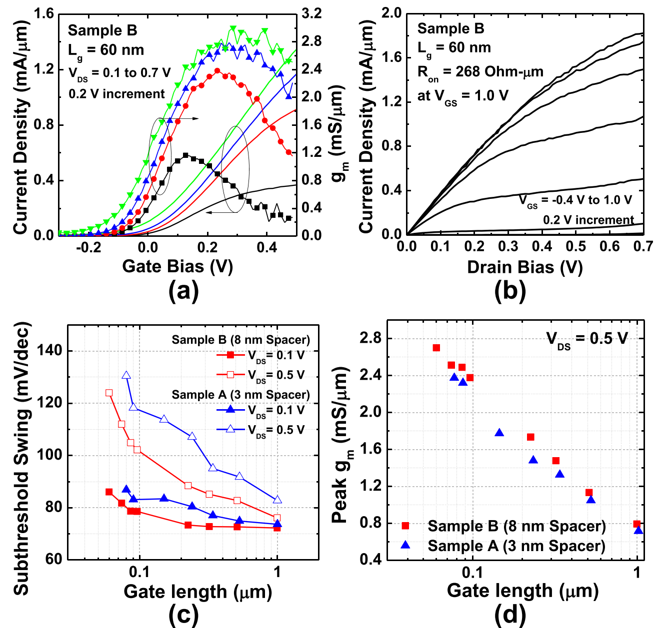


FIG. 4. (a) Drain current and transconductance vs. V_{GS} for *sample B*. (b) Common-source characteristics for *sample* B showing 1.8 mA/μm maximum I_D. (c) Subthreshold swing vs. L_g, at 100 mV and 500 mV V_{DS}, for *samples A* and *B*. (d) Peak transconductance vs. L_g, at 500 mV V_{DS}, for *samples A* and *B*.

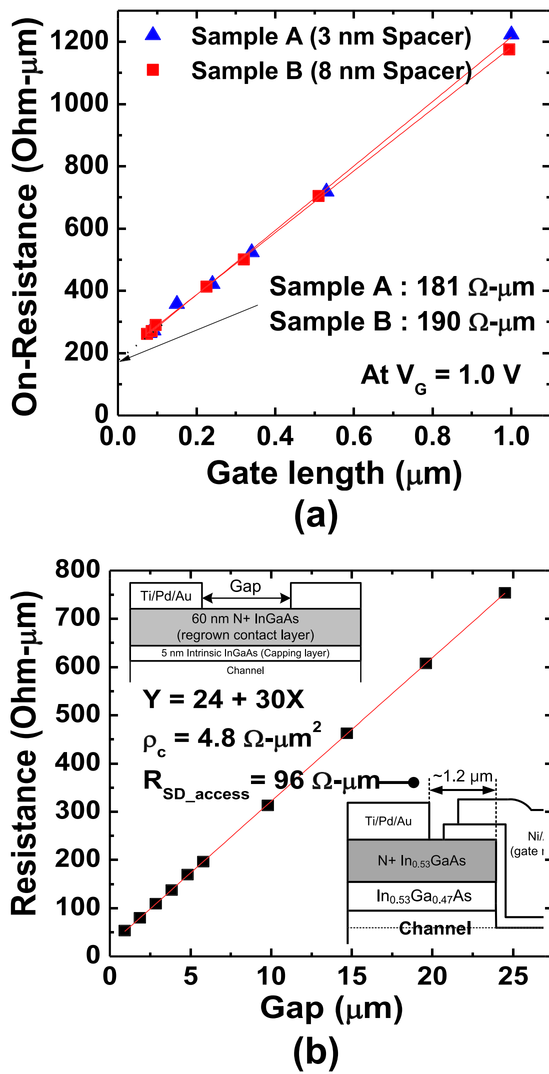


FIG. 5. (a) Drain-source on-resistance vs. L_g for *samples A* and *B*. (b) TLM measurement for the N+ S/D and contacts.

sample A and *B*, interpolated at the zero gate length, are 181 and 190 Ω μm, respectively, and their discrepancy is within fitting error. This, again, confirms adding the 8 nm spacer layer does not degrade on-state performance by increasing R_{on}. From transmission line method (TLM) measurement for regrown S/D (Figure 5(b)), the S/D specific contact resistivity is 4.8 Ω μm^2 and sheet resistance (R_{sheet}) of the regrown S/D is 30 Ω/sq. The large 1.2 μm distances between the gate edges and the S/D contacts contribute 96 Ω μm to R_{on} and degrade g_m by ~11%.

We now compare 6 nm- (*sample B*) and 4.5 nm-thick-InAs channel devices (*sample C*). Figure 6(a) compares SS as a function of L_g for *samples B* and *C*. The thin InAs channel (*sample C*) has significantly improved SS at high V_{DS} and small L_g, which we attribute to better electrostatic control and the larger quantized bandgap. The quantized bandgaps for *sample B* and *C*, computed from a self-consistent 1-D Schrödinger and Poisson solver, are ~0.44 eV and ~0.50 eV, respectively. Figure 6(b) shows peak g_m in terms of L_g. The peak g_m of *sample C* is ~10% smaller than that of *sample B* at every gate length. This is possibly due to increased surface roughness scattering. Figure 6(c) shows a transfer characteristic of a 55 nm-L_g device for *sample C*. At $V_{DS} = 0.5$ V, its

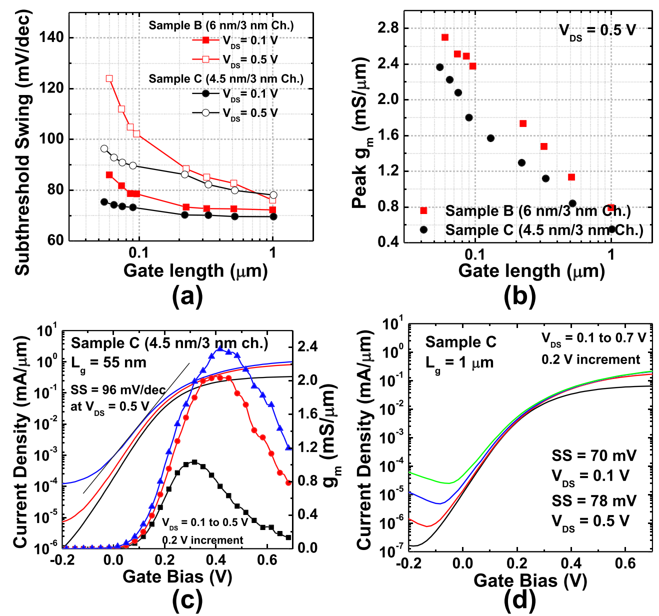


FIG. 6. (a) Subthreshold swing vs. L_g, at 100 mV and 500 mV V_{DS}, for *samples B* and *C*. (b) Peak transconductance vs. L_g, at 500 mV V_{DS}, for *samples B* and *C*. (c) I_D-V_{GS} characteristics and transconductance of *sample C* at $L_g = 55$ nm. (d) I_D-V_{GS} characteristics of *sample C* at $L_g = 1$ μm.

SS is 96 mV/dec and peak g_m is 2.4 mS/μm. Defined $I_D = 1$ μA/μm, the threshold voltage (V_T) is 60 mV and DIBL is 130 mV/V. Figure 6(d) plots the transfer curve for an 1 μm-L_g device of *sample C*. Its SS at $V_{DS} = 0.1$ V is 70 mV/dec from which its interfacial trap density (D_{it}) is determined to be $\sim 5 \times 10^{12}$ /cm^2 eV. Its gate leakage (I_G) is less than 0.1 A/cm^2 at relevant bias conditions (not shown).

In conclusion, we have demonstrated raised S/D InAs/$In_{0.53}Ga_{0.47}As$ channel MOSFETs using an intrinsic $In_{0.53}Ga_{0.47}As$ spacer in a high-field region between InAs channel and N + S/D. The devices with an 8 nm spacer shows 5:1 reduced off-state leakage and 10%–15% lower SS at $V_{DS} = 0.5$ V when compared to those with a 3 nm spacer. The device with a 6 nm/3 nm InAs/$In_{0.53}Ga_{0.47}As$ channel and 60 nm L_g shows 2.7 mS/μm peak g_m and 125 mV/dec SS at $V_{DS} = 0.5$ V, which is record peak g_m in any III-V MOSFETs technology to date. Furthermore, by thinning the InAs channel to 4.5 nm, the device with an 8 nm spacer and 55 nm-L_g shows 2.4 mS/μm peak g_m, 96 mV/dec SS at $V_{DS} = 0.5$ V, and 130 mV/V DIBL.

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