Development of AlAsSb as a barrier material for ultra-thin-channel InGaAs nMOSFETs

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ABSTRACT

We investigated $AlAs_{0.56}Sb_{0.44}$ epitaxial layers lattice-matched to InP grown by molecular beam epitaxy (MBE). Silicon (Si) and tellurium (Te) were studied as n-type dopants in $AlAs_{0.56}Sb_{0.44}$ material. Similar to most Sb-based materials, $AlAs_{0.56}Sb_{0.44}$ demonstrates a maximum active carrier concentration around low-10^{18} cm^{-3} when using Te as a dopant. We propose the use of a heavily Si-doped InAlAs layer embedded in the AlAsSb barrier as a modulation-doped layer. The $In_{0.53}Ga_{0.47}As/AlAs_{0.56}Sb_{0.44}$ double heterostructures with a 10 nm InGaAs well show an electron mobility of about 9400 $cm^2/V\cdot s$ at 295 K and 32000 $cm^2/V\cdot s$ at 46 K. A thinner 5 nm InGaAs well has an electron mobility of about 4300 $cm^2/V\cdot s$ at 295 K. This study demonstrates that $AlAs_{0.56}Sb_{0.44}$ is a promising barrier material for highly scaled InGaAs MOSFETs and HEMTs.

INTRODUCTION

III-V metal-oxide-semiconductor field effect transistors (MOSFETs), particularly $In_xGa_{1-x}As$ ($x\geq0.53$), are being investigated to replace silicon for future CMOS VLSI technology. At the same oxide thickness, the low electron transport mass with resultant high saturated and injection velocity may provide high on-state current and transconductance. To date, most InGaAs MOSFETs are built utilizing the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ material system. Aiming at replacing Si channels below 10 nm gate-length generations, the InGaAs channel thickness must be scaled down (t_{ch}~2-5 nm) in order to maintain strong electrostatic gate control. Thinning the channel could also decrease the electron wave-function depth, increase total gate capacitance and device transconductance. However, given the small conduction band offset between $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ (~0.5 eV), upon shrinking the InGaAs channel thickness, the increased eigenstate energy will cause increased electron wave-function penetration into the barrier layer, leading to a parallel conduction path in the barrier. The channel electron spillover into the barrier layer will degrade electron transport velocity and reduce device performance [1]. Additionally, the increasing eigenstate energy with decrease of channel thickness will reduce the total allowable sheet charge density in the channel before the Fermi level reaches the conduction band energy of the barrier layer. Further increases in gate voltage will modulate the parasitic charge in the barrier layer with resultant less confinement and lower transconductance. Therefore, to mitigate these problems, a wider band-gap barrier material with higher conduction band offset to InGaAs channel is needed for realizing InGaAs MOSFETs for sub-10-nm generations.

In this work, an $AlAs_{0.56}Sb_{0.44}$ layer lattice matched to InP is proposed as a novel barrier material for $In_{0.53}Ga_{0.47}As$ channel MOSFETs. $AlAs_{0.56}Sb_{0.44}$ with a 1.6-1.7 eV conduction band offset to $In_{0.53}Ga_{0.47}As$ at the Gamma valley could provide better electron confinement compared with $In_{0.52}Al_{0.48}As$ barrier [2, 3]. The growth and doping behavior of $AlAs_{0.56}Sb_{0.44}$ layers were

investigated by solid source molecular beam epitaxy (MBE). Silicon and tellurium were studied as n-type dopant sources. However, similar to most Sb-based materials, $AlAs_{0.56}Sb_{0.44}$ demonstrates a limited maximum active carrier concentration of around low-10^{18} cm^{-3}. Instead of using n-doped AlAsSb layers, a Si-doped $In_{0.52}Al_{0.48}As$ layer was inserted in the AlAsSb barrier as a modulation-doped layer. We demonstrate an $In_{0.53}Ga_{0.47}As/AlAs_{0.56}Sb_{0.44}$ two dimensional electron gas (2DEG) structure with 10 nm channel thickness, showing an electron mobility of about 9400 $cm^2/V{\cdot}s$ at 295 K and 32000 $cm^2/V{\cdot}s$ at 46 K. A highly scaled 5 nm $In_{0.53}Ga_{0.47}As/AlAs_{0.56}Sb_{0.44}$ 2DEG structure still maintains an electron mobility of about 4300 $cm^2/V{\cdot}s$ at 295 K. The mobility degradation in the thinner channel could be attributed to the effect of interface roughness scattering.

EXPERIMENT

All the $AlAs_{0.56}Sb_{0.44}$ samples were grown by Veeco Gen II solid source molecular beam epitaxy using As_2 and Sb_2 from valved crackers. The substrates were epi-ready, semi-insulating InP (001) substrates. To grow the mixed group-V $AlAs_{0.56}Sb_{0.44}$ material, As_2 and Sb_2 flux must be carefully calibrated in order to control the composition of AlAsSb layer. Figure 1 shows the X-ray diffraction measurements of two lattice-matched n-doped $AlAs_{0.56}Sb_{0.44}$ epitaxial layers grown at different V/III ratio. For $AlAs_{0.56}Sb_{0.44}$ lattice matched to InP, the beam equivalent pressure (BEP) ratio of As_2 to Sb_2 is around 5.1 for the total $(As_2+Sb_2)/Al$ ratio ~22 and As_2/Sb_2~1.8 for total $(As_2+Sb_2)/Al$~42. All the AlAsSb epitaxial layers were grown at 490 °C measured by infrared pyrometer and the growth rate was 0.24 μm/hr. During the growth of AlAsSb, the reflected high energy electron diffraction (RHEED) shows a 1x3 surface reconstruction. Silicon (sample A series) and tellurium (sample B series) were also investigated as n-type dopant sources for $AlAs_{0.56}Sb_{0.44}$ layers. Table I summarizes the growth conditions and Hall measurements for all the n-doped AlAsSb samples. From XRD measurements, the lattice mismatch between AlAsSb layers and InP substrates is below $\pm 4{\cdot}10^{-3}$ for all the n-doped samples. The active carrier concentration was measured by van der Pauw technique at room temperature.

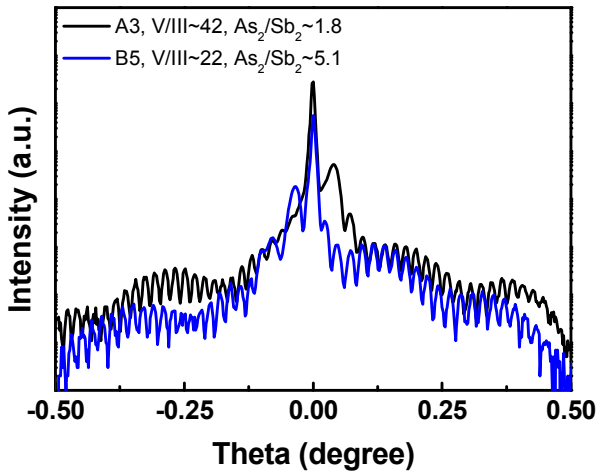

Figure 1. X-ray diffraction measurements of n-doped AlAsSb layers grown at different V/III ratio. The lattice matched condition to InP substrates is As_2/Sb_2~5.1 for total $(As_2+Sb_2)/Al$~22 and As_2/Sb_2~1.8 for total $(As_2+Sb_2)/Al$~42.

Table I. The growth conditions and Hall measurement results for Si-doped $AlAs_{0.56}Sb_{0.44}$ (Sample A series) and Te-doped $AlAs_{0.56}Sb_{0.44}$ layers (Sample B series).

Sample	Total V/III ratio	As_2/Sb_2 ratio	Si or Te cell temperature (°C)	Type	Active carrier (10^{17} cm^{-3})	Hall mobility ($cm^2/V{\cdot}s$)
A1	22	5.1	1300	n	4.27	701.7
A2	22	5.1	1360	n	2.95	951.3
A3	42	1.8	1360	n	4.89	756.2
B1	22	5.1	550	n	0.66	252.1
B2	22	5.1	600	n	5.30	210.5
B3	22	5.1	625	n	8.59	141.7
B4	22	5.1	650	n	15.6	338.2
B5	22	5.1	675	n	20.3	269.6

To examine the electron transport properties in $In_{0.53}Ga_{0.47}As$ quantum wells with respect to $In_{0.52}Al_{0.48}As$ and $AlAs_{0.56}Sb_{0.44}$ barriers, double-heterojunction 2DEG structures were grown as shown in Figure 2(a) and (b). The 2DEG structures consist of a SI-InP substrate, a 270 nm InAlAs buffer layer, a 30 nm InAlAs or AlAsSb bottom barrier, a 5 nm or 10 nm InGaAs channel, a 3 nm InAlAs or AlAsSb spacer layer, a 3 nm $1.3{\cdot}10^{19}$ cm^{-3} Si-doped InAlAs modulation-doped layer, a 15 nm InAlAs or AlAsSb top barrier and a 5 nm InGaAs cap layer. At the AlAsSb-on-InAlAs interfaces and AlAsSb-on-InGaAs interfaces, the growth was interrupted for two minutes under As exposure in order to stabilize the As flux, and pump down the background As pressure. In addition, a heavily Si-doped InAlAs modulation-doped layer was inserted between the AlAsSb top barrier and the AlAsSb spacer layer to achieve high n-type doping. The schematic conduction band profile of 5 nm InGaAs/AlAsSb 2DEG structure is shown in Figure 2(c). The 2DEG carrier concentration and Hall mobility were measured by van der Pauw technique from 45 K to room temperature.

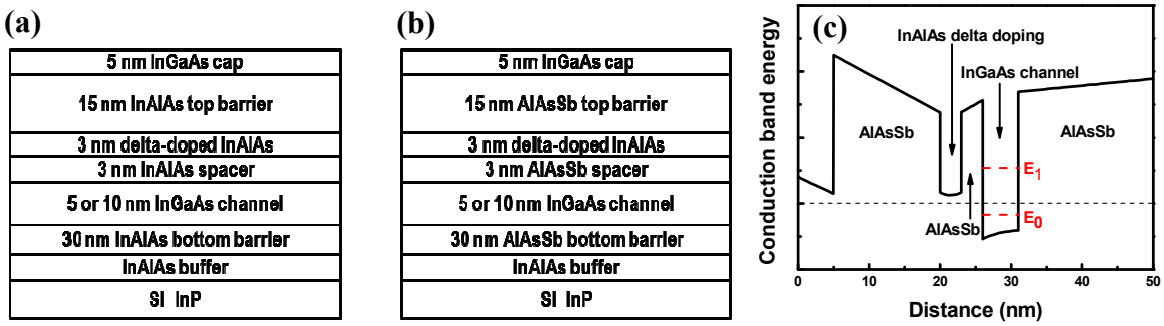

Figure 2. (a) InGaAs/InAlAs and (b) InGaAs/AlAsSb 2DEG structures with 3 nm, $1.3{\cdot}19$ cm^{-3} Si-doped InAlAs modulation-doped layer inserted in the top barrier. (c) The schemetic conduction band profile of 5 nm InGaAs channel with the AlAsSb barrier layer.

DISCUSSION

Table I summarizes the electrical properties of Si-doped (Sample A series) and Te-doped (Sample B series) $AlAs_{0.56}Sb_{0.44}$ layers. It was found that Te is capable of doping the AlAsSb

layers more effectively, while Si appears not to be a robust n-type dopant in AlAsSb layers. Similar to most Sb-based materials, the Te-doped AlAsSb samples show a limited electron concentration of about $2 \cdot 10^{18}$ cm^{-3} under current growth conditions. In comparison, the active carrier concentration of Si-doped AlAsSb samples is around low-10^{17} cm^{-3}, which is lower than that of Te-doped AlAsSb. Also, it was known that Si exhibits amphoteric doping behavior in III-V semiconductors. Si had been reported as a donor for AlAs while being an acceptor for AlSb [4, 5]. This amphoteric nature of Si may introduce dopant instability in AlAsSb layers, rendering it unsuitable as a carrier supply layer for practical device applications.

In order to overcome the lack of heavily doped AlAsSb layers, a heavily Si-doped InAlAs layer was embedded in the AlAsSb barrier as a modulation-doped layer, as shown in Figure 2(b). This device concept was first reported on InAs/AlSb heterostructure-field-effect transistors [6, 7]. Figure 3 shows temperature-dependent Hall measurements of InGaAs/InAlAs and InGaAs/AlAsSb 2DEG structures. It was found that the sheet carrier density of both InGaAs/AlAsSb and InGaAs/InAlAs 2DEG's is about 2.0-2.4$\cdot 10^{12}$ cm^{-2} and is insensitive to temperature as shown in Figure 3(a). In Figure 3(b), the InGaAs/AlAsSb double heterostructures with a 10 nm InGaAs well show an electron mobility of about 9400 $cm^2/V \cdot s$ at 295 K and 32000 $cm^2/V \cdot s$ at 46 K, which is comparable to the InGaAs/InAsAs 2DEG's. With the reduction of the InGaAs well width from 10 nm to 5 nm, the electron mobility of the InGaAs/AlAsSb 2DEG's degrades more rapidly than the InGaAs/InAlAs 2DEG's. Although the 2DEG Hall mobility degrades upon thinning the channel thickness, a highly scaled 5 nm InGaAs/AlAsSb 2DEG structure still retains an electron mobility up to about 4300 $cm^2/V \cdot s$ at 295 K.

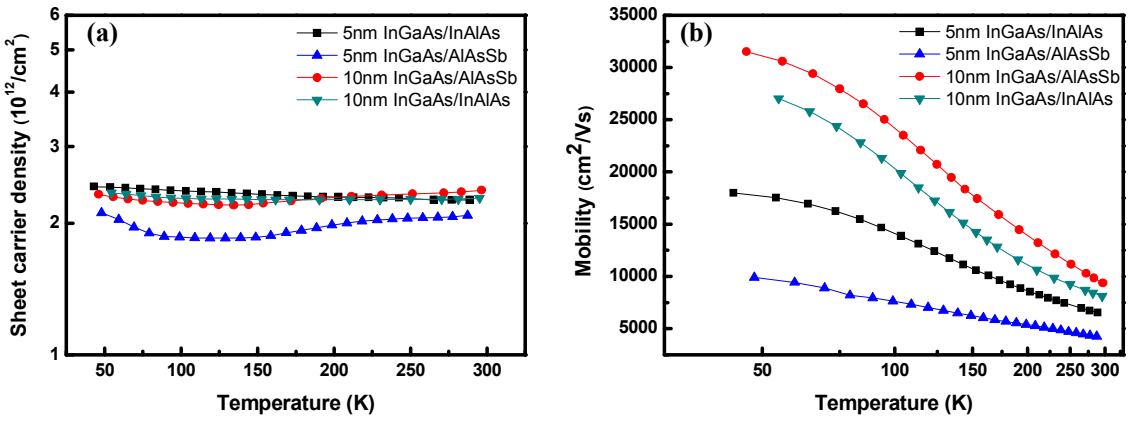

Figure 3. (a) The temperature-dependent sheet carrier density and (b) temperature-dependent Hall mobility of InGaAs/InAlAs and InGaAs/AlAsSb 2DEG structures.

To clarify the effects of different scattering mechanisms on the electron transport in InGaAs/AlAsSb 2DEG structures, theoretical calculations were implemented which considered acoustic phonon scattering [8], polar optical phonon scattering [9-10], remote impurity scattering [11], interface roughness scattering [11], and alloy scattering [12]. The InGaAs/AlAsSb quantum well was considered as an infinite quantum well and no intersubband scattering was taken into account for the simulation. This approximation is satisfactory because the conduction band offset of InGaAs/AlAsSb is large and only the lowest subband is occupied as shown in Figure 2(c). The total electron mobility can be calculated using Matthiessen's rule, as seen in equation 1.

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_{ac}} + \frac{1}{\mu_{op}} + \frac{1}{\mu_{im}} + \frac{1}{\mu_{irs}} + \frac{1}{\mu_{alloy}} \quad (1)$$

Figure 4(a) and 4(b) show the simulation of temperature-dependent electron mobility for 10 nm and 5 nm InGaAs/AlAsSb 2DEG structures respectively. The calculated electron mobility is in good agreement with experimental data from the InGaAs/AlAsSb 2DEG's. In the high temperature regime, polar optical phonon scattering is the main scattering process in the 2DEG's. In the low temperature regime, alloy scattering dominates the electron mobility for the 10 nm InGaAs well. However, upon thinning the channel, the interface roughness scattering becomes the dominant term among all the scattering processes. For the 5 nm InGaAs well, the low temperature 2DEG electron mobility is limited by both alloy and interface roughness scattering. The room temperature mobility is also degraded due to severe interface roughness scattering.

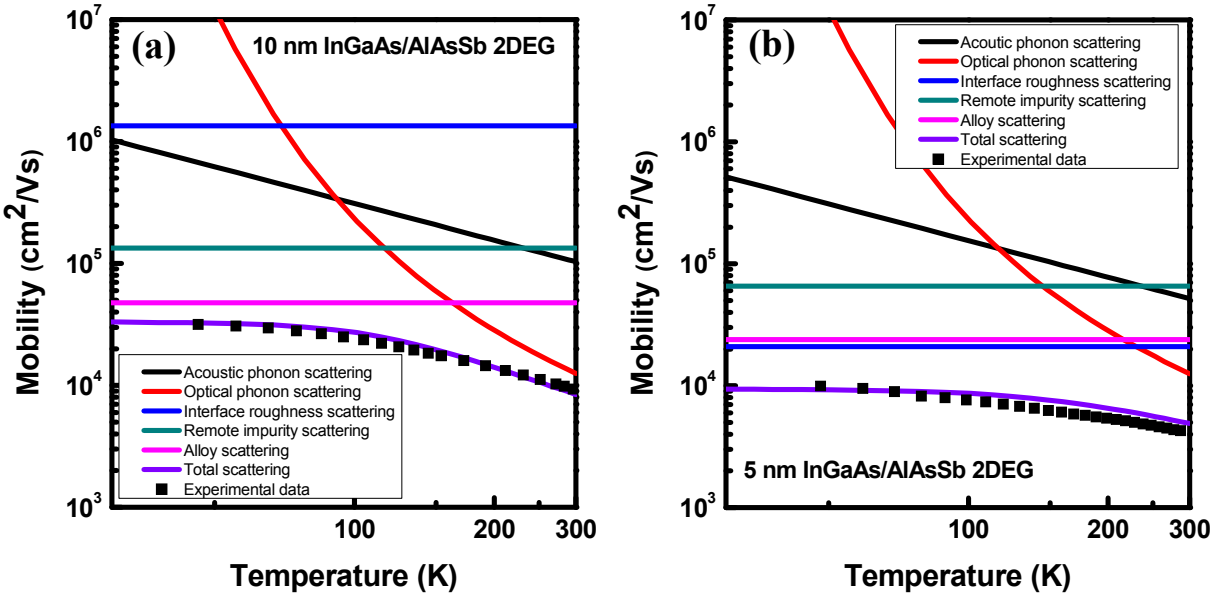

Figure 4. The calculated electron mobility and experimental results for (a) 10 nm and (b) 5 nm InGaAs/AlAsSb 2DEG's. In the simulation, the spacer layer is 3 nm, and the 2DEG sheet carrier density is 2.4×10^{12} cm^{-2}, and the remote impurity doping density is 3.9×10^{12} cm^{-2}. The interface topology is assumed as a Gaussian fluctuation with average height Δ =1ML(2.93Å) and correlation length Λ =100 Å.

From the above simulation, it is evident that the rapid drop of electron mobility for the InGaAs/AlAsSb 2DEG's upon thinning the channel could be attributed to the rougher InGaAs/AlAsSb interface as compared to the InGaAs/InAlAs interface. Growing an interface with a high aluminum content bottom layer may lead to a rough interface, which has been reported in GaAs/AlAs and InAs/AlSb material systems [13-15]. To implement the AlAsSb barrier in ultra-thin-channel InGaAs MOSFETs or HEMTs, the interface roughness scattering must be minimized so that the InGaAs channel can preserve high electron transport mobility. Therefore, further improvements on the interface smoothness will be of great importance for realizing high performance ultra-thin-channel InGaAs MOSFETs or HEMTs.

CONCLUSIONS

We have successfully grown $AlAs_{0.56}Sb_{0.44}$ barrier layers lattice matched to InP and demonstrated a high mobility $In_{0.53}Ga_{0.47}As/AlAs_{0.56}Sb_{0.44}$ two dimensional electron gas structure using a Si-doped InAlAs modulation-doped layer. The room temperature electron mobility of the $In_{0.53}Ga_{0.47}As/AlAs_{0.56}Sb_{0.44}$ 2DEG's–with about 9400 $cm^2/V \cdot s$ for a 10 nm InGaAs channel and 4300 cm^2/V for a 5 nm InGaAs channel–is comparable to that of the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ material system. From the theoretical calculation of 2DEG electron transport, the mobility degradation upon thinning the InGaAs channel is attributed to interface roughness scattering. This work shows promise for using $AlAs_{0.56}Sb_{0.44}$ material as the barrier layer for realizing high performance InGaAs MOSFETs and HMETs.

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