High Transconductance Surface Channel $In_{0.53}Ga_{0.47}As$ MOSFETs Using MBE Source-Drain Regrowth and Surface Digital Etching

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***Abstract* — We demonstrate $In_{0.53}Ga_{0.47}As$ surface channel MOSFETs using a gate-last process and MBE source/drain (S/D) regrowth. The structure uses a sacrificial N+ InGaAs channel cap layer between the regrown S/D contact layer and the channel, which is removed in the channel region by a "digital" etch process incorporating UV ozone oxidation and surface stripping in dilute HCl. A device with 65 nm-L_g and 1.2 nm EOT shows 1.6 mS/μm peak transconductance at V_{ds} = 0.5 V and 120 mV/dec SS at V_{ds} = 0.05 V, while 535 nm-L_g devices show 95 mV/dec SS at at V_{ds} = 0.1 V**

Keywords—InGaAs MOSFETs; source-drain regrowth; digital etching style; substitutional-gate; surface channel

I. Introduction

Because of the potential for increased on-state current, $In_{1-x}Ga_xAs$ MOSFETs have been widely studied for potential future application in VLSI [1]-[6]. High performance MOSFETs require ultra-thin EOT gate dielectrics with low interface trap density (D_{it}). In addition, heavily-doped source/drain (S/D) regions are required for adequate carrier supply and for low S/D access resistance given roadmap-compliant (~20-50 nm) S/D contact pitch. MOSFETs with heavily-doped S/D regions can be formed by first growing an N+ S/D contact layer above the channel and subsequently recess etching through this layer in the region where the gate will be placed [1]-[3]. To be viable in VLSI at the 8-22 nm nodes, this recess etch would need to provide ~0.5-2 nm precision depth control within gate openings of 8-22 nm length. N+ S/D regions can also be formed by epitaxial regrowth [4]-[6], in either a gate-first or a substitutional-gate process. In such devices, performance can be limited by defects at the junction between regrown S/D and the channel, or by damage to the channel surface during regrowth.

Here, we report InGaAs MOSFETs with an N+ source-drain contact layer regrown by molecular beam epitaxy (MBE). These MOSFETs incorporates a 5 nm InGaAs N+ epitaxial cap layer grown above the InGaAs channel. The S/D contact layers are regrown on this cap layer, and the cap layer is then removed in the channel region using digital etch process [3], [7] incorporating UV ozone oxidation and surface stripping in dilute HCl. A device with 65 nm-L_g shows an excellent peak transconductance of ~1.60 mS/μm at V_{ds} = 0.5 V and 120 mV/dec sub-threshold swing (SS) at V_{ds} = 0.05 V.

II. Device Fabrication

The epitaxial layers, grown by MBE, consist of a InP (100) semi-insulating (S. I.) substrate, a 400 nm unintentionally doped (UID) $In_{0.52}Al_{0.48}As$ buffer/barrier layer, a 3 nm Si-doped ($3.9\cdot10^{12}$ /cm^2) $In_{0.52}Al_{0.48}As$ pulse doping layer, a 10 nm $In_{0.53}Ga_{0.47}As$ channel, and a 5 nm Si-doped (4-5$\cdot10^{19}$ /cm^3) $In_{0.53}Ga_{0.47}As$ cap layer. Dummy gates were defined by e-beam lithography using hydrogen silsesquioxane (HSQ) resist and an atomic layer deposition (ALD) Al_2O_3 adhesion layer. Prior to transferring into the MBE chamber, the semiconductor surface was oxidized by UV ozone exposure and then etched in 10:1 deionized water (DI):HCl. Approximately 50 nm Si-doped ($5\cdot10^{19}$ /cm^3) InAs was non-selectively grown on the N+ cap layer. Amorphous InAs growth on top of the dummy gates was removed by a planarization/etch process [8]. Device mesas were defined by wet-etching, and the dummy gates removed in buffered oxide etch (BOE) with Tergitol surfactant. The exposed InGaAs N+ cap layer was etched by 4 cycles of oxidation by UV ozone and surface removal by dilute HCl dip. AFM measurements indicate that the exposed channel surface has 0.15-0.16 nm RMS roughness after the etch. This is comparable to an unprocessed InGaAs surface. Immediately after removing the InGaAs native oxide in BOE, the sample was loaded into the ALD loadlock. 1 nm/4 nm Al_2O_3/HfO_2 (~1.2 nm EOT) gate dielectric was deposited by ALD. The sample was then annealed for 15 minutes at 400 ºC in forming gas. 20 nm/100 nm Ni/Au was thermally deposited as the gate electrode. Subsequently, 20 nm/100 nm Ni/Au was lifted off for source/drain metallization by thermal evaporation. The schematic cross-section of the device is shown in Fig. 1.

III. Results and Discussion

Fig. 2 shows transfer characteristics (I_d-V_{gs} and g_m-V_{gs}) for a device with L_g = 65 nm. The peak transconductance is 1.6 mS/μm at V_{ds} = 0.5 V, while its minimum SS is 120

mV/dec at V_{ds} = 0.05 V. Fig. 3 shows transfer and output characteristics a L_g = 75 nm device. This device exhibits ~1.4 mS/µm peak transconductance at V_{ds} = 0.5 V and ~0.65 mA/µm on-current at V_{gs}-V_{th} = 0.5 V and V_{ds} = 0.5 V, where the threshold voltage is determined to be ~0.15 V from linear extrapolation. From the I_d-V_{ds} plot in Fig. 4, its S/D on-resistance is approximately 300 Ω-µm at V_{gs} = 1.6 V. Fig. 4(a) and (b) show sub-threshold characteristics for both a short channel (L_g = 75 nm) and a long channel (L_g = 535 nm) device. The 75 nm-L_g device shows 124 mV/dec minimum SS at V_{ds} = 0.1 V and 375 mV/V DIBL, whereas a 535 nm-L_g device shows 95 mV/dec minimum SS and <10 mV/dec DIBL at the same V_{ds}.

In comparison with similar substitutional-gate MOSFETs [6] which do not use the recess etch, both the sub-threshold swing and on-state transconductance are considerably improved. The improved sub-threshold swing is strong evidence of decrease D_{it} in the recess-etch sample, suggesting the removal of surface damage associated with processing. Experiments are in progress to determine whether the increased transconductance is be a consequence of removal of this surface damage or of improved S/D access resistivity.

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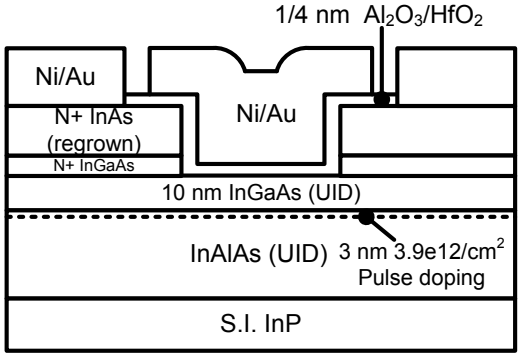

Fig. 1. Schematic cross-section of the substitutional-gate MOSFET.

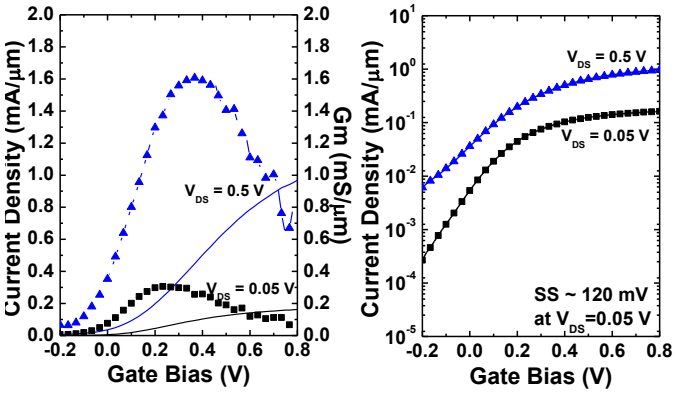

Fig. 2. Transfer (I_d-V_{gs} and g_m-V_{gs}) and sub-threshold (log(I_d)-V_{gs}) characteristics of a 65 nm-L_g device. The device shows an excellent peak transconductance of ~1.60 mS/µm at Vds = 0.5 V and 120 mV/dec at Vgs = 0.05 V.

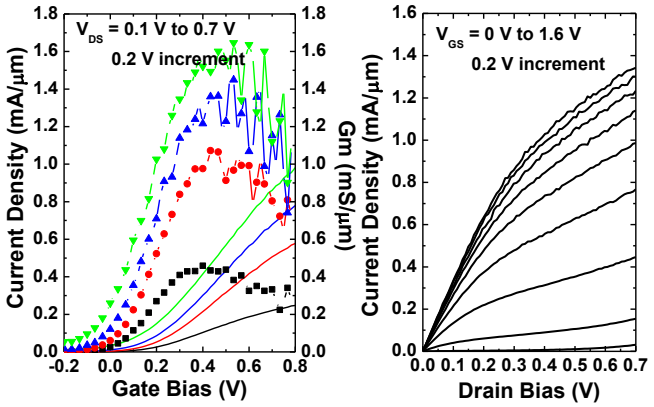

Fig. 3. Transfer (I_d-V_{gs} and g_m-V_{gs}) characteristics and output characteristics (I_d-V_{ds}) of a 75 nm-L_g device. Its on-resistance is extracted to be approximately 300 Ω-µm at V_{gs} = 1.6 V.

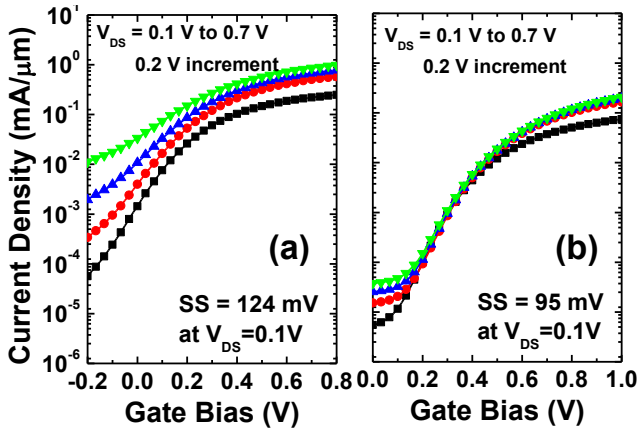

Fig. 4. Sub-threshold (log(I_d)-V_{gs}) characteristics of a short channel device (75 nm-L_g) (a) and a long channel device (535 nm-L_g).