Transistors for THz Systems

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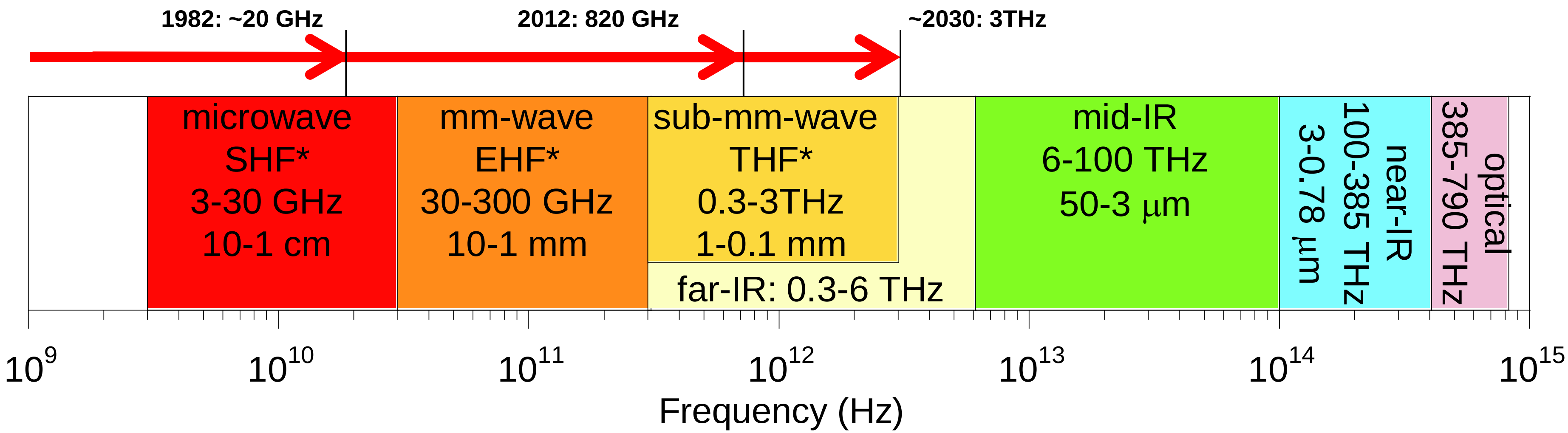
DC to Daylight. Far-Infrared Electronics

How high in frequency can we push electronics ?

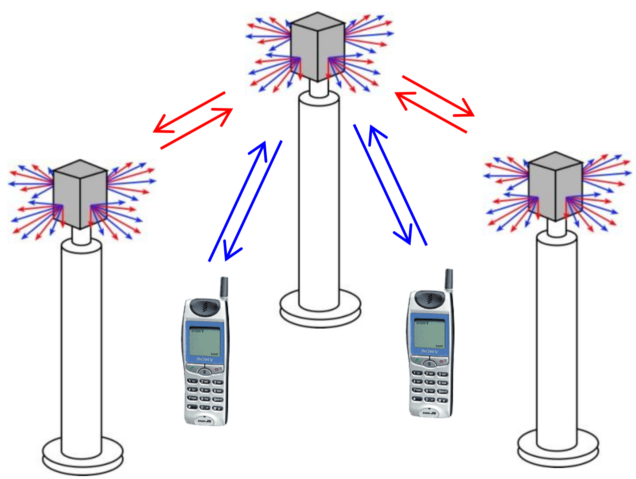
*ITU band designations

** IR bands as per ISO 20473

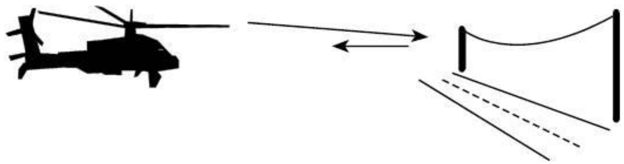


...and what we would be do with it ?

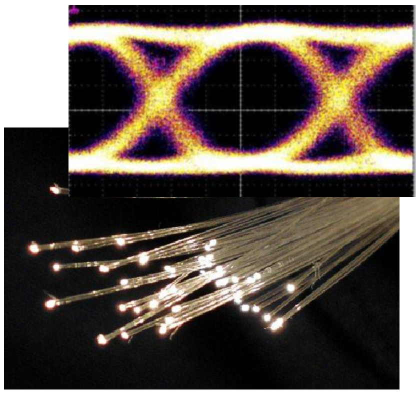
100+ Gb/s wireless networks



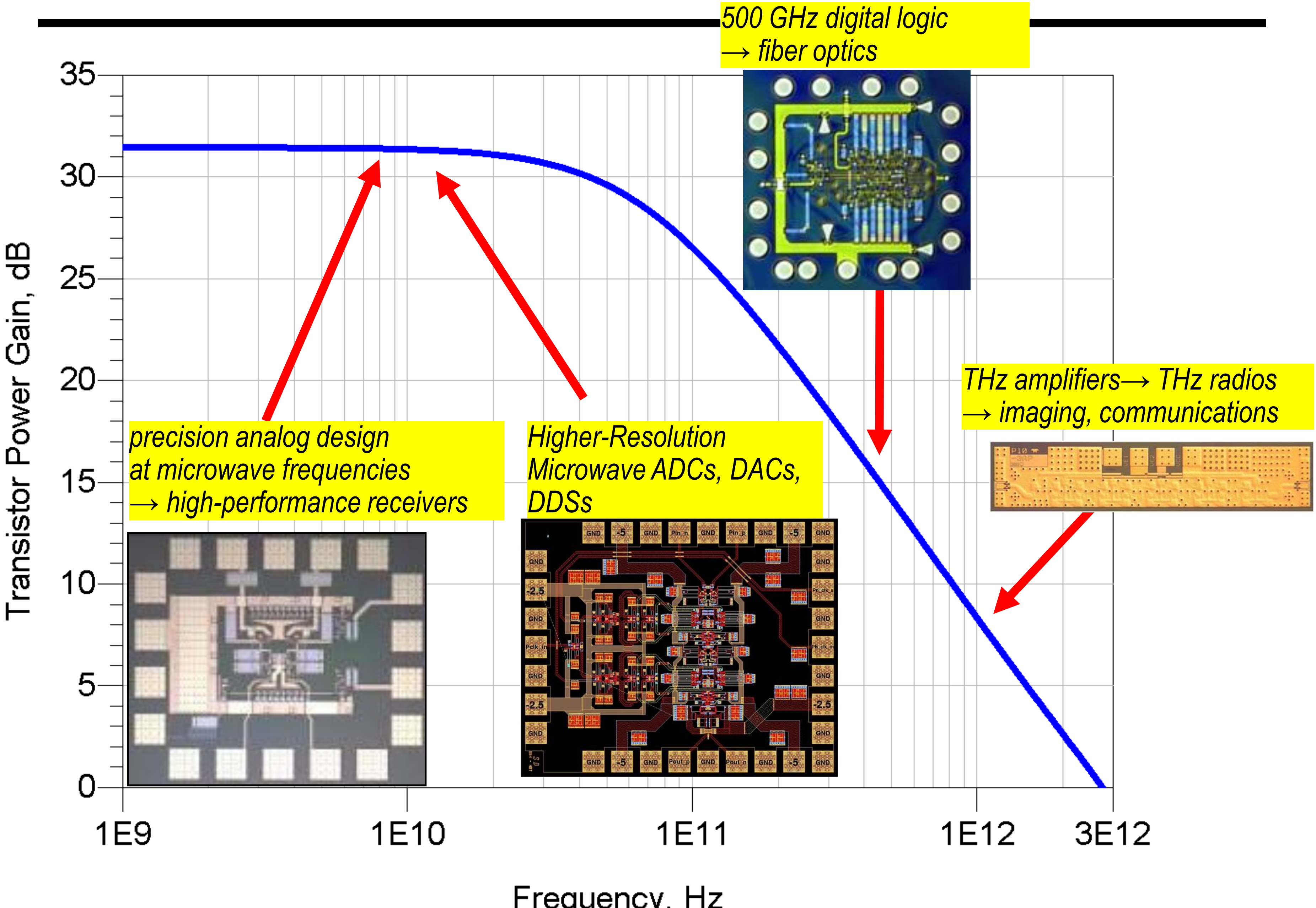
Video-resolution radar
→ fly & drive through fog & rain



near-Terabit optical fiber links

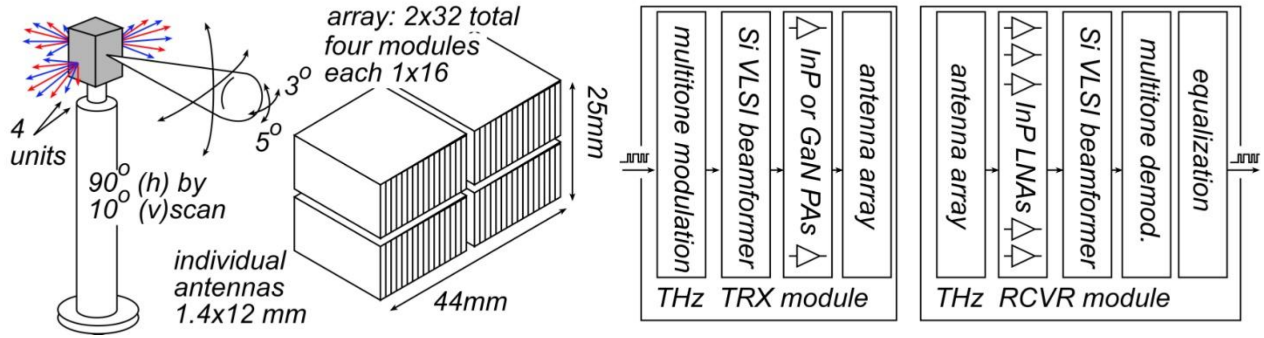


THz Transistors: Not Just For THz Circuits

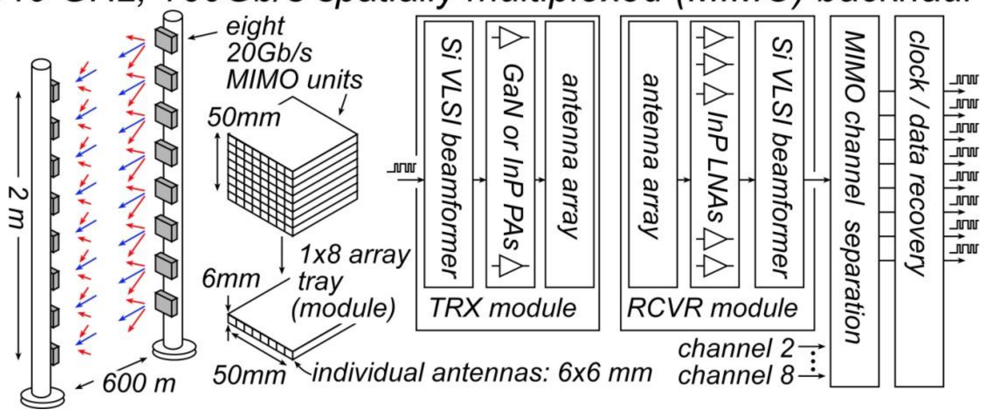


THz Communications Needs High Power, Low Noise

140 GHz, 10 Gb/s spatially scanned network node



340 GHz, 160Gb/s spatially multiplexed (MIMO) backhaul

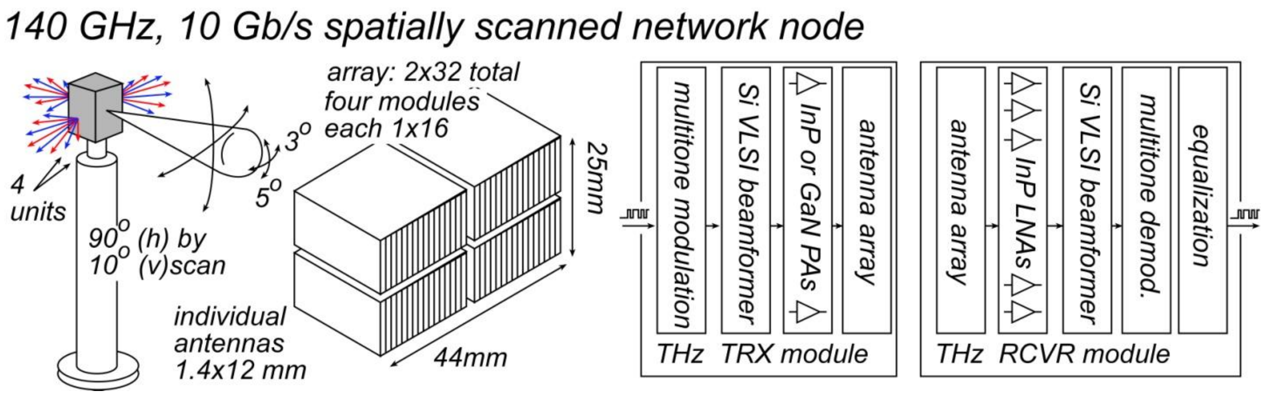


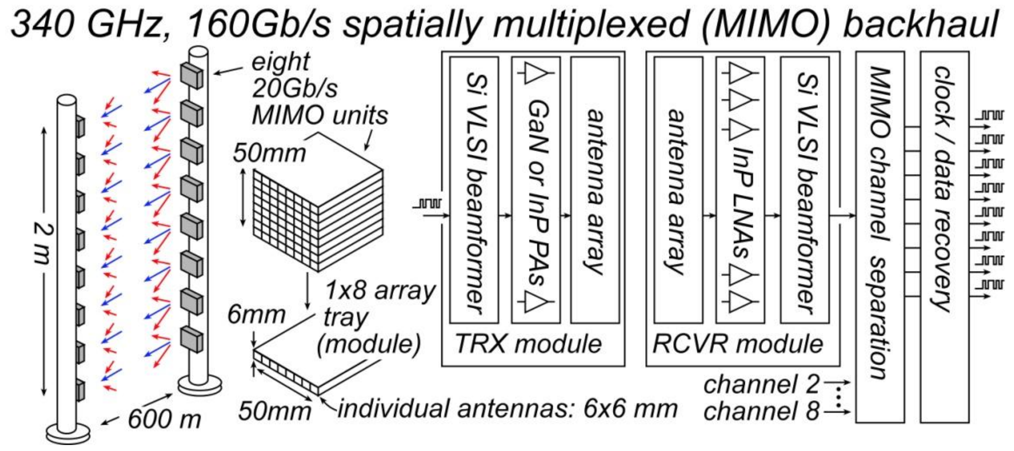
Real systems with real-world weather & design margins, 500-1000m range:

Will require:

3-7 dB Noise figure, 50mW- 1W output/element, 64-256 element arrays
→ InP or GaN PAs and LNAs, Silicon beamformer ICs

THz Communications Needs High Power, Low Noise



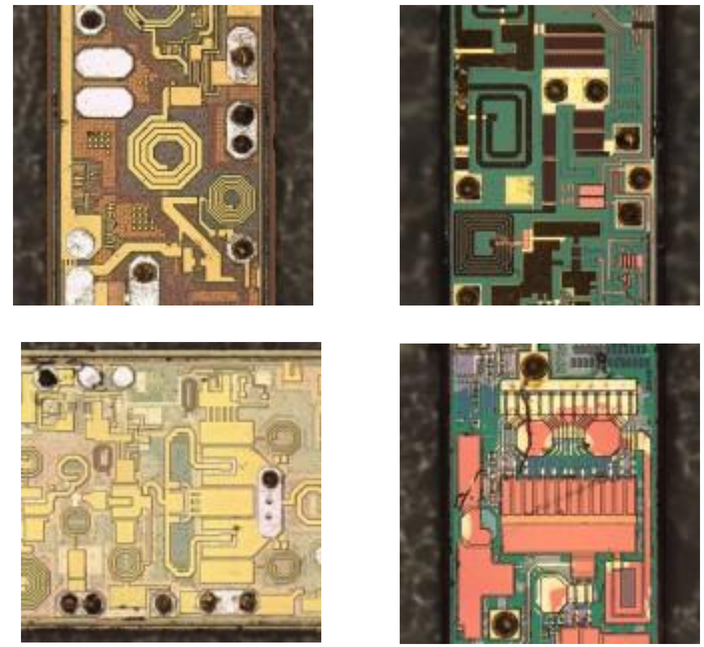


Real systems→ LNAs with low Fmin, PAs with high Psat & high PAE

Comparing technologies

InP HEMTs give the best noise. InP HBT & GaN HEMT compete for the PA.
CMOS is great for signal processing, but noise, power, PAE are poor.
Harmonic generation is low power, inefficient. Harmonic mixing is noisy.

III-V PAs and LNAs in today's wireless systems...

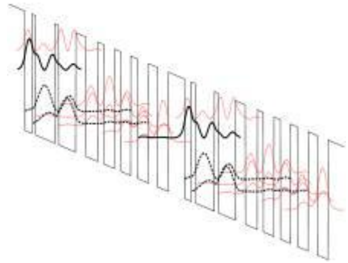


http://www.chipworks.com/blog/recentteardowns/2012/10/02/apple-iphone-5-the-rf/

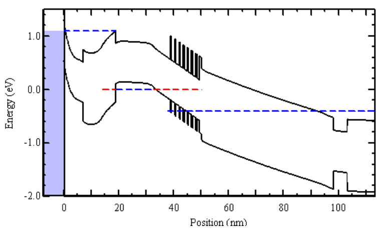
THz Device Scaling

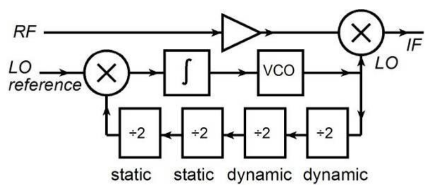
nm Transistors, Far-Infrared Integrated Circuits

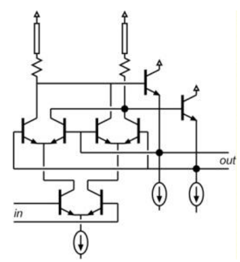
IR today→ lasers & bolometers → generate & detect

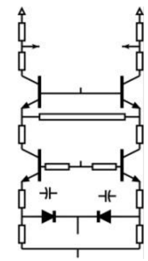


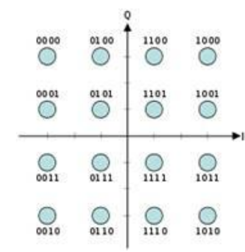
Far-infrared ICs: classic device physics, classic circuit design









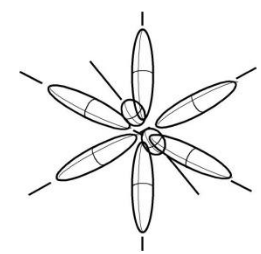


It's all about the interfaces: contact and gate dielectrics...

...wire resistance,...

...heat,...

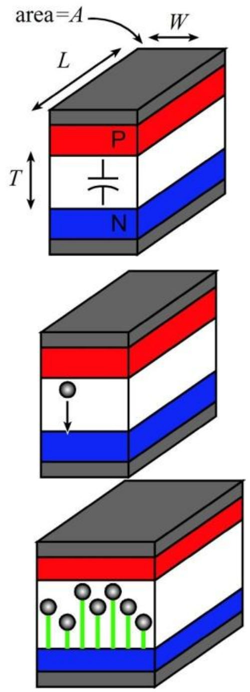
...& charge density.



band structure and density of states !

Transistor scaling laws: (V,I,R,C,t) vs. geometry

Depletion Layers

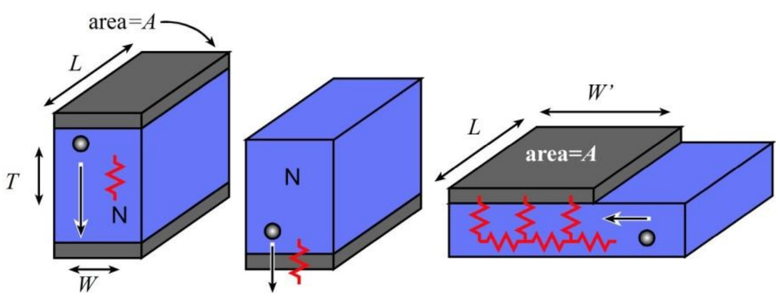


$$C = \varepsilon \cdot \frac{A}{T}$$

$$\tau = \frac{T}{2v}$$

$$\frac{I_{\max}}{A} = \frac{4\varepsilon v_{sat}(V_{appl} + \phi)}{T^2}$$

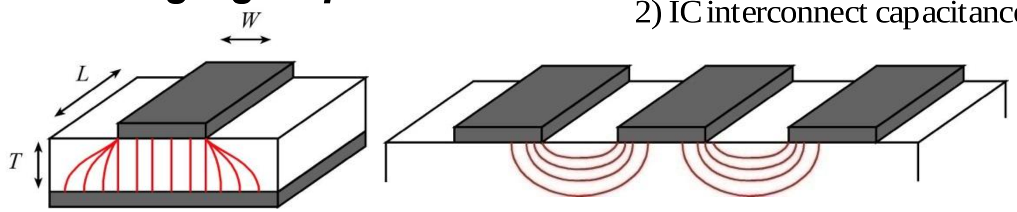
Bulk and Contact Resistances



$R \cong \rho_{contact} / A$ contact terms dominate

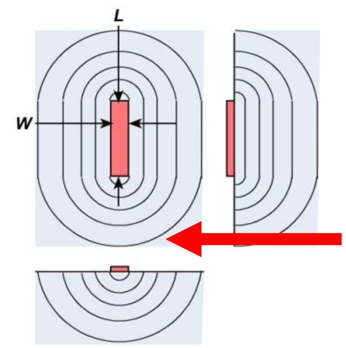
Fringing Capacitances

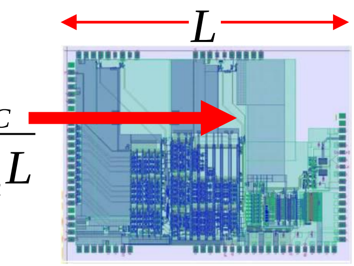
1) FET fringing capacitances
2) IC interconnect capacitances



$C_{finging} / L \sim \varepsilon$ $C_{finging} / L \sim \varepsilon$

Thermal Resistance

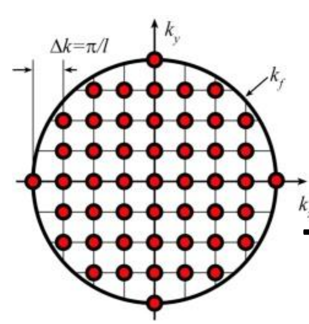


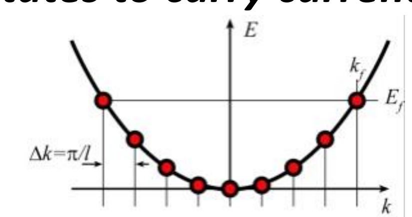


$$\Delta T_{IC} \propto \frac{P_{IC}}{K_{th} L}$$

$$\Delta T_{\text{transistor}} \sim \frac{P}{\pi K_{th} L} \ln\left(\frac{L}{W}\right)$$

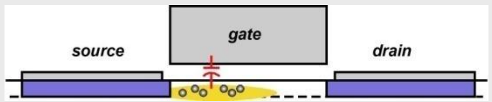
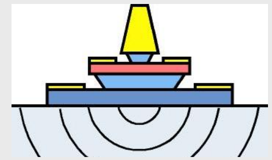
Available quantum states to carry current

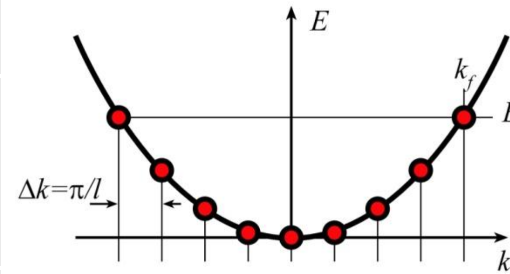


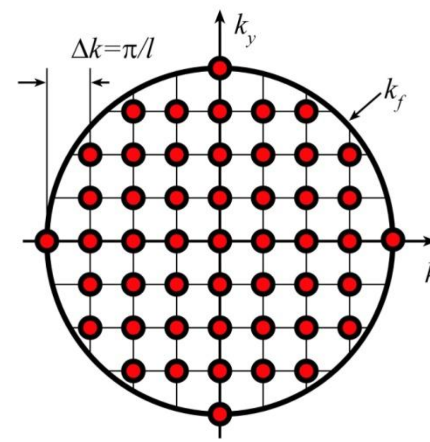


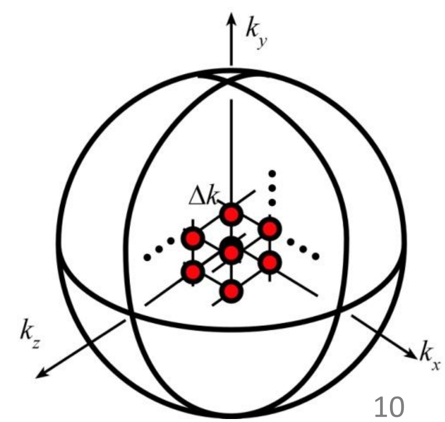
→ ***capacitance,***
transconductance
contact resistance

THz & nm Transistors: State Density Limits

	2-D: FET	3-D: BJT
		
capacitance	$C_{DOS} = \frac{q^2 m^*}{2\pi\hbar^2}$	
current	$J_{sheet} = \frac{2^{3/2} q^{5/2} (m^*)^{1/2} V^{3/2}}{3\pi^2\hbar^2}$	$J = \frac{q^3 m^* V^2}{4\pi^2\hbar^3}$
conductivity	$\sigma_c = \left(\frac{q^2}{\hbar}\right)\cdot\left(\frac{2}{\pi^3}\right)^{1/2}\cdot n^{1/2}$	$\sigma_c = \left(\frac{q^2}{\hbar}\right)\cdot\left(\frac{3}{8\pi}\right)^{2/3}\cdot n^{2/3}$

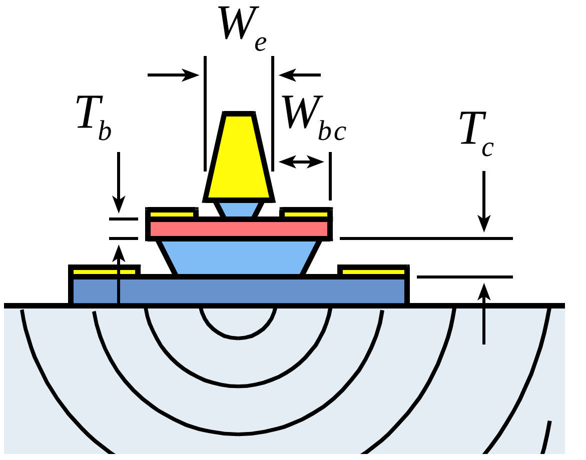






# of available quantum states / energy
- **determines FET channel capacitance**
- **FET and bipolar transistor current**
- **access resistance of Ohmic contact**

Bipolar Transistor Design



$\left(\text{emitter length } L_E\right)$

$$\tau_b \approx T_b^2 / 2D_n$$

$$\tau_c = T_c / 2v_{sat}$$

$$C_{cb} = \varepsilon A_c / T_c$$

$$I_{c,\max} \propto v_{sat} A_e \left(V_{\text{ce,operating}} + V_{\text{ce,punch-through}}\right) / T_c^2$$

$$\Delta T \propto \frac{P}{L_E}\left[1 + \ln\left(\frac{L_e}{W_e}\right)\right]$$

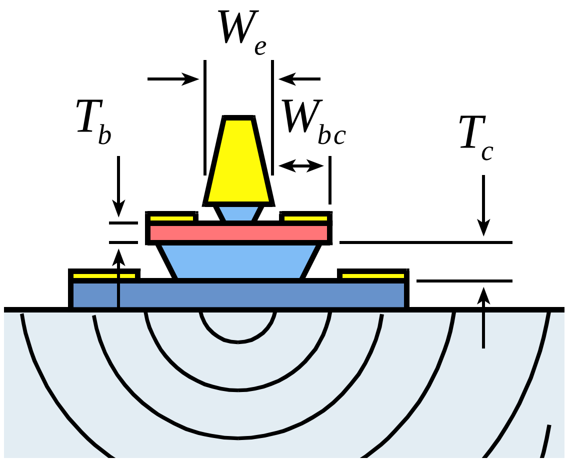
$$R_{ex} = \rho_{\text{contact}} / A_e$$

$$R_{bb} = \rho_{\text{sheet}}\left(\frac{W_e}{12L_e} + \frac{W_{bc}}{6L_e}\right) + \frac{\rho_{\text{contact}}}{A_{\text{contacts}}}$$

Bipolar Transistor Design: Scaling

$$\tau_b \approx T_b^2 / 2D_n$$

$$\tau_c = T_c / 2v_{sat}$$



(emitter length L_E)

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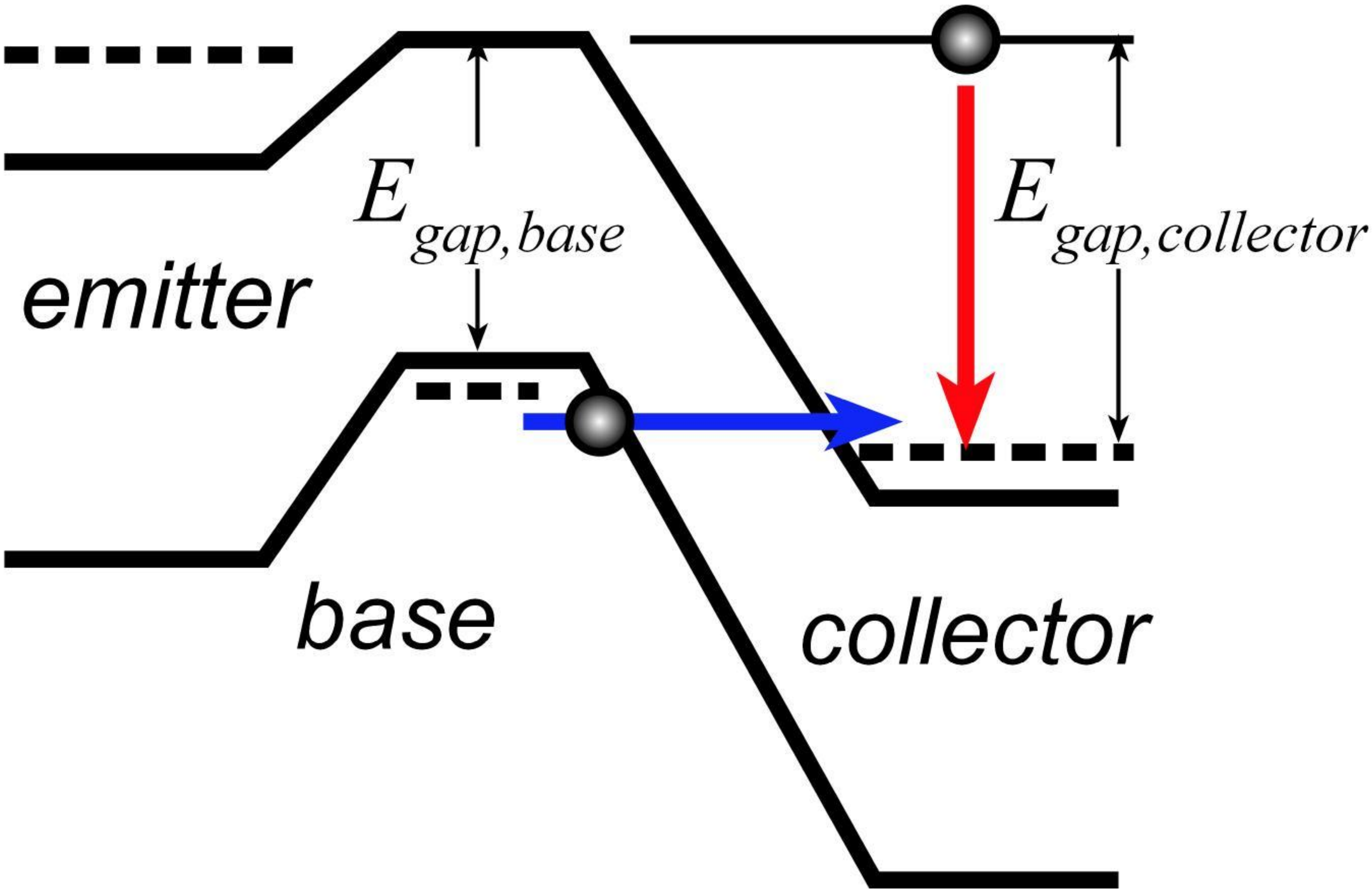
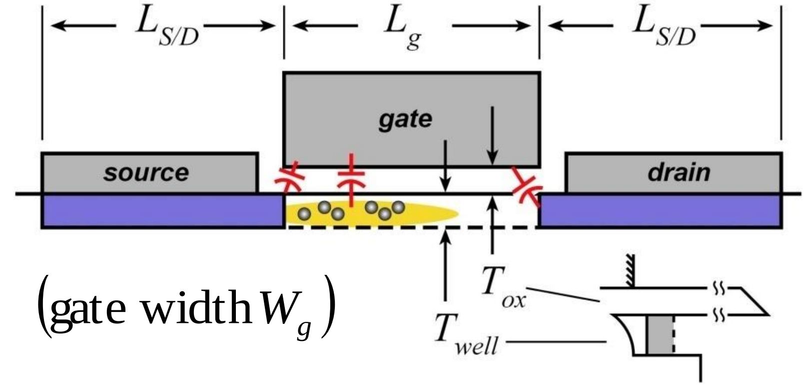
Breakdown: Never Less than the Bandgap



band-band tunneling: base bandgap
impact ionization: collector bandgap

FET Design



$$C_{gd} \cong C_{gs,f} \cong \varepsilon W_g$$

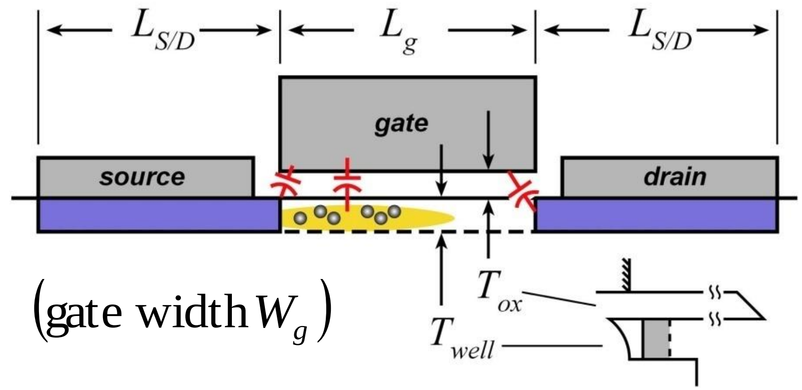
$$g_m = C_{g-ch} \cdot (v / L_g)$$

$$C_{g-ch} = \frac{L_g W_g}{T_{ox}/\varepsilon_{ox} + T_{\text{well}}/2\varepsilon_{\text{well}} + (q^2/\text{well state density})}$$

$$v \propto \begin{pmatrix} \text{voltage division ratio between} \\ \text{the above three capacitors} \end{pmatrix}^{-1/2} \cdot \frac{1}{\sqrt{\text{transport mass}}}$$

$$R_{DS} \approx L_g /(W_g v \varepsilon) \qquad R_S = R_D = \frac{\rho_{\text{contact}}}{L_{\text{S/D}} W_g}$$

FET Design: Scaling



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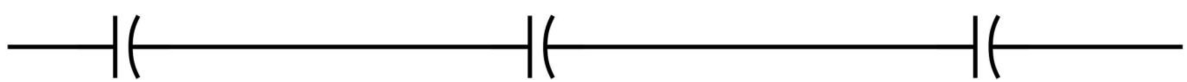

$$v \propto \left(\begin{array}{c} \text{voltage division ratio between} \\ \text{the above three capacitors} \end{array} \right)^{-1/2} \cdot \frac{1}{\sqrt{\text{transport mass}}}$$

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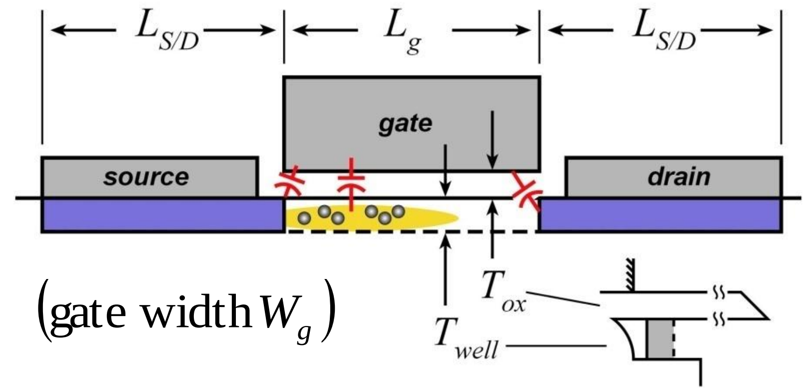
FET Design: Scaling



2:1 ↓ $$C_{gd} \cong C_{gs,f} \cong \varepsilon W_g$$ 2:1 ↓

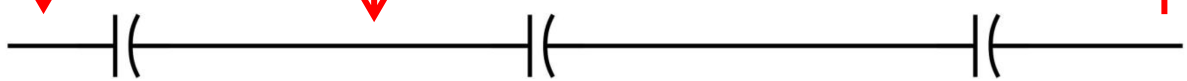
constant, 2:1 ↓, 2:1 ↓

$$g_m = C_{g-ch} \cdot (v / L_g)$$

2:1 ↓, 2:1 ↓, 2:1 ↓

$$C_{g-ch} = \frac{L_g W_g}{T_{ox}/\varepsilon_{ox} + T_{well}/2\varepsilon_{well} + (q^2/\text{well state density})}$$

2:1 ↓, 2:1 ↓, 2:1 ↑



$$v \propto \left(\begin{array}{c} \text{voltage division ratio between} \\ \text{the above three capacitors} \end{array} \right)^{-1/2} \cdot \frac{1}{\sqrt{\text{transport mass}}}$$

constant, constant, constant

constant

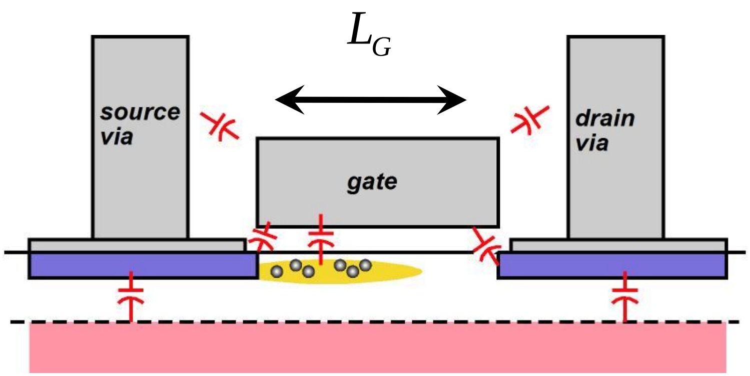
$$R_{DS} \approx L_g / (W_g v \varepsilon)$$

2:1 ↓, 2:1 ↓

$$R_S = R_D = \frac{\rho_{contact}}{L_{S/D} W_g}$$

constant, 4:1 ↓, 2:1 ↓, 2:1 ↓

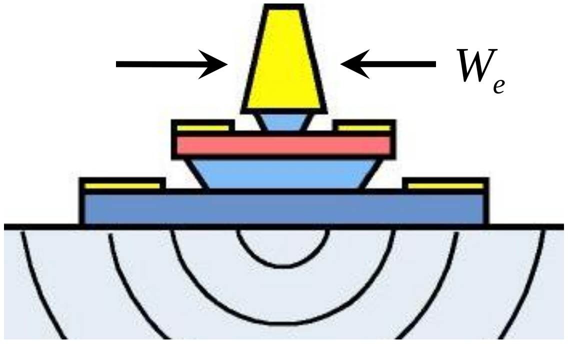
Changes required to double transistor bandwidth



$(\text{gate width } W_G)$

FET parameter	change
gate length	decrease 2:1
current density (mA/μm), g_m (mS/μm)	increase 2:1
transport effective mass	constant
channel 2DEG electron density	increase 2:1
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
channel thickness	decrease 2:1
channel density of states	increase 2:1
source & drain contact resistivities	decrease 4:1

fringing capacitance does not scale → linewidths scale as (1 / bandwidth)



$(\text{emitter length } L_E)$

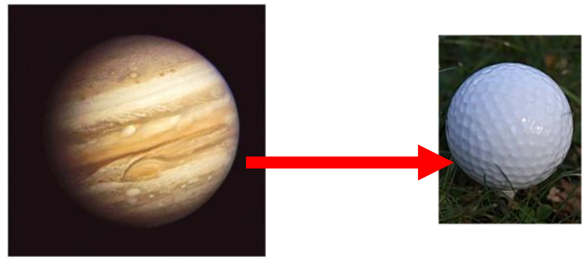
HBT parameter	change
emitter & collector junction widths	decrease 4:1
current density (mA/μm^2)	increase 4:1
current density (mA/μm)	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1

constant voltage, constant velocity scaling

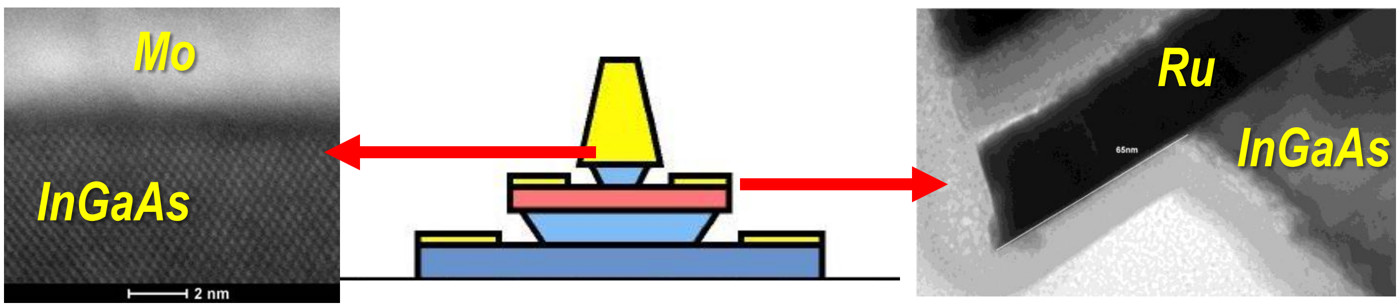
nearly constant junction temperature → linewidths vary as (1 / bandwidth)^2

THz & nm Transistors: what needs to be done

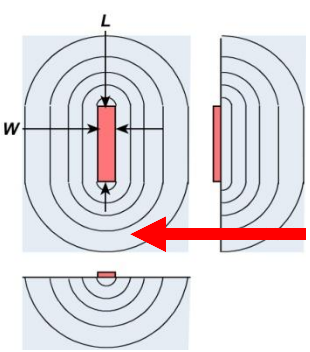
Metal-semiconductor interfaces (Ohmic contacts): <u>very low resistivity</u>
Dielectric-semiconductor interfaces (Gate dielectrics---FETs only): <u>thin !</u>



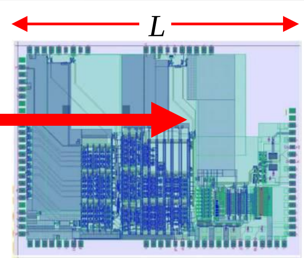
Ultra-low-resistivity (~0.25 Ω-μm^2), ultra shallow (1 nm), ultra-robust (0.2 A/μm^2) contacts



Heat

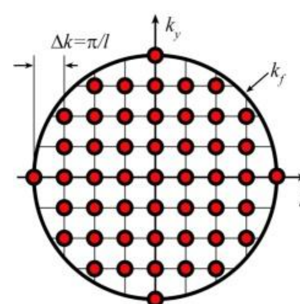


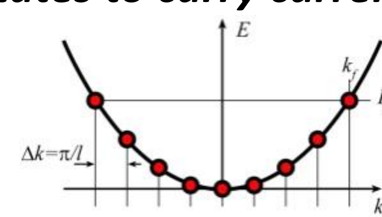
$$\Delta T_{IC} \propto \frac{P_{IC}}{K_{th} L}$$



$$\Delta T_{\text{transistor}} \sim \frac{P}{\pi K_{th} L} \ln\left(\frac{L}{W}\right)$$

Available quantum states to carry current





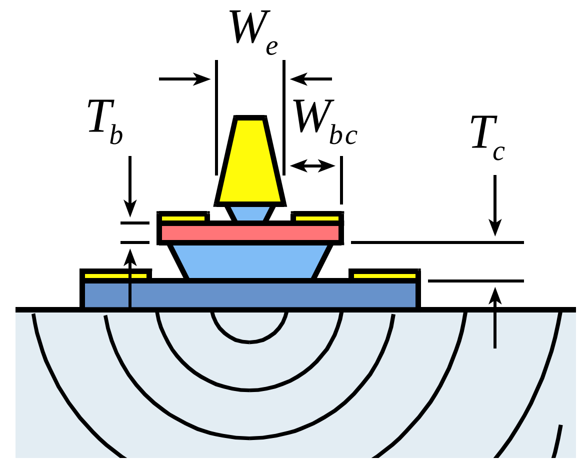
→ *capacitance, transconductance contact resistance*

THz InP HBTs

Scaling Laws, Scaling Roadmap

scaling laws: to double bandwidth

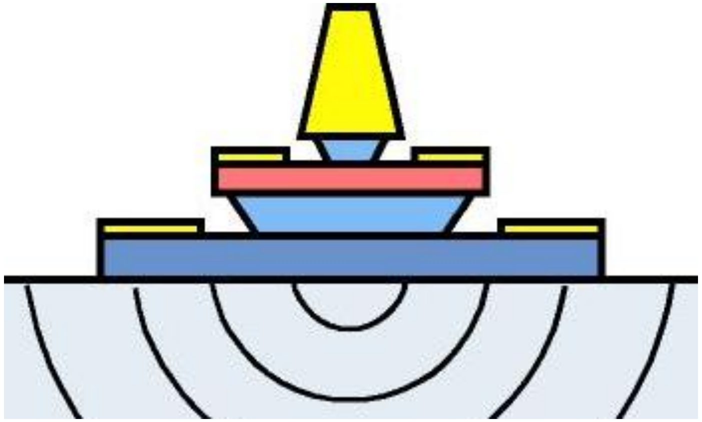
HBT parameter	change
emitter & collector junction widths	decrease 4:1
current density (mA/μm²)	increase 4:1
current density (mA/μm)	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1



$(\text{emitter length } L_E)$

emitter	128	64	32 nm width
	4	2	1 $\Omega\cdot\mu m^2$ access ρ
base	120	60	30 nm contact width,
	5	2.5	1.25 $\Omega\cdot\mu m^2$ contact ρ
collector	75	53	37.5 nm thick,
	18	36	72 mA/μm^2 current density
	3.3	2.75	2-2.5 V, breakdown
f_τ	730	1000	1400 GHz
f_{max}	1300	2000	2800 GHz
RF-ICs	660	1000	1400 GHz
digital divider	330	480	660 GHz

HBT Fabrication Process Must Change... Greatly



32 nm width base & emitter contacts...self-aligned

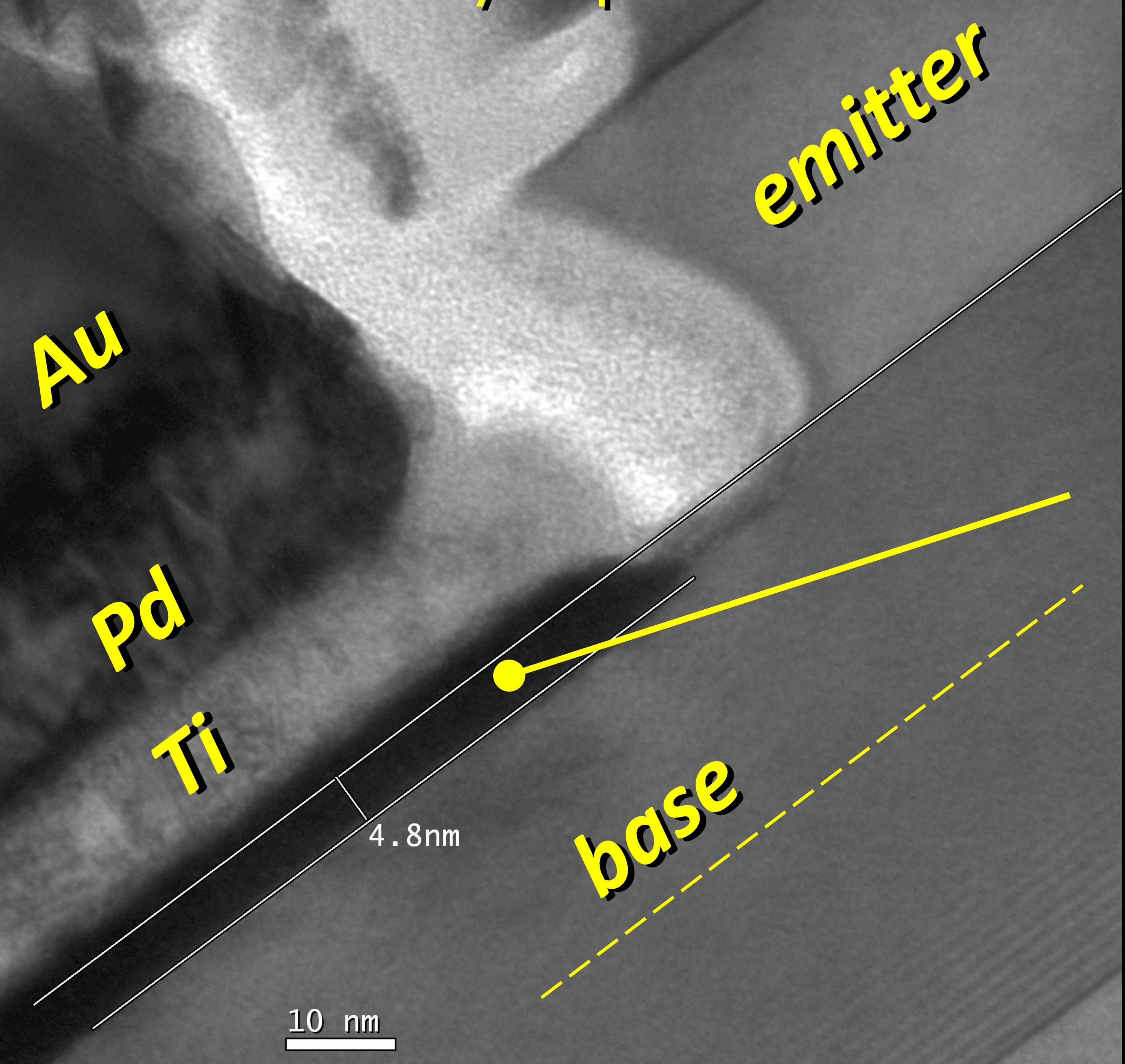
32 nm width emitter semiconductor junctions

Contacts:

1 Ω-μm^2 resistivities
70 mA/μm^2 current density
~1 nm penetration depths
→ refractory contacts

nm III-V FET, Si FET processes have similar requirements

Needed: Greatly Improved Ohmic Contacts

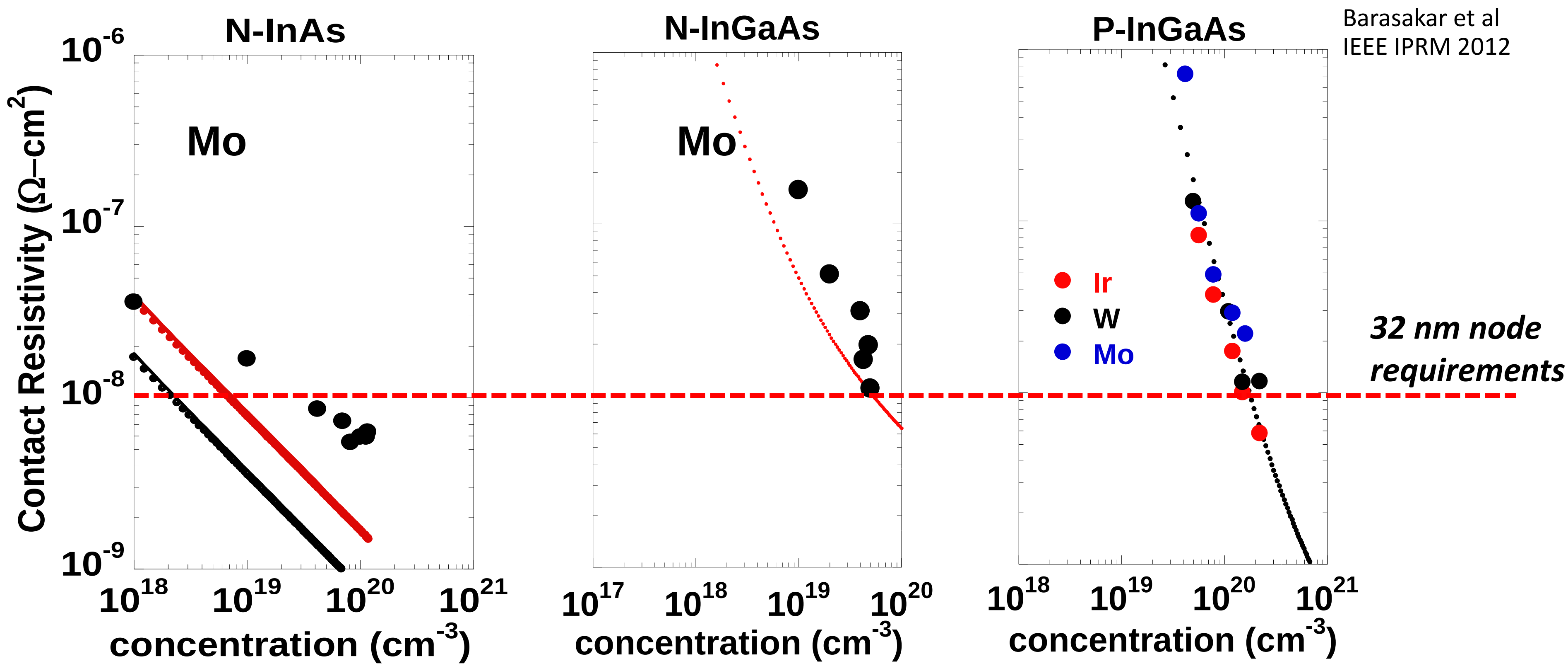


Pt/Ti/Pd/Au

~5 nm
Pt contact
penetration

(into 25 nm base)

Ultra Low-Resistivity Refractory Contacts



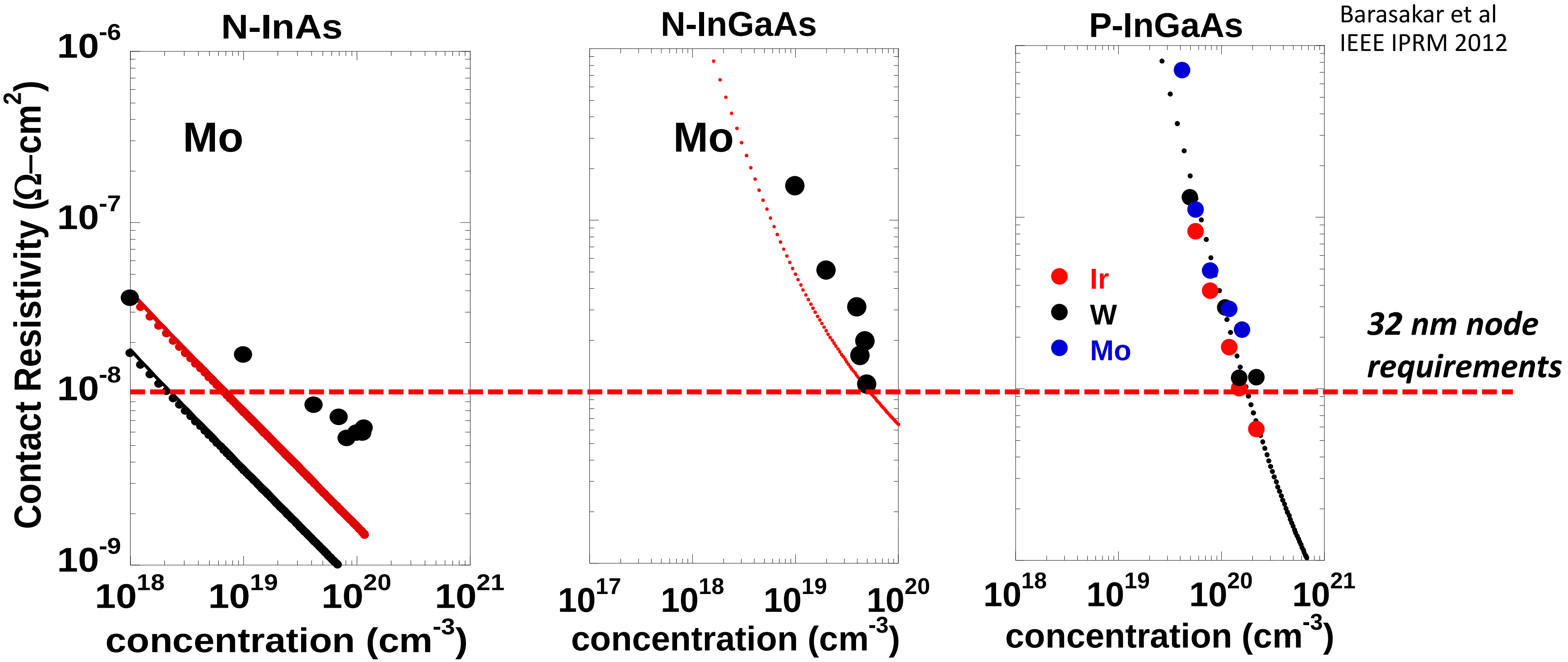
In-situ: avoids surface contaminants

Refractory: robust under high-current operation

Low penetration depth, ~ 1 nm

Contact performance sufficient for 32 nm /2.8 THz node.

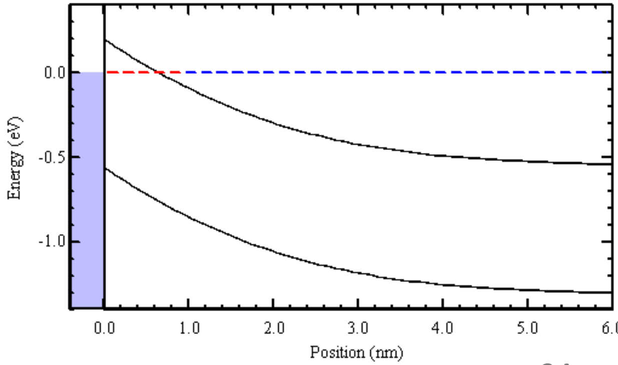
Ultra Low-Resistivity Refractory Contacts



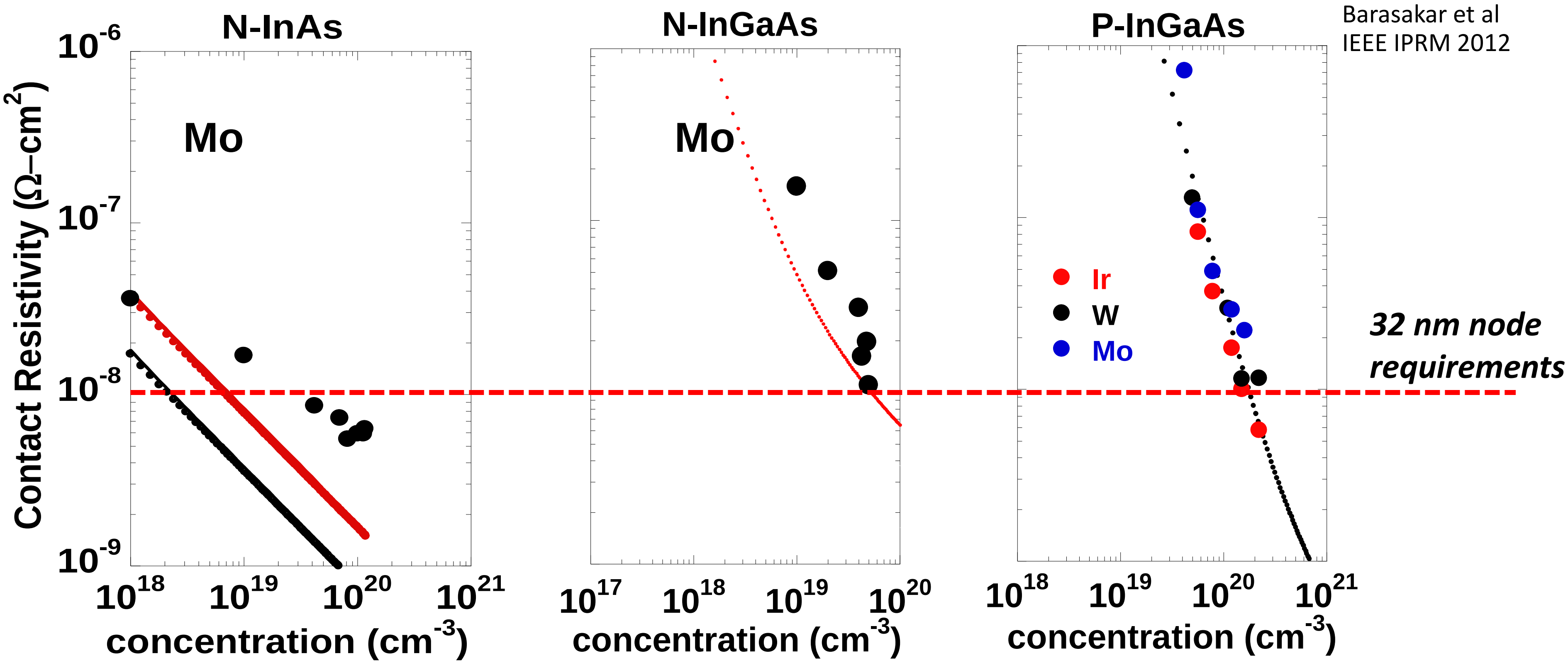
Schottky Barrier is about one lattice constant

what is setting contact resistivity ?

what resistivity should we expect ?



Ultra Low-Resistivity Refractory Contacts



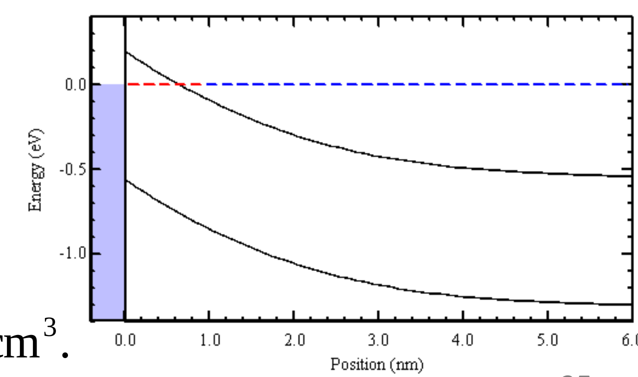
Zero-barrier contact resistivity: (state density and quantum-reflectivity limit)

$$\rho_c = \left(\frac{\hbar}{q^2}\right)\cdot\left(\frac{8\pi}{3}\right)^{2/3}\cdot\frac{1}{T^2}\cdot\frac{1}{n^{2/3}}$$

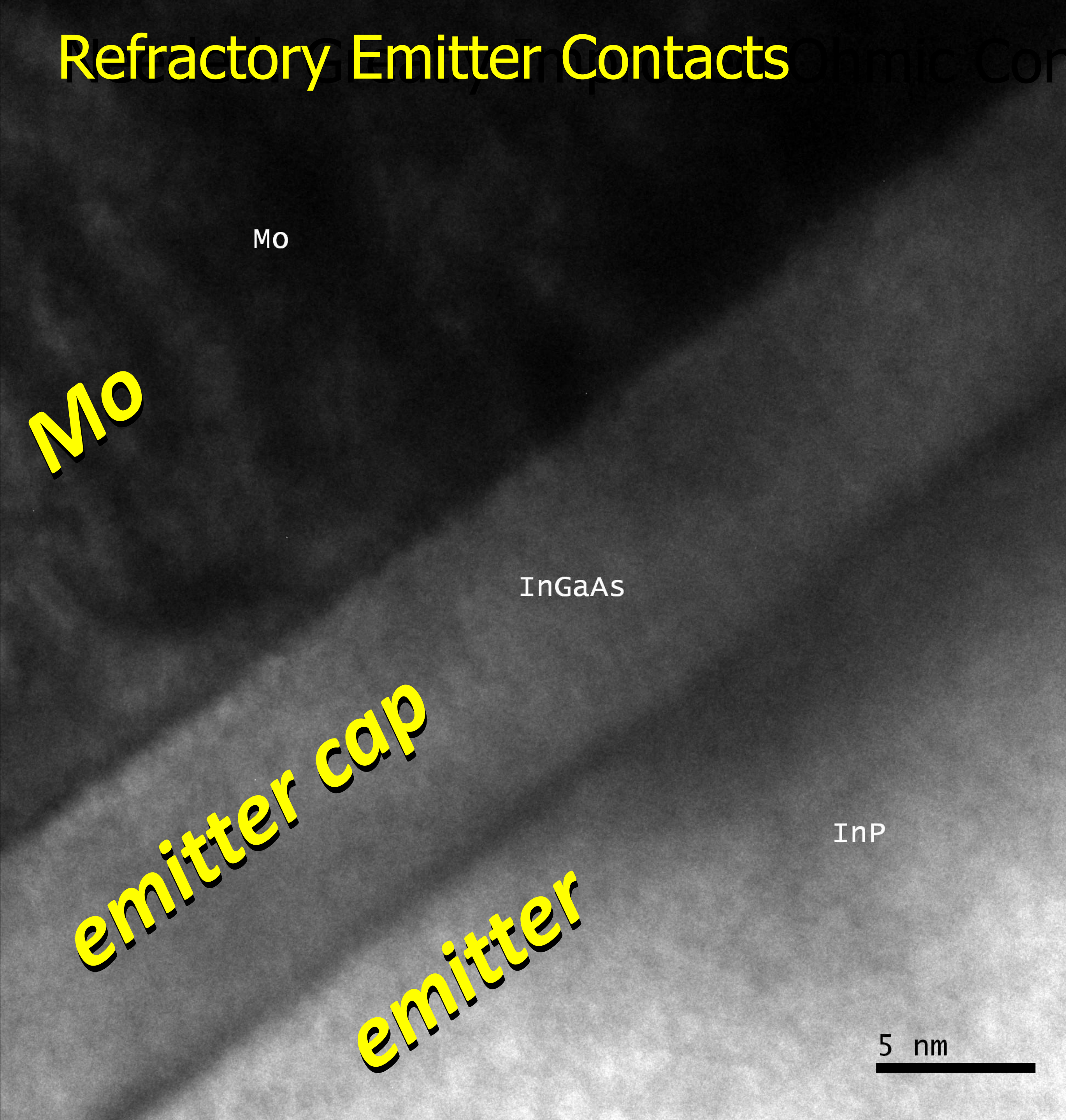
n = carrier concentration

T = transmission coefficient

$\rho_c \cong 0.1\,\Omega-\mu\text{m}^2$ at $n = 7\cdot10^{19}/\text{cm}^3$.



Refractory Emitter Contacts



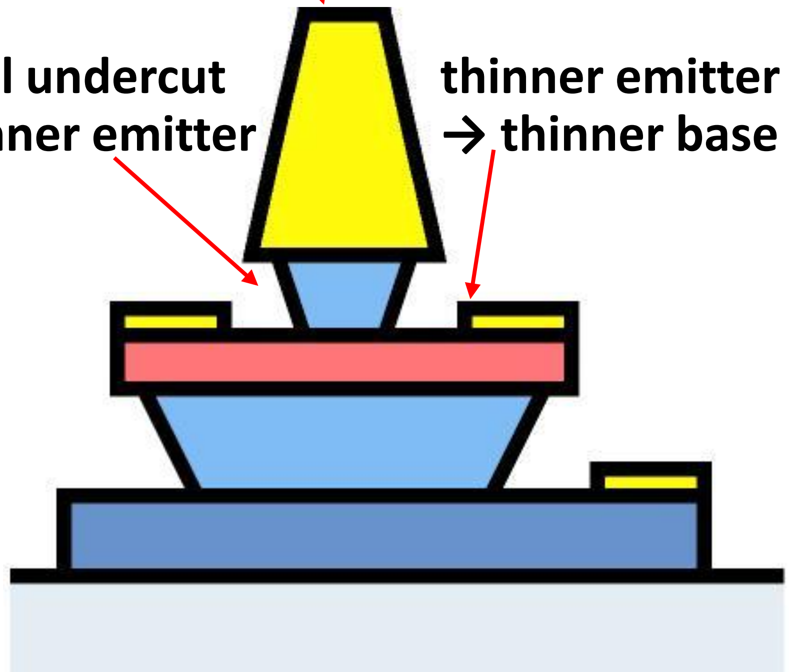
negligible penetration

HBT Fabrication Process Must Change... Greatly

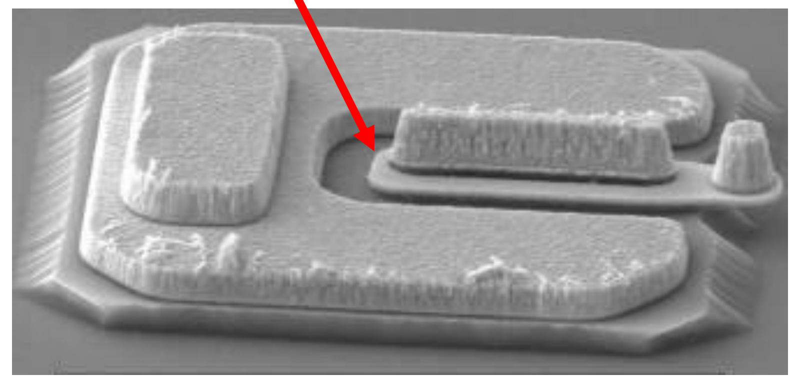
tall, narrow contacts: liftoff fails !

control undercut
→ thinner emitter

thinner emitter
→ thinner base metal

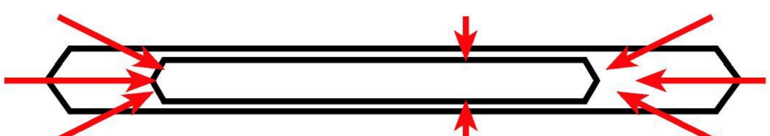


thinner base metal
→ excess base metal resistance

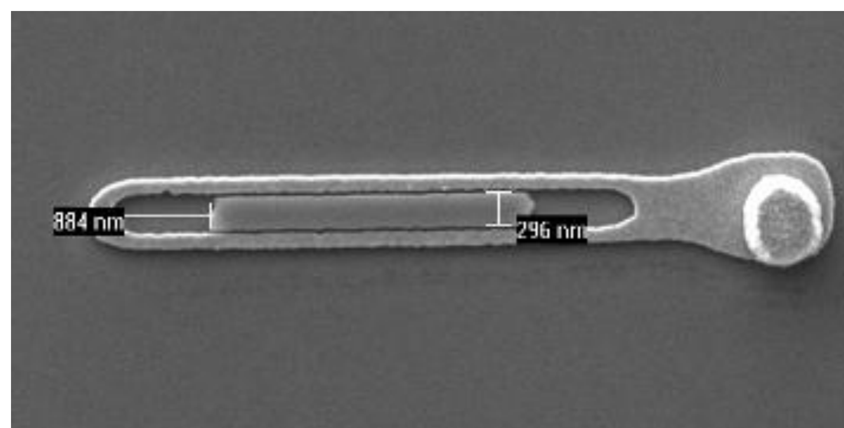


Undercutting of emitter ends

{101}A planes: fast



{111}A planes: slow



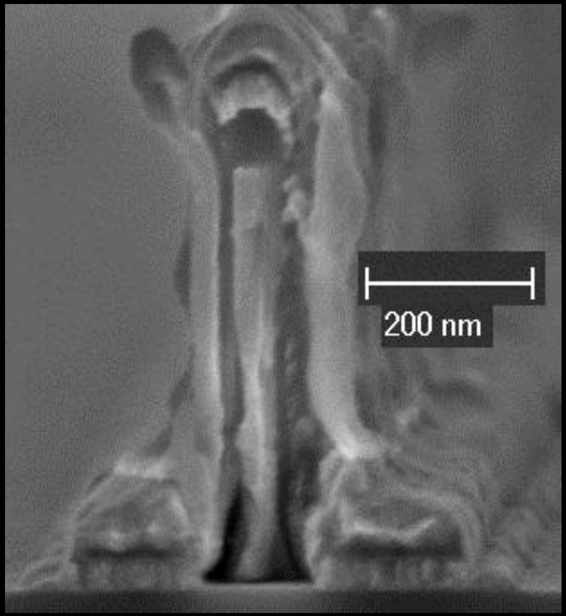
Sub-200-nm Emitter Contact & Post

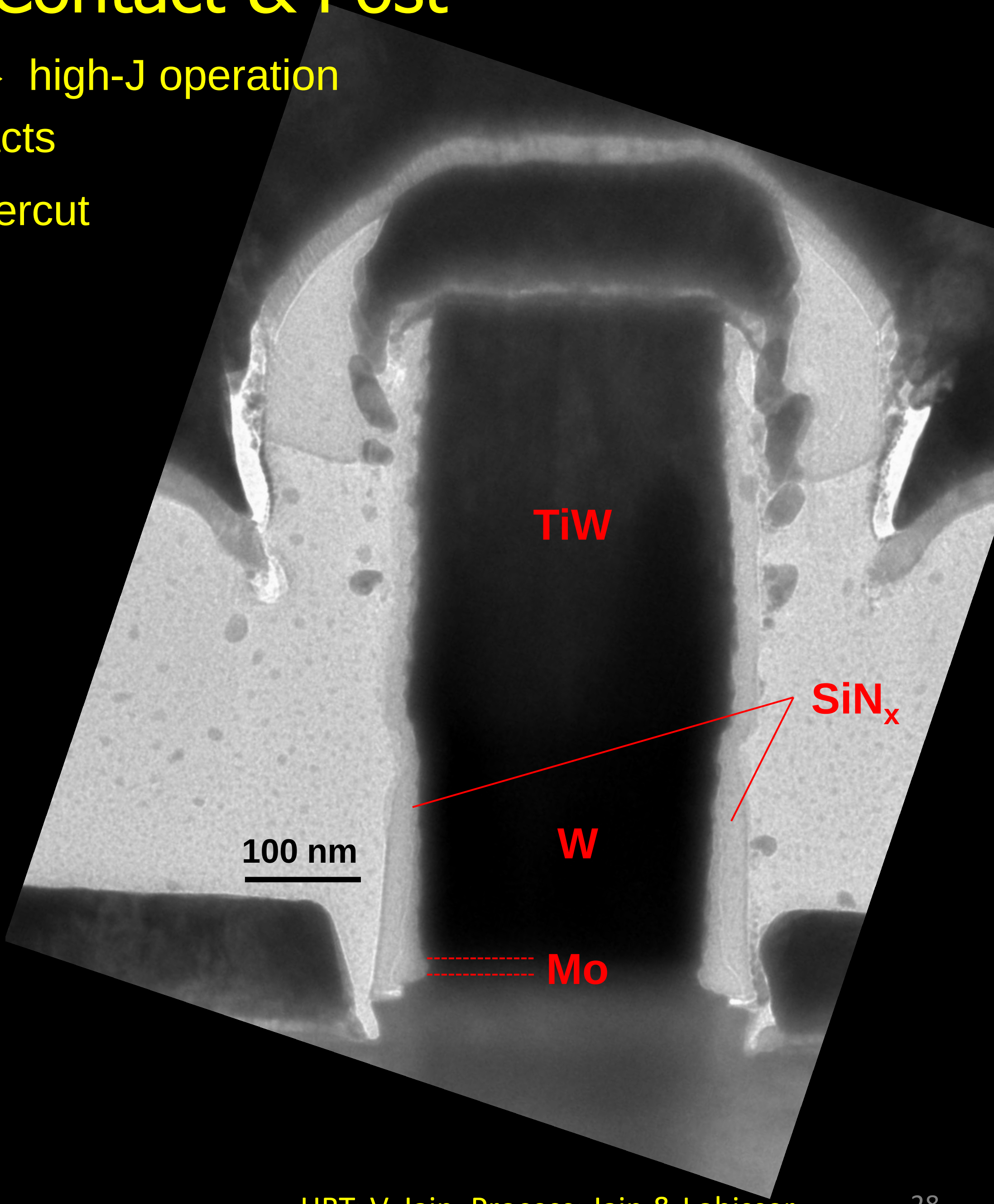
Refractory contact, refractory post→ high-J operation

Sputter+dry etch→ 50-200nm contacts

Liftoff aided by TiW/W interface undercut

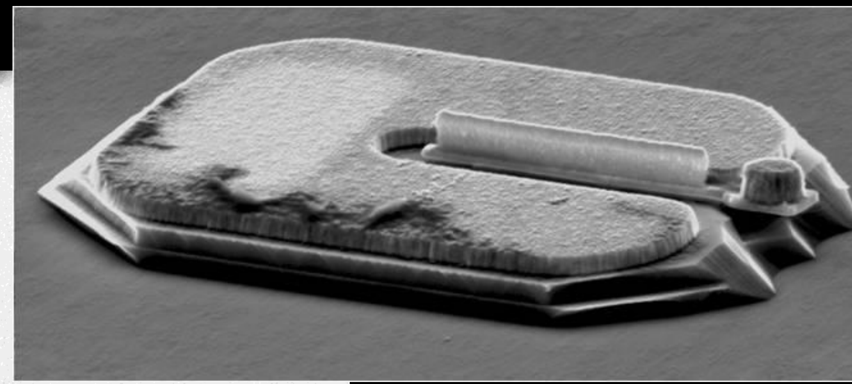
Dielectric sidewalls

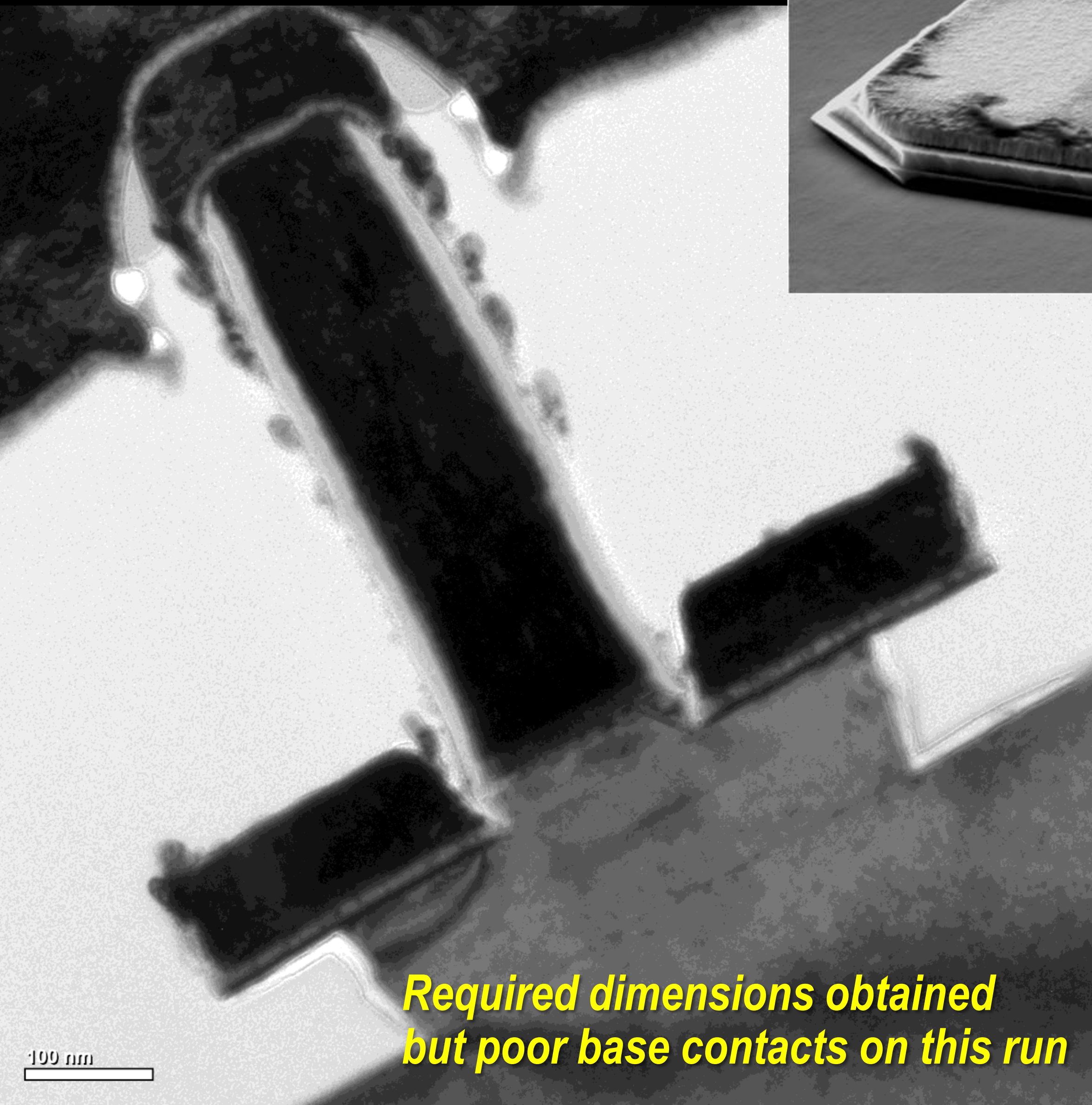


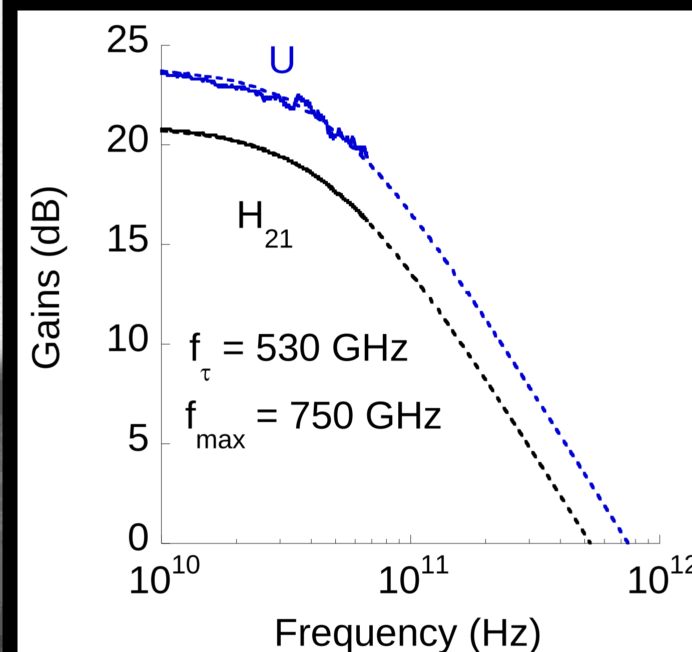


HBT: V. Jain. Process: Jain & Lobisser

RF Data: 25 nm thick base, 75 nm Thick Collector



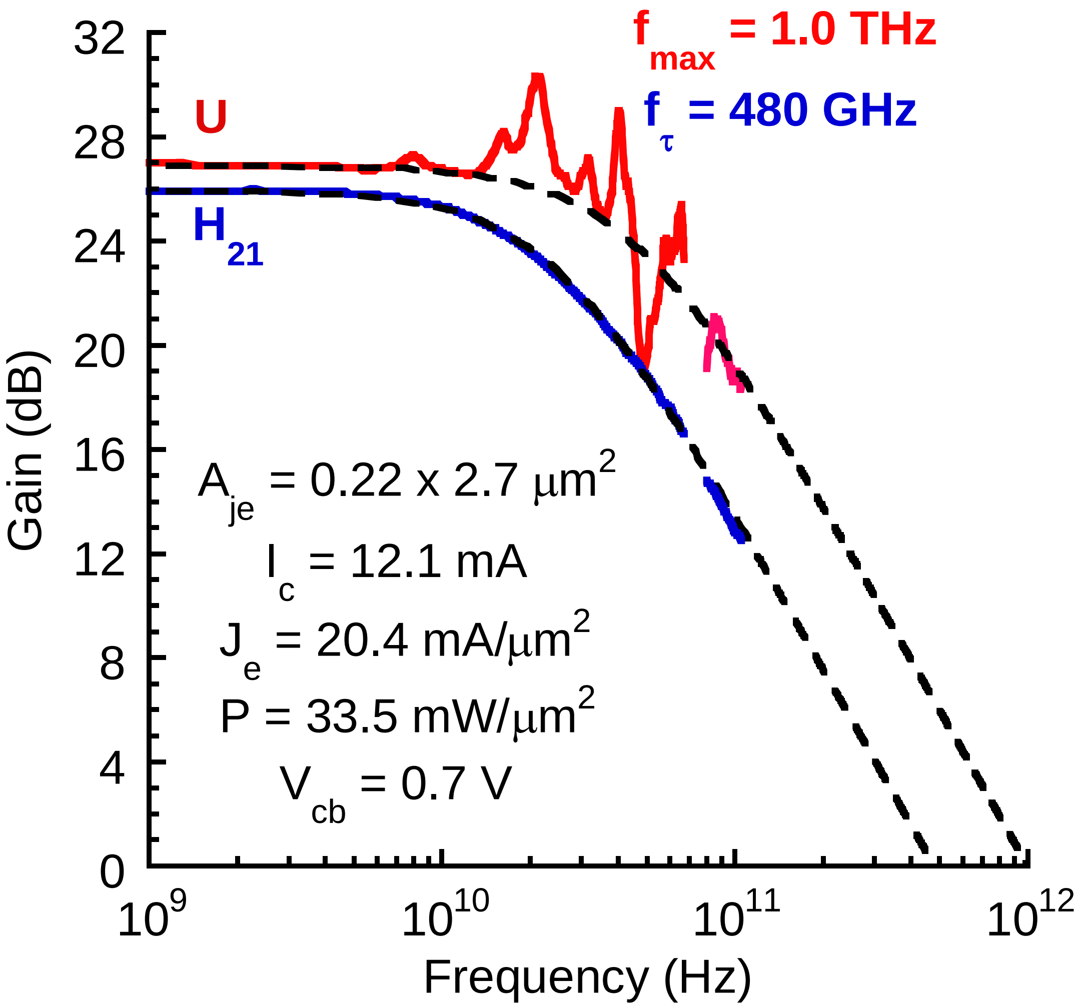




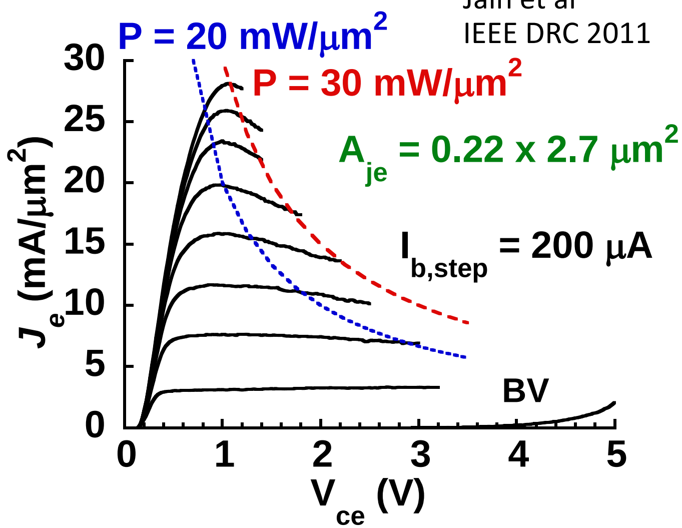
Required dimensions obtained but poor base contacts on this run

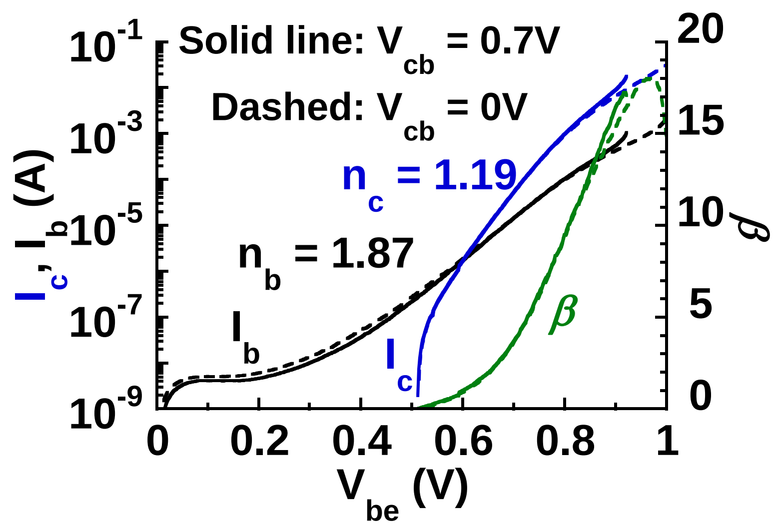
E. Lobisser, ISCS 2012, August, Santa Barbara

DC, RF Data: 100 nm Thick Collector



Jain et al
IEEE DRC 2011





THz InP HBTs From Teledyne

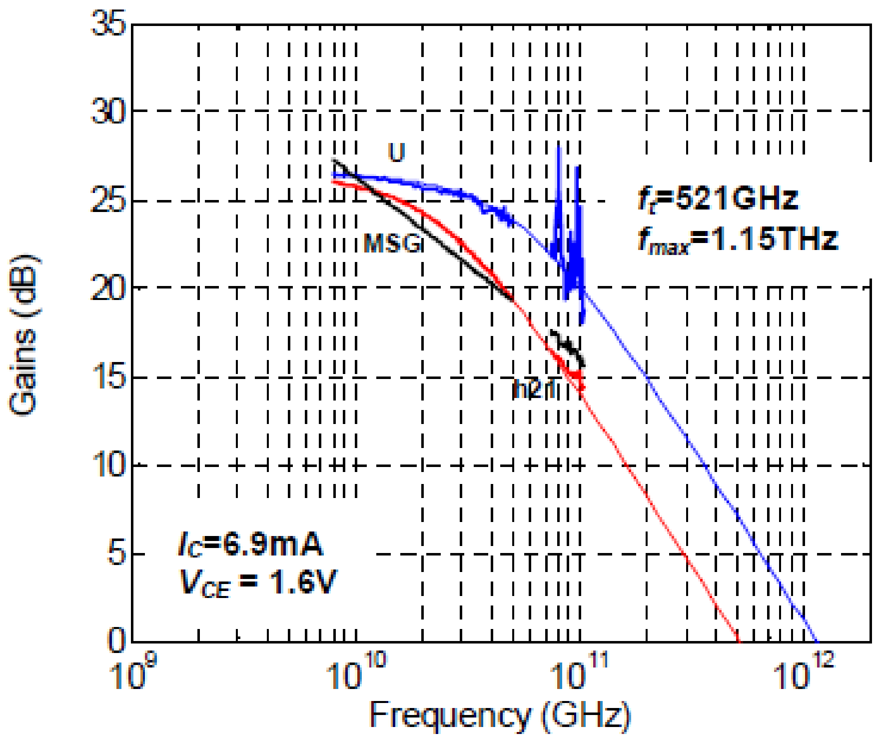


Fig. 3 RF gains of 0.13x2μm^2 HBT

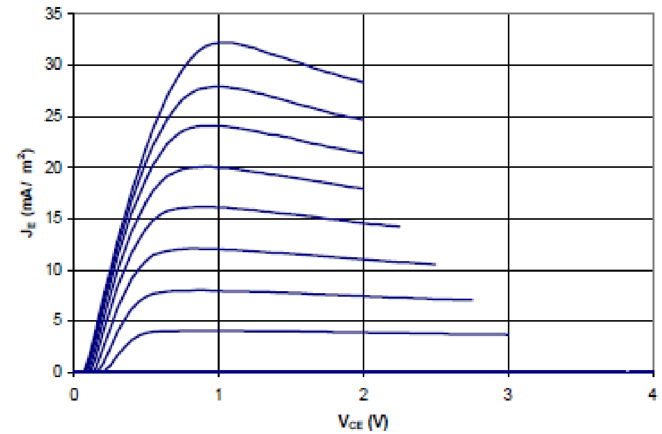


Fig. 2 Common-emitter IV characteristics of 130nm HBT normalized to emitter area

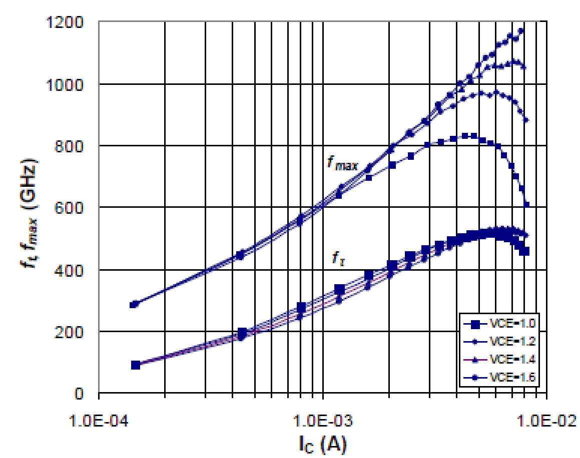


Fig. 4 f_t and f_{max} versus collector current at varying values of V_{CE} for 0.13x2μm^2 HBT

130nm InP DHBTs with f_t>0.52THz and f_{max} >1.1THz

M. Urteaga[1], R. Pierson[1], P. Rowell[1], V. Jain[2], E. Lobisser[2], M.J.W. Rodwell[2]
[1]Teledyne Scientific Company, Thousand Oaks, CA 93160. [2]Department of ECE, University of California, Santa Barbara, CA 93106. E-mail: murteaga@teledyne-si.com

TELEDYNE SCIENTIFIC COMPA A Teledyne Technologies Comp

Urteaga et al, DRC 2011, June

Towards & Beyond the 32 nm /2.8 THz Node

Base contact process:

Present contacts too resistive (4Ω–μm²)

Present contacts sink too deep (5 nm) for target 15 nm base

→ ***refractory base contacts***

Emitter Degeneracy:

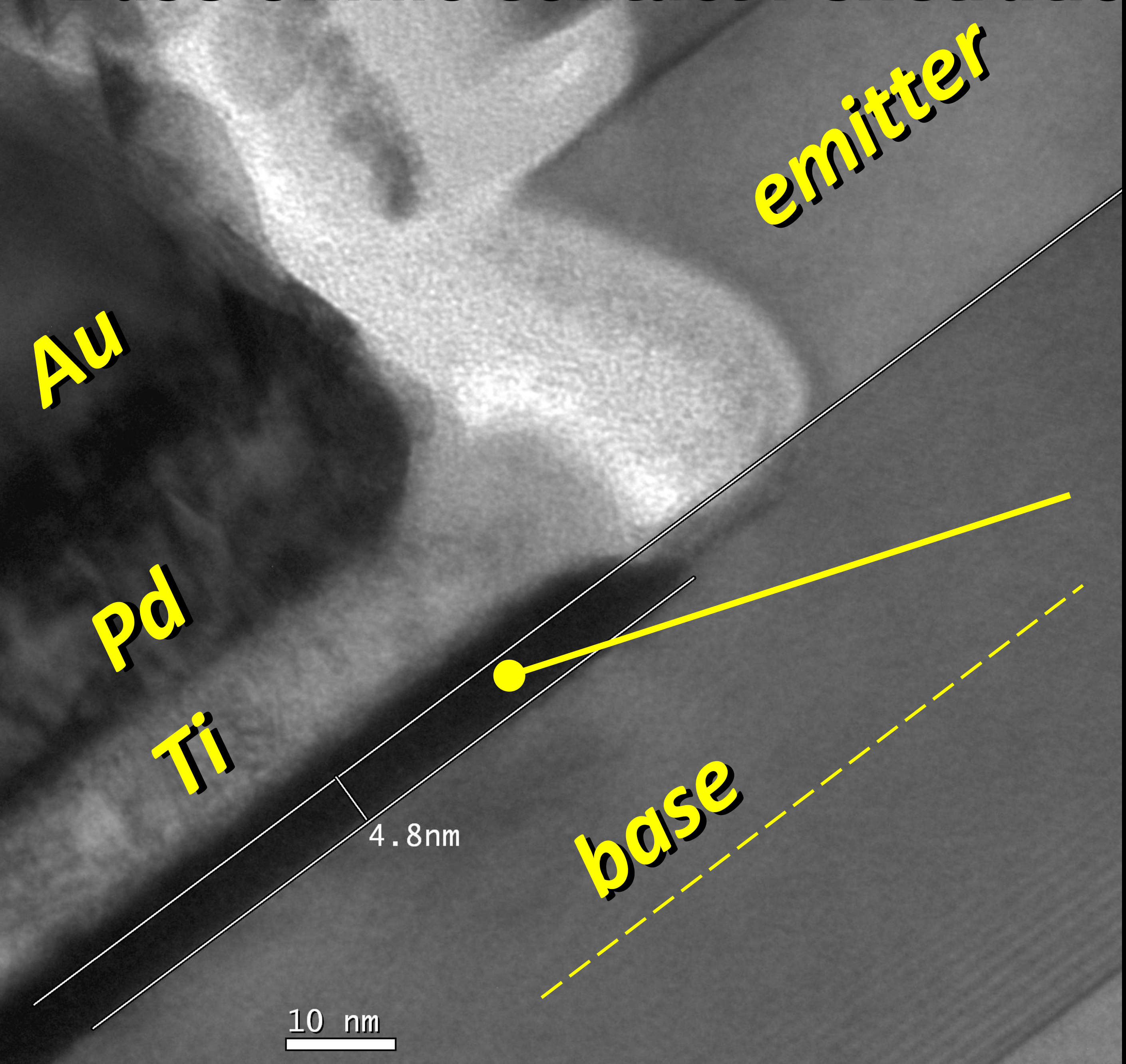
Target current density is almost 0.1 Amp/μm² (!)

Injected electron density becomes degenerate.

transconductance is reduced.

→ ***Increased electron mass in emitter***

Base Ohmic Contact Penetration

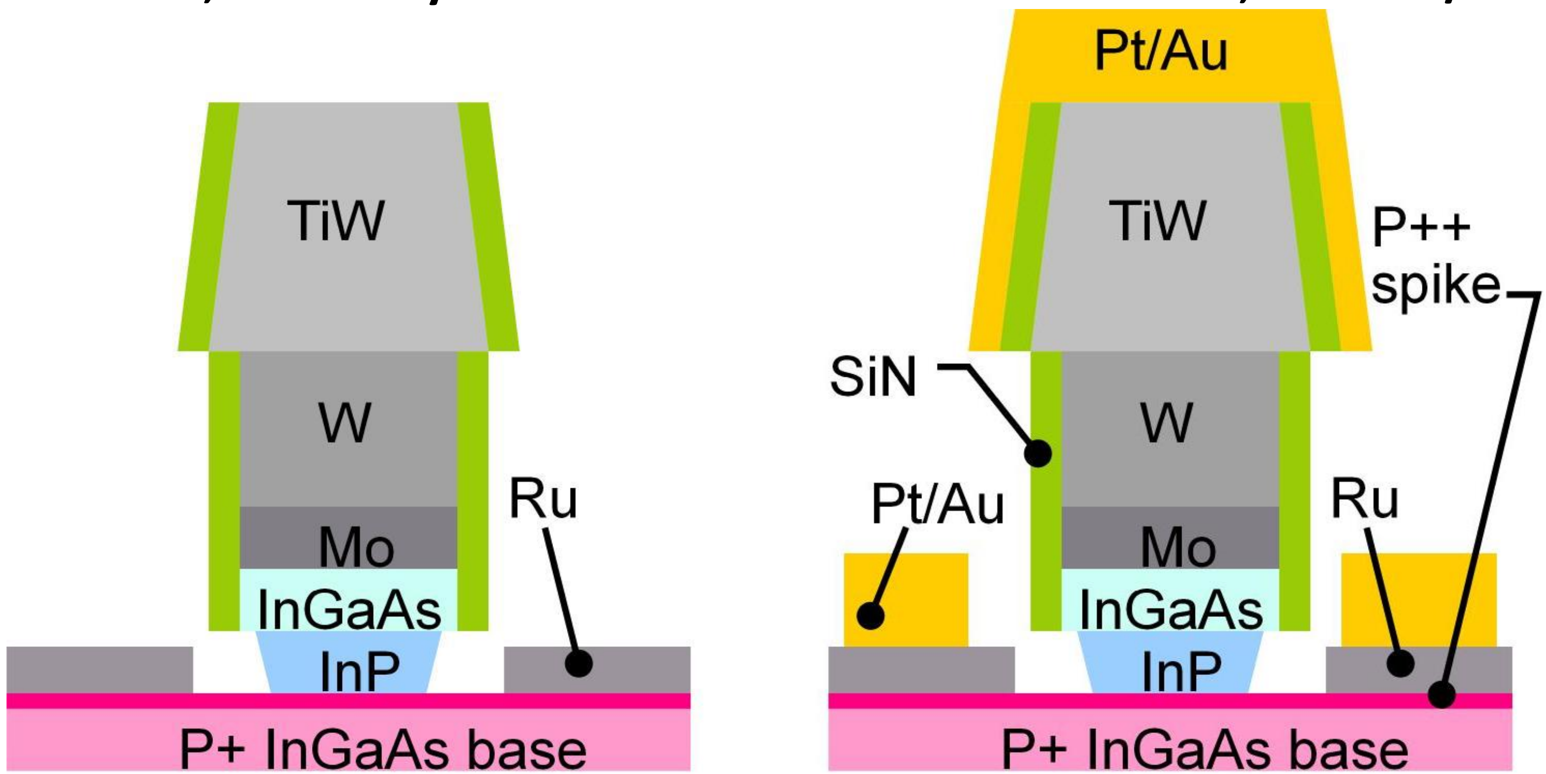


~5 nm
Pt contact
penetration

(into 25 nm base)

Refractory Base Process (1)

Blanket liftoff; refractory base metal | **Patterned liftoff; Thick Ti/Au**

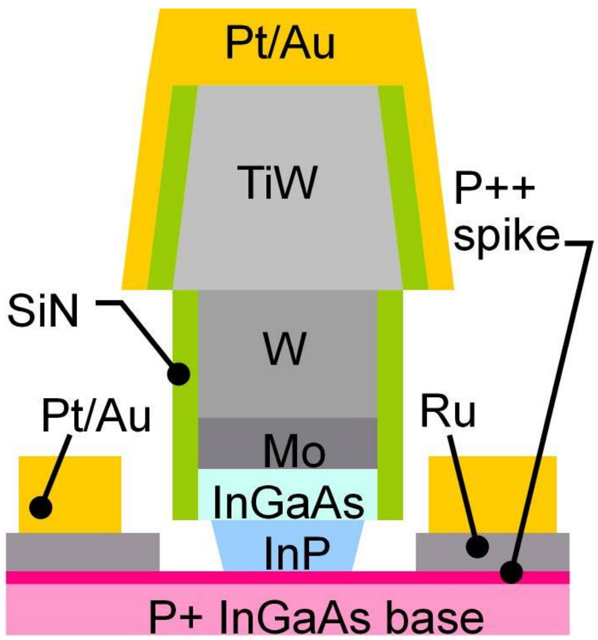


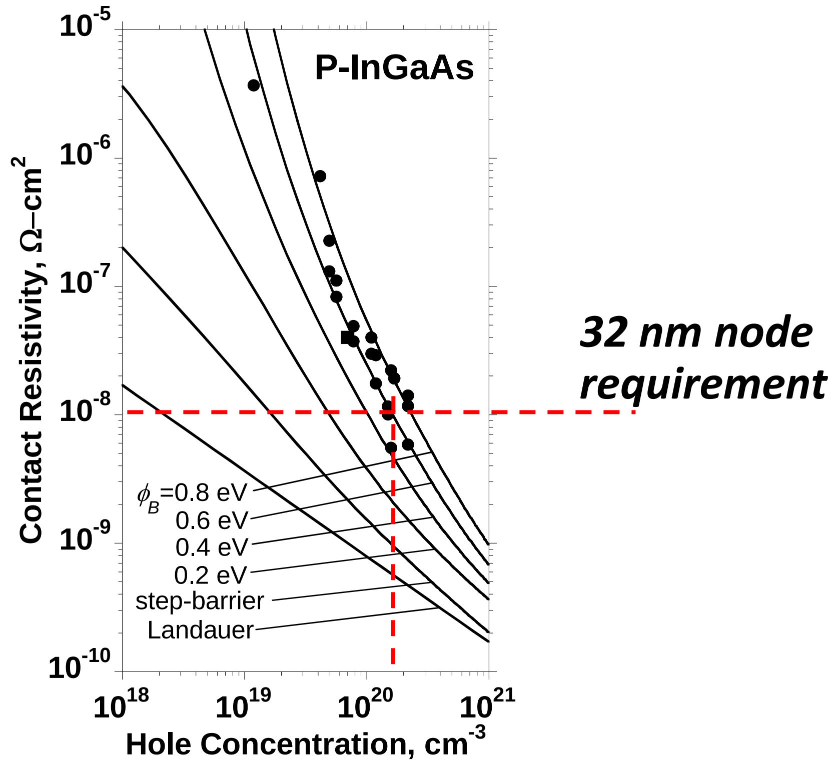
low contact resistivity
low penetration depth

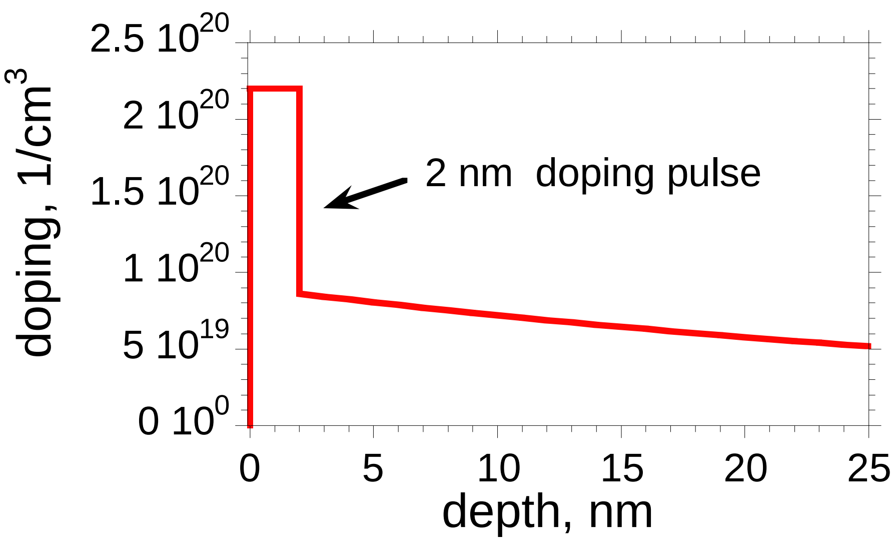
low bulk access resistivity

base surface not exposed to photoresist chemistry: no contamination
low contact resistivity, shallow contacts
low penetration depth allows thin base, pulsed-doped base contacts

Refractory Base Process (2)





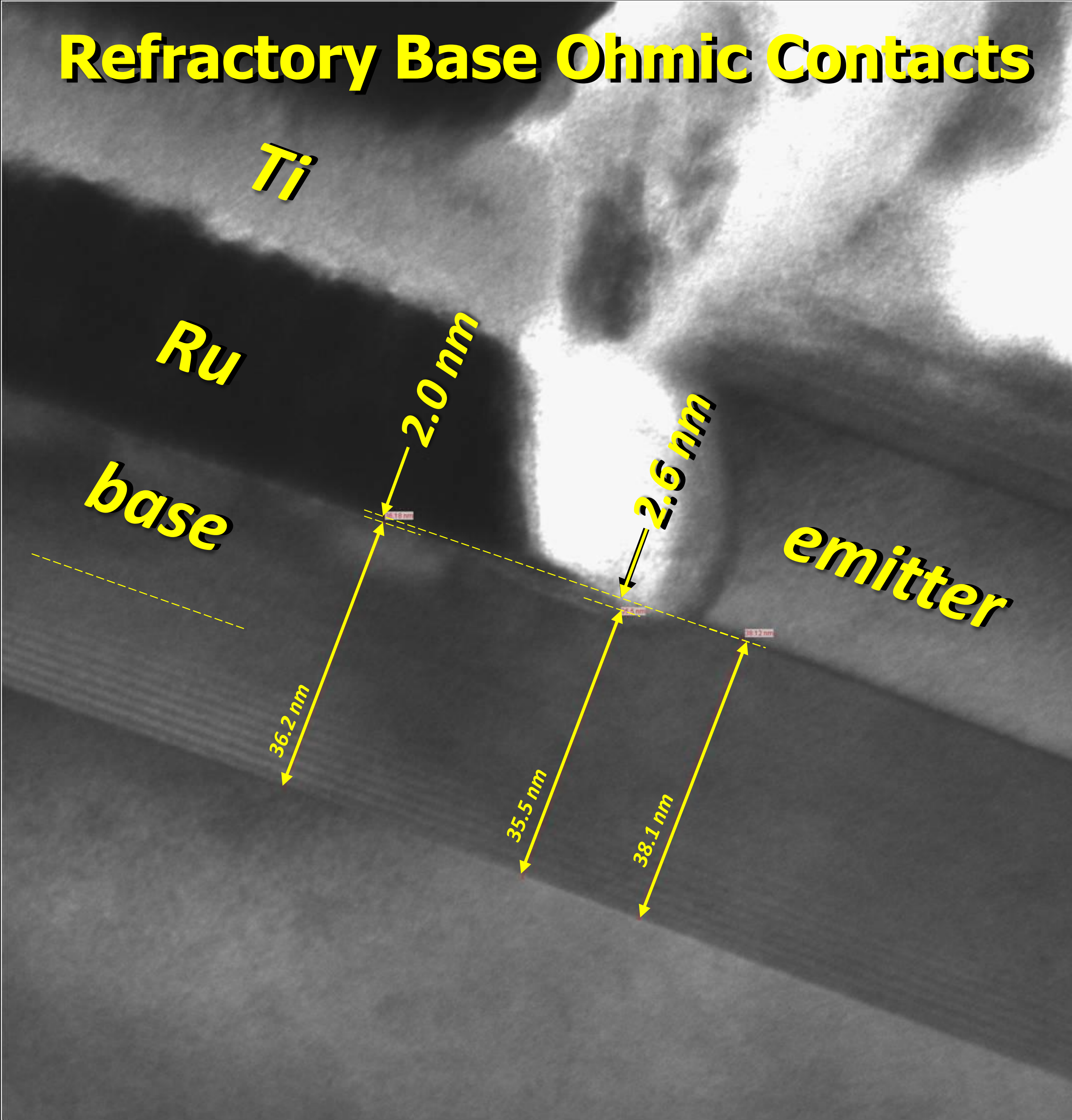


Increased surface doping:
reduced contact resistivity,
but increased Auger recombination.

→ Surface doping spike at most 2-5 thick.

Refractory contacts do not penetrate; compatible with pulse doping.

Refractory Base Ohmic Contacts

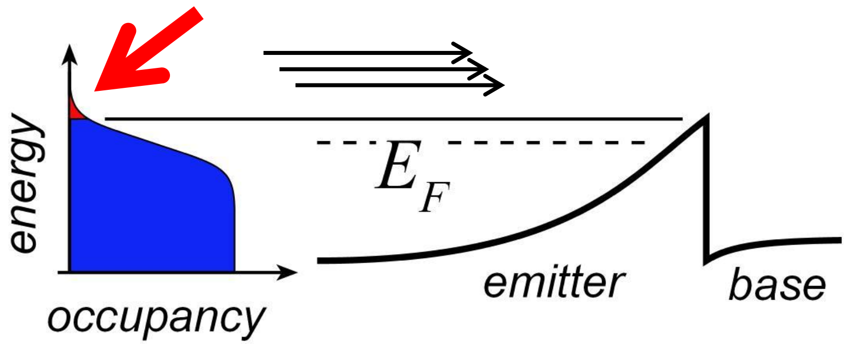


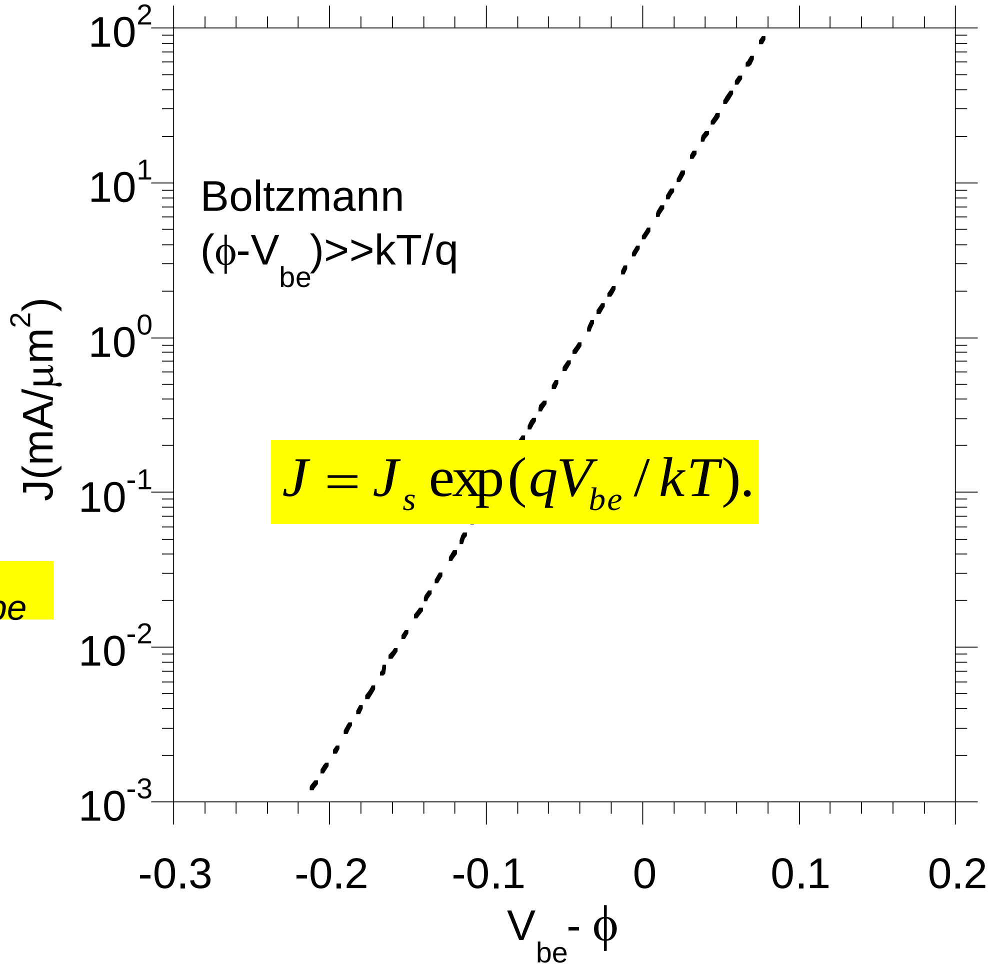
Ru / Ti / Au

<2 nm
Ru contact
penetration

(surface removal during cleaning)

Degenerate Injection→ Reduced Transconductance





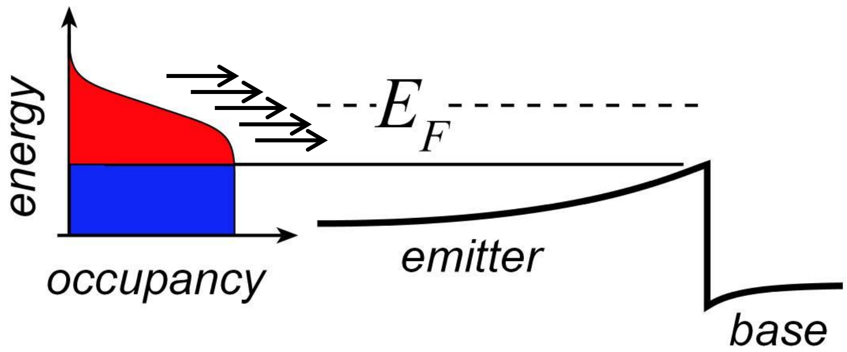
Current varies exponentially with V_{be}

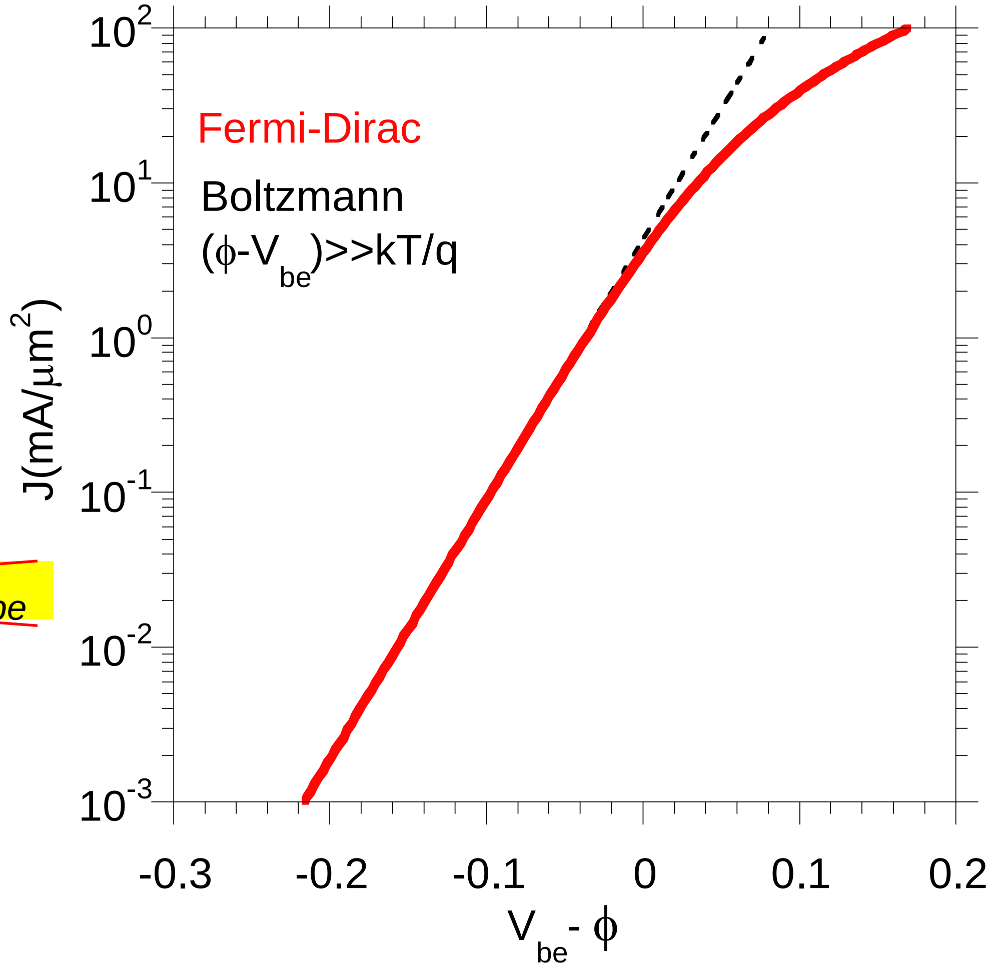
$$J = J_s \exp(qV_{be}/kT).$$

Transconductance is high

$$g_m / A_E \propto J$$

Degenerate Injection→ Reduced Transconductance



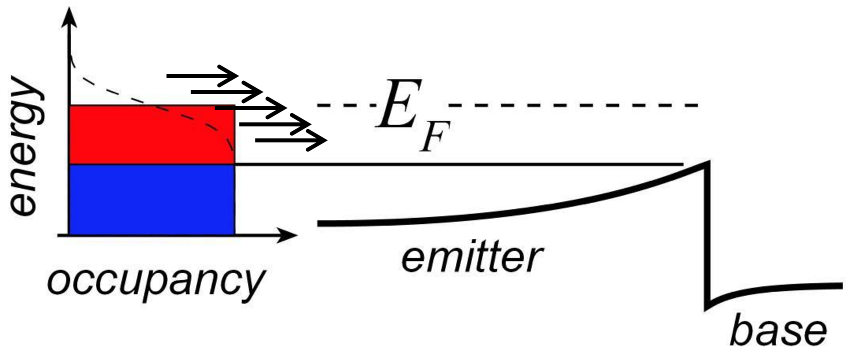


~~*Current varies exponentially with V_{be}*~~

~~$J = J_s \exp(qV_{be}/kT)$.~~

Transconductance is reduced

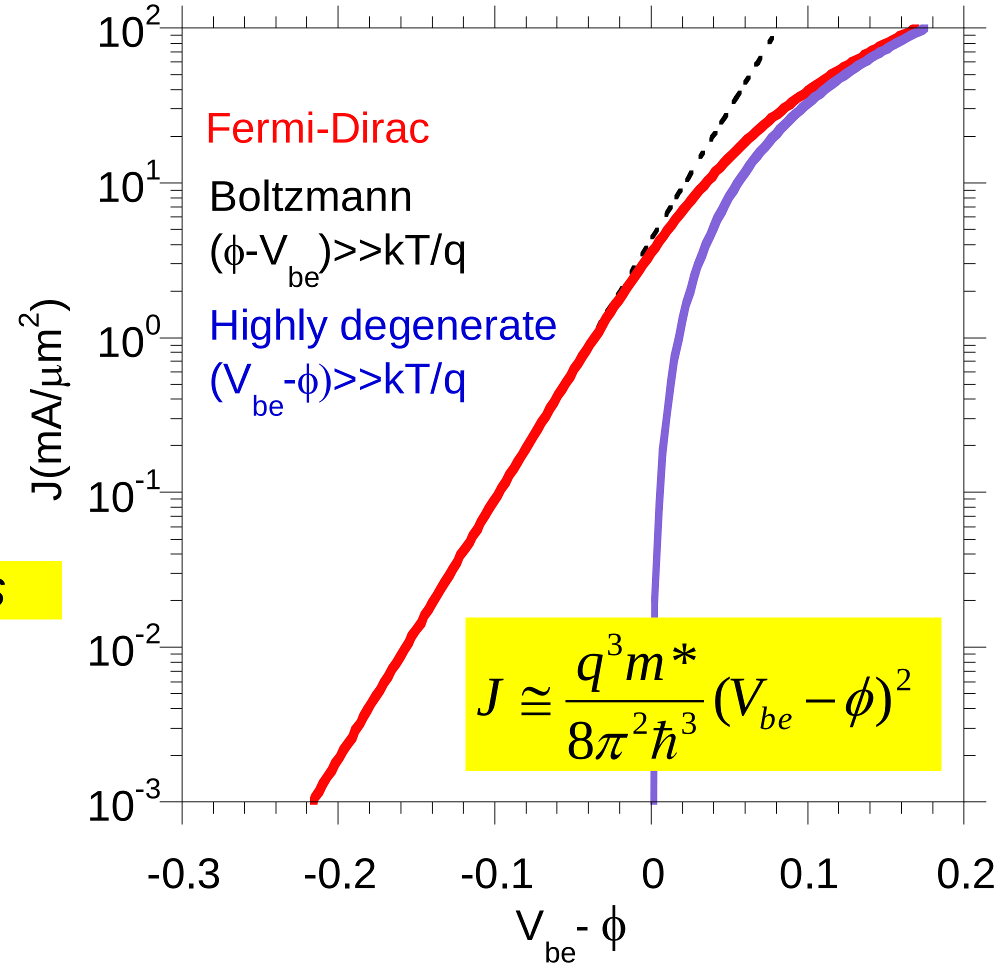
Degenerate Injection→ Reduced Transconductance



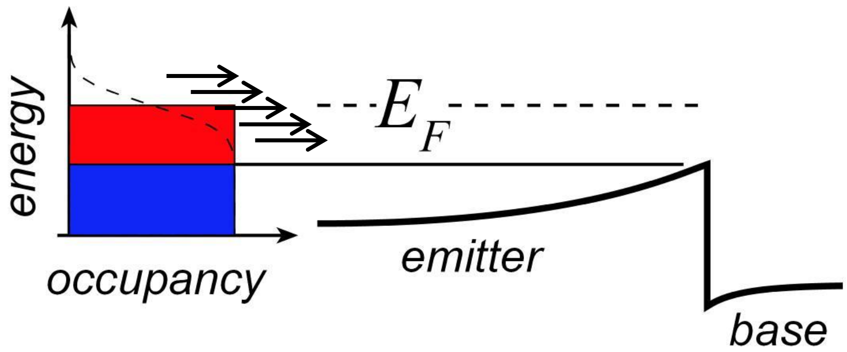
Highly degenerate limit:

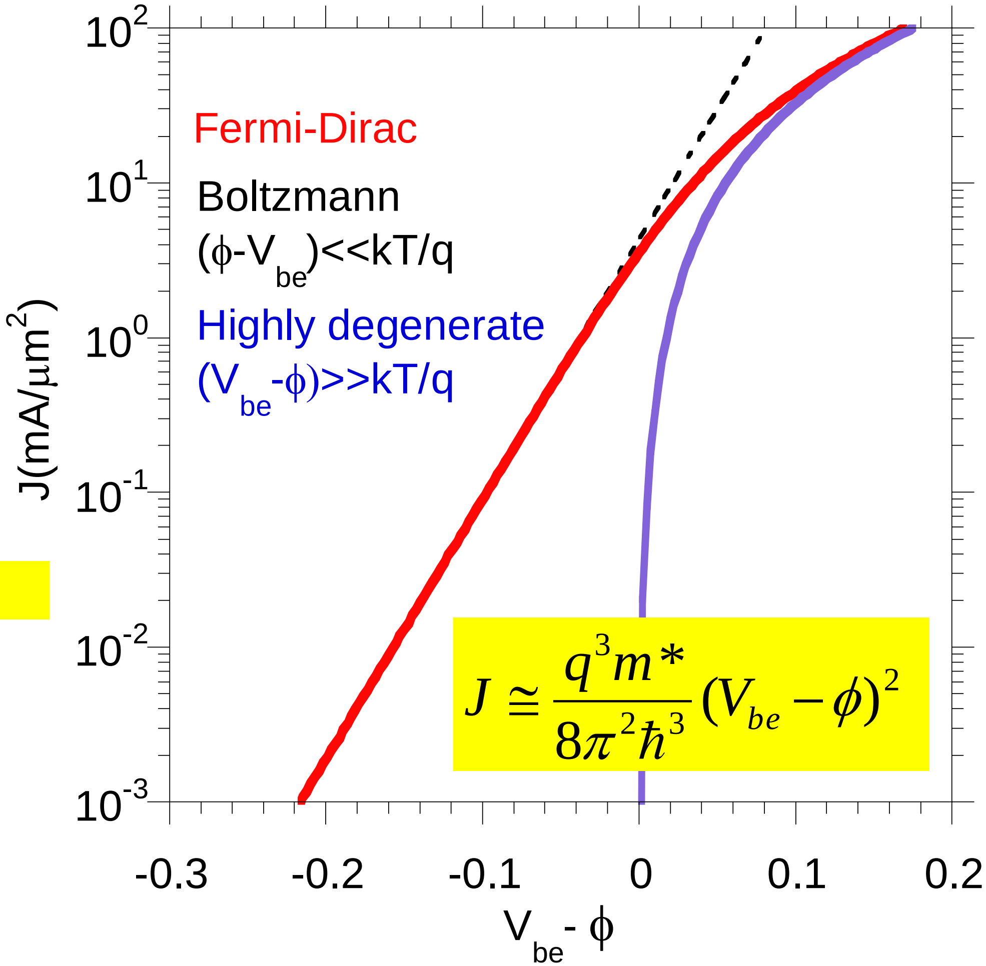
current varies as the square of bias

$$J \propto m_E^* (V_{be} - \phi)^2$$



Degenerate Injection→ Reduced Transconductance





Highly degenerate limit:

current varies as the square of bias

$$J \propto m_E^*(V_{be}-\phi)^2$$

Transconductance varies as $J^{1/2}$

$$g_m / A_E \propto \sqrt{m_E^* J}$$

...and as $(m^*)^{1/2}$

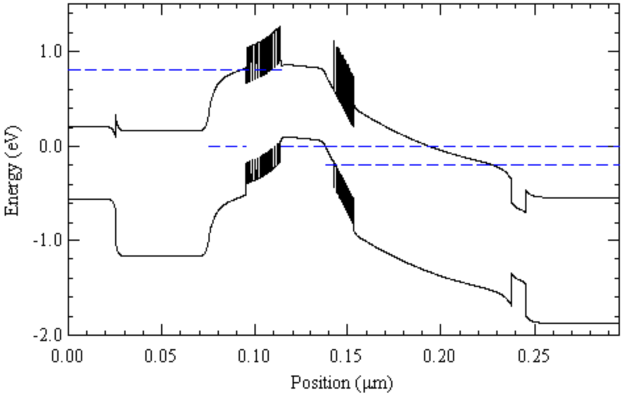
At & beyond 32 nm, we must increase the emitter effective mass.

Degenerate Injection→Solutions

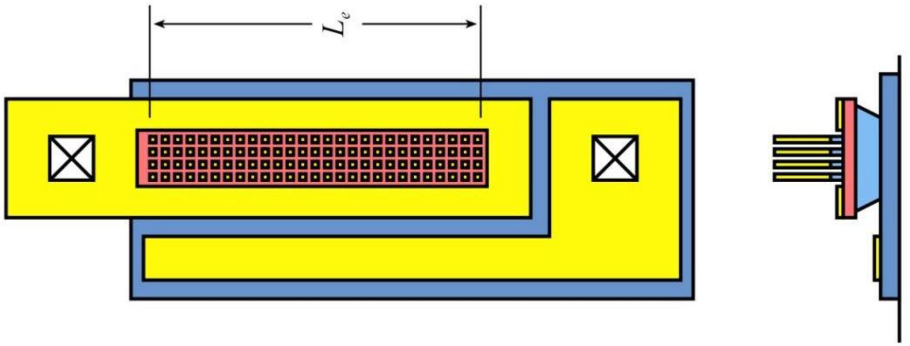
At & beyond 32 nm, we must increase the emitter (transverse) effective mass.

Other emitter semiconductors:
no obvious good choices (band offsets, etc.).

Emitter-base superlattice:
increases transverse mass in junction
evidence that InAlAs/InGaAs grades are beneficial



Extreme solution (10 years from now):
partition the emitter into small sub-junctions, ~ 5 nm x 5 nm.
parasitic resistivity is reduced progressively as sub-junction areas are reduced.



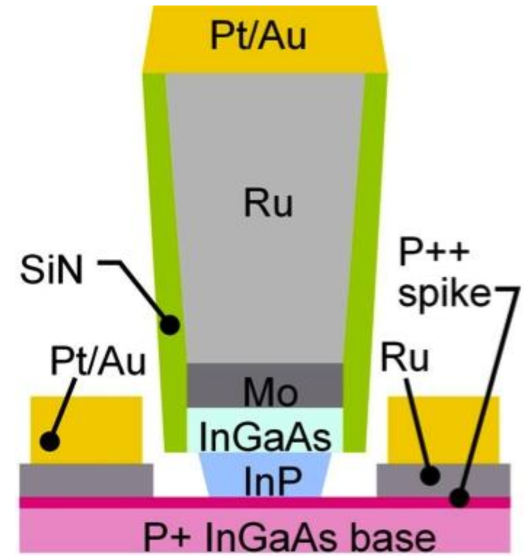
3-4 THz Bipolar Transistors are Feasible.

4 THz HBTs realized by:

Extremely low resistivity contacts

Extreme current densities

Processes scaled to 16 nm junctions



Scaling Node	64	32	16	nm
Emitter Width	64	32	16	nm
Resistivity	2	1	0.5	Ω-μm^2
Base Thickness	18	15	13	nm
Contact width	60	30	15	nm
Contact ρ	2.5	1.25	0.63	Ω-μm^2
Collector Width	180	90	45	nm
Thickness	53	37.5	26	nm
Current Density	36	72	140	$mA/\mu m^2$
f_τ	1.0	1.4	2.0	THz
f_{max}	2.0	2.8	4.0	THz

Impact:
efficient power amplifiers
and complex signal processing
from 100-1000 GHz.

InP HBT: Key Features

512 nm node:

high-yield "pilot-line" process, ~4000 HBTs/IC

256 nm node:

Power Amplifiers: >0.5 W/mm @ 220 GHz

highly competitive mm-wave / THz power technology

128 nm node:

>500 GHz f_τ , >1.1 THz f_{max}, ~3.5 V breakdown

breakdown* f_τ = 1.75 THz*Volts

highly competitive mm-wave / THz power technology

64 nm (2 THz) & 32 nm (2.8 THz) nodes:

Development needs major effort, but no serious scaling barriers

1.5 THz monolithic ICs are feasible.

Can we make a 1 THz SiGe Bipolar Transistor ?

Simple physics clearly drives scaling

transit times, C_{cb}/I_c

→ thinner layers, higher current density

high power density → narrow junctions

small junctions→ low resistance contacts

Key challenge: Breakdown

15 nm collector → very low breakdown

Also required:

low resistivity Ohmic contacts to Si

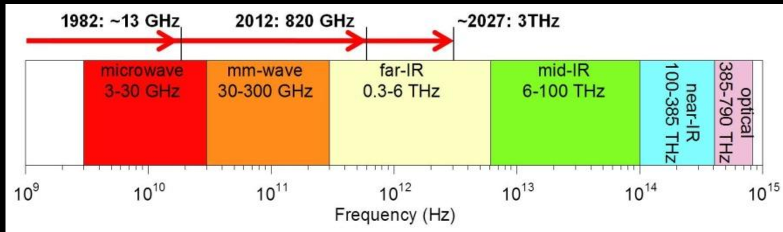
very high current densities: heat

	InP	SiGe	
emitter	64	18	nm width
	2	**0.6**	$\Omega\cdot\mu m^2$ access ρ
base	64	18	nm contact width,
	2.5	**0.7**	$\Omega\cdot\mu m^2$ contact ρ
collector	53	**15**	nm thick
	36	125	$mA/\mu m^2$
	2.75	**1.3?**	V, breakdown
f_τ	**1000**	**1000**	GHz
f_{max}	**2000**	**2000**	GHz
PAs	1000	1000	GHz
digital	480	480	GHz
(2:1 static divider metric)			

Assumes collector junction 3:1 wider than emitter.
Assumes SiGe contacts no wider than junctions

THz InP Bipolar Transistor Technology

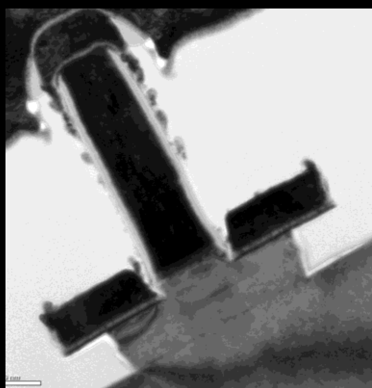
UCSB



Goal:
extend the operation of electronics to the highest feasible frequencies

THz InP Heterojunction Bipolar Transistors

1 THz device



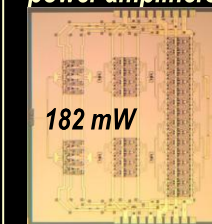
Scaling roadmap through 3 THz

emitter	512	256	128	64	32 nm width
	16	8	4	2	1 $\Omega\cdot\mu m^2$ access ρ
base	300	175	120	60	30 nm contact width,
	20	10	5	2.5	1.25 $\Omega\cdot\mu m^2$ contact ρ
collector	150	106	75	53	37.5 nm thick,
	4.5	9	18	36	72 mA/μm^2 current density
	4.9	4	3.3	2.75	2-2.5 V, breakdown
f_τ	370	520	730	1000	1400 GHz
f_{max}	490	850	1300	2000	2800 GHz
power amplifiers	245	430	660	1000	1400 GHz
digital 2:1 divider	150	240	330	480	660 GHz

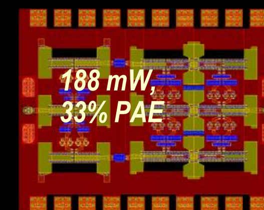
Enabling Technologies :
~30 nm fabrication processes, extremely low resistivity (epitaxial, refractory) contacts, extreme current densities, doping at solubility limits, few-nm-thick junctions

60-600 GHz IC examples; demonstrated & in fab

220 GHz power amplifiers

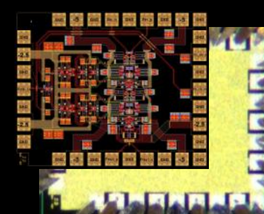


ultra-efficient 85 GHz power amplifiers

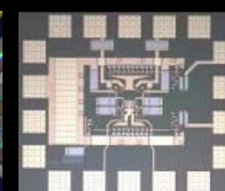


*100 GHz ICs for *electronic* demultiplexing of WDM optical communications*

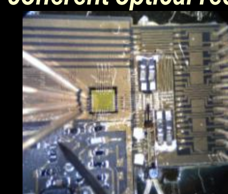
50 GHz sample/hold



40 GHz op-amp

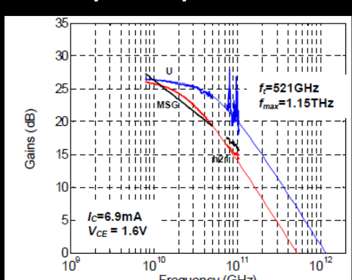


40 Gb/s phase-locked coherent optical receivers

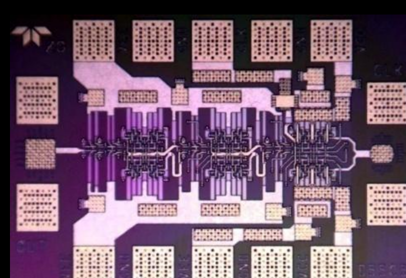


Teledyne Scientific: moving THz IC Technology towards aerospace applications

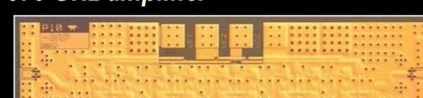
1.1 THz pilot IC process



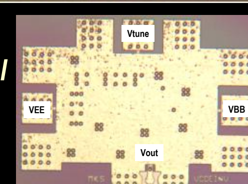
204 GHz digital logic (M/S latch)



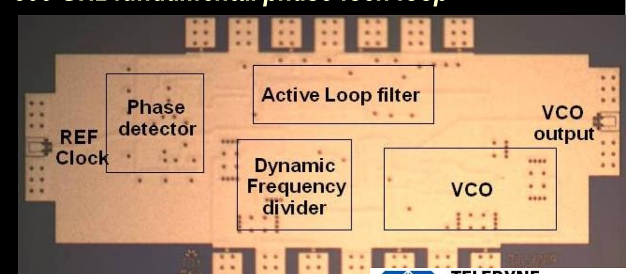
670 GHz amplifier



614 GHz fundamental oscillator (VCO)



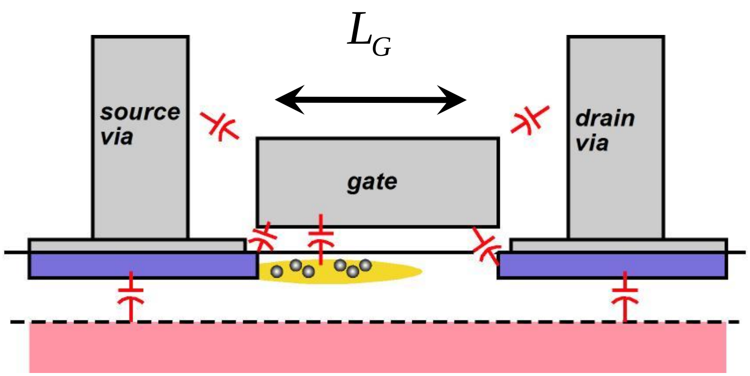
300 GHz fundamental phase-lock-loop



TELEDYNE SCIENTIFIC COMPANY
A Teledyne Technologies Company

THz InP HEMTs and III-V MOSFETs

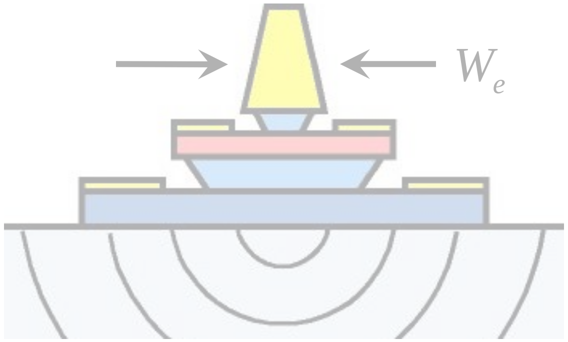
Changes required to double transistor bandwidth



$(\text{gate width } W_G)$

FET parameter	change
gate length	decrease 2:1
current density (mA/μm), g_m (mS/μm)	increase 2:1
transport effective mass	constant
channel 2DEG electron density	increase 2:1
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
channel thickness	decrease 2:1
channel density of states	increase 2:1
source & drain contact resistivities	decrease 4:1

fringing capacitance does not scale → linewidths scale as (1 / bandwidth)



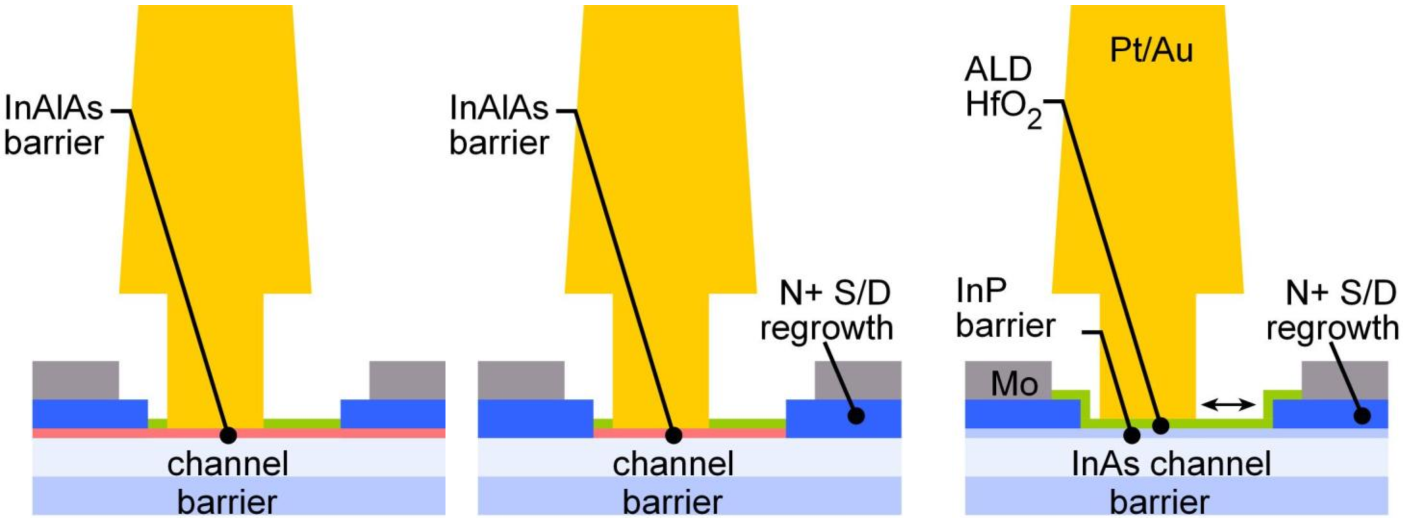
$(\text{emitter length } L_E)$

HBT parameter	change
emitter & collector junction widths	decrease 4:1
current density (mA/μm^2)	increase 4:1
current density (mA/μm)	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1

constant voltage, constant velocity scaling

nearly constant junction temperature → linewidths vary as (1 / bandwidth)^2

FET scaling challenges...and solutions



Gate barrier under S/D contacts → high S/D access resistance
addressed by S/D regrowth

High gate leakage from thin barrier, high channel charge density
(almost) eliminated by ALD high-K gate dielectric

Other scaling considerations:
low InAs electron mass→ low state density capacitance → g_m fails to scale
increased m* , hence reduced velocity in thin channels
minimum feasible thickness of gate dielectric (tunneling) and channel

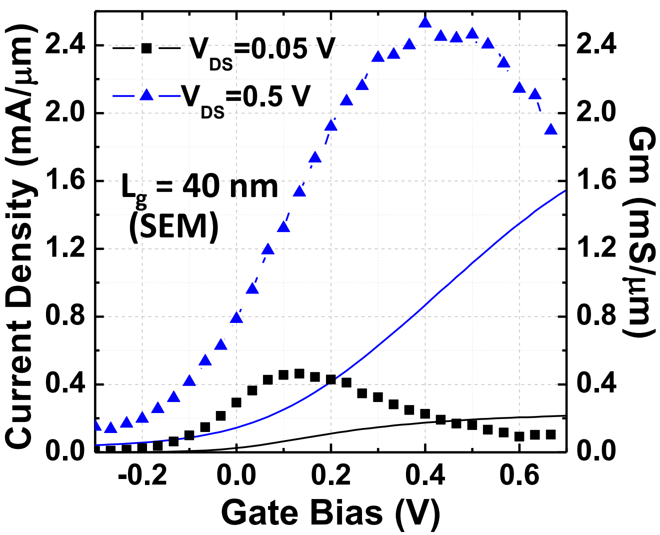
III-V MOS

Peak transconductance; VLSI-style FET:

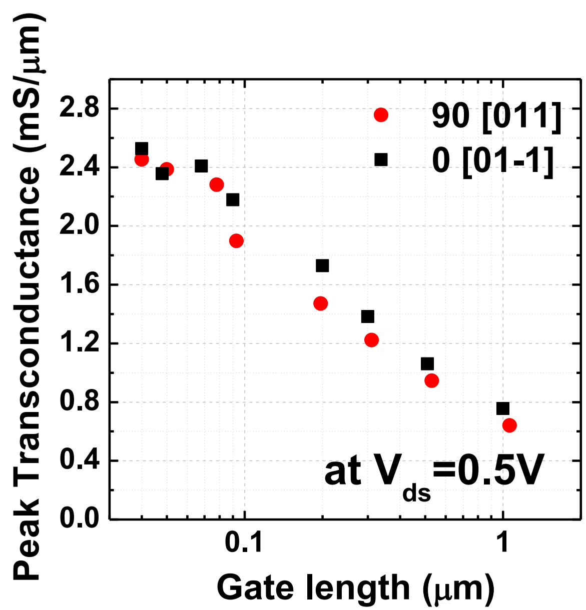
2.5 mS/micron

~85% of best THz InAs HEMTs

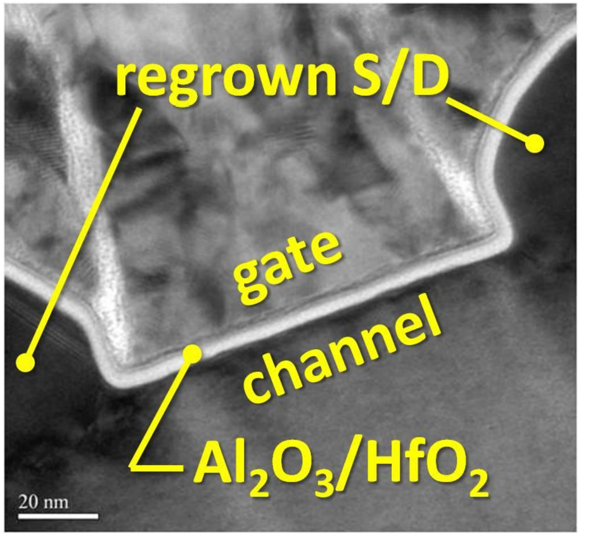
III-V MOS will soon surpass HEMTs in RF performance



Sanghoon Lee

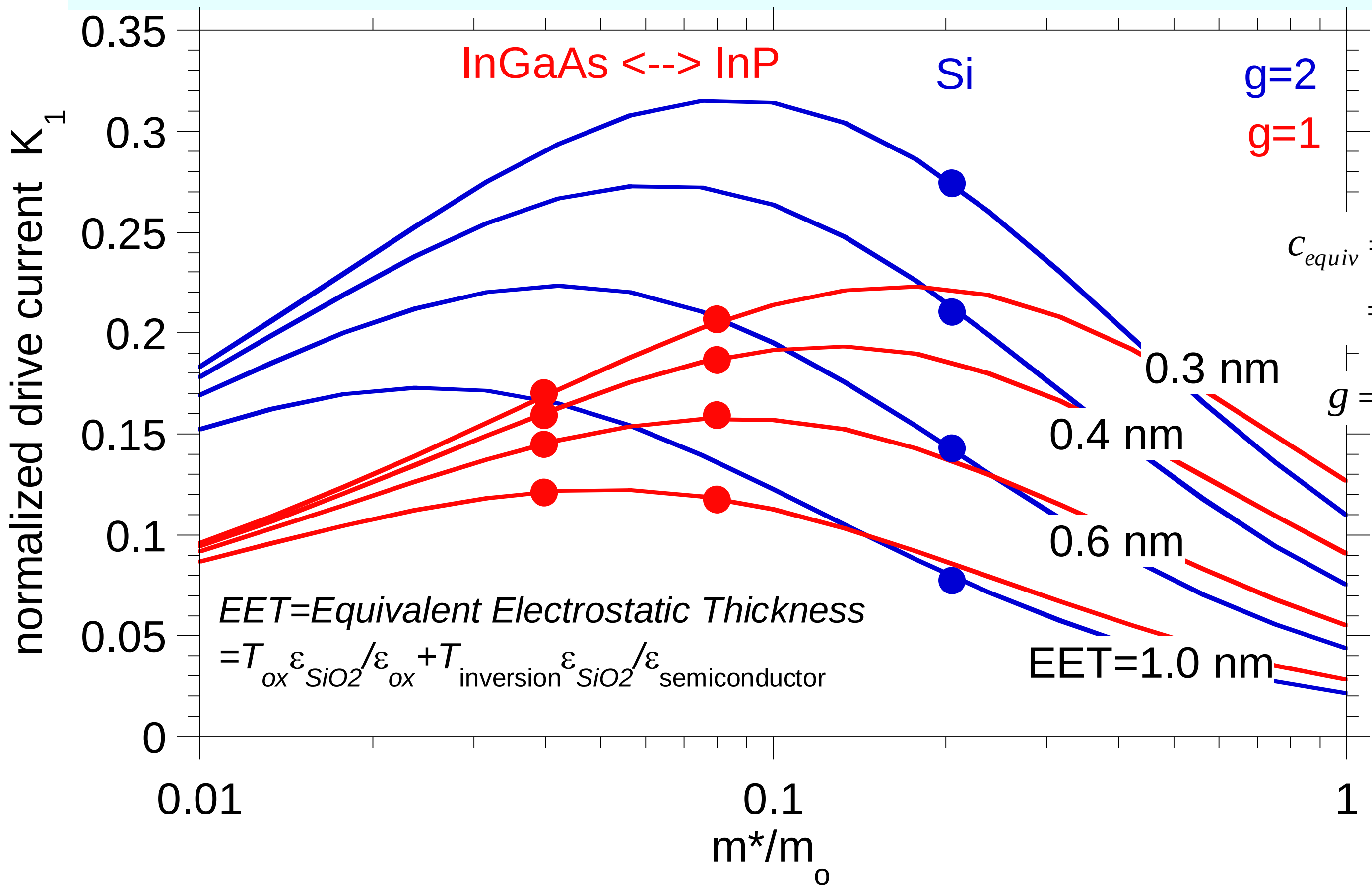


40 nm devices are nearly ballistic



FET Drain Current in the Ballistic Limit

$$J = \underline{K_1} \cdot \left(84 \frac{\text{mA}}{\mu\text{m}}\right) \cdot \left(\frac{V_{gs} - V_{th}}{1\,\text{V}}\right)^{3/2}, \quad \text{where } \underline{K_1} = \frac{g \cdot (m^*/m_o)^{1/2}}{\left(1 + (c_{dos,o}/c_{equiv}) \cdot g \cdot (m^*/m_o)\right)^{3/2}}$$



$$c_{equiv} = (1/c_{ox} + 1/c_{\text{depth}})^{-1} = \varepsilon_{\text{SiO}_2}/EET$$

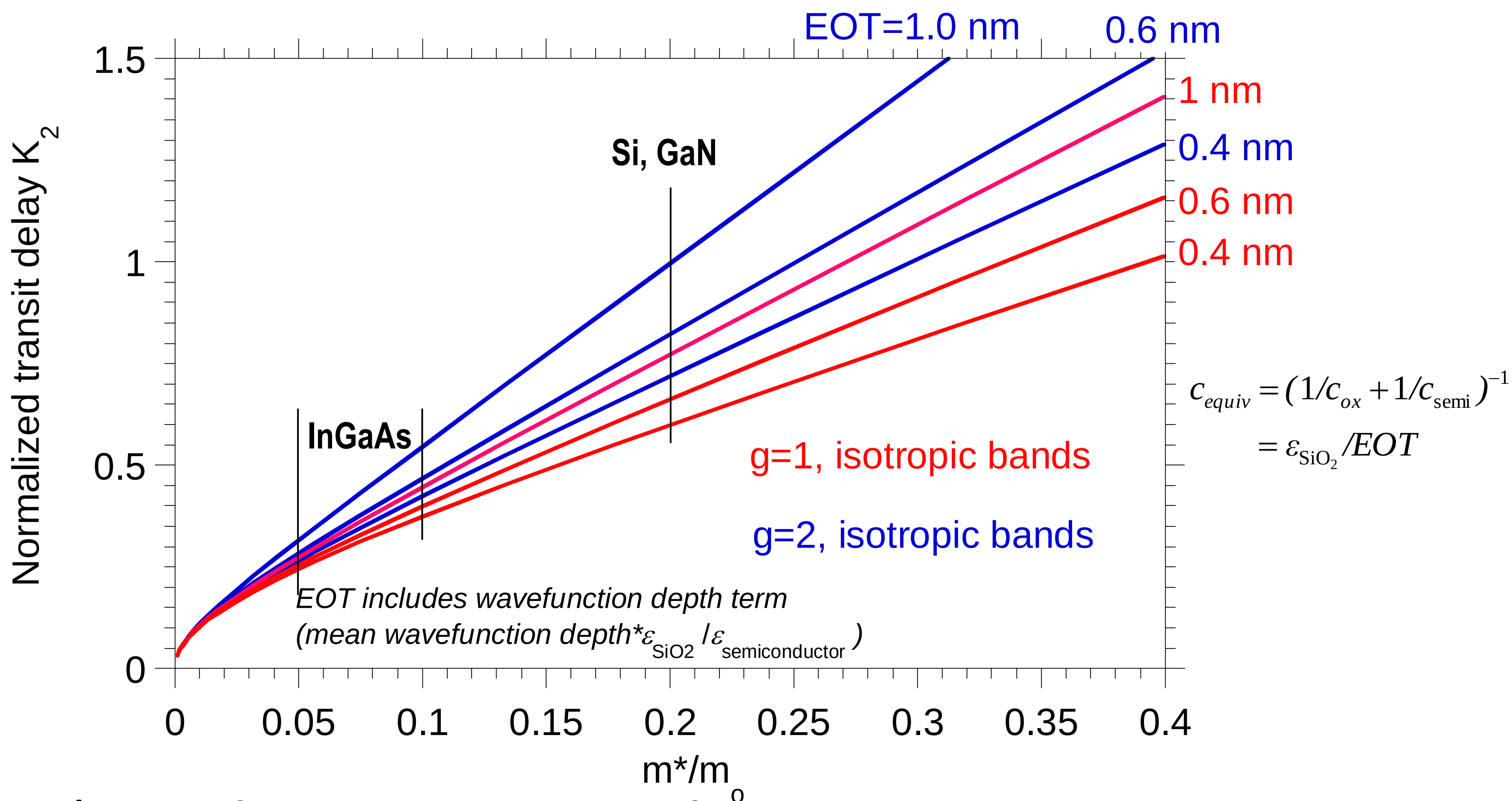
$g = \#$ band minima

$$c_{dos,o} = q^2 m_0 / 2\pi\hbar^2$$

In ballistic limit, current and transconductance are set by: channel & dielectric thickness, transport mass, state density

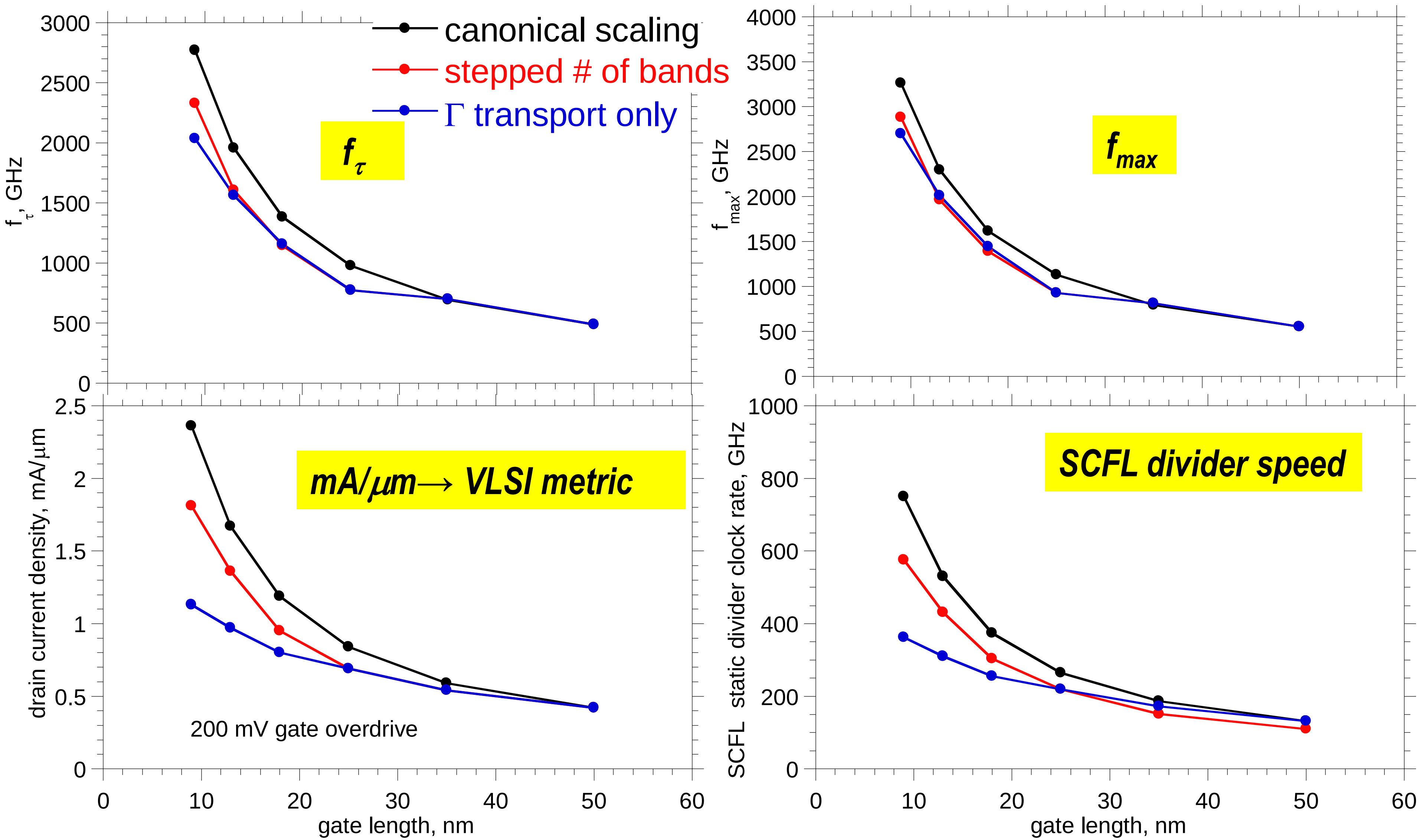
Transit delay versus mass, # valleys, and EOT

$$\tau_{ch} \equiv \frac{Q_{ch}}{I_D} = K_2 \cdot \left(\frac{L_g}{2.52 \cdot 10^7 \text{ cm/s}} \right) \cdot \left(\frac{1\,\text{Volt}}{V_{gs} - V_{th}} \right)^{1/2} \text{ where } K_2 = \left(\frac{m^*}{m_0} \right)^{1/2} \cdot \left(1 + \frac{c_{dos,o}}{c_{eq}} \cdot g \cdot \frac{m^*}{m_o} \right)^{1/2}$$



Low m* gives lowest transit time, lowest Cgs at any EOT.

FET Scaling: fixed vs. increasing state density



Need higher state density for ~10 nm node

2-3 THz Field-Effect Transistors are Feasible.

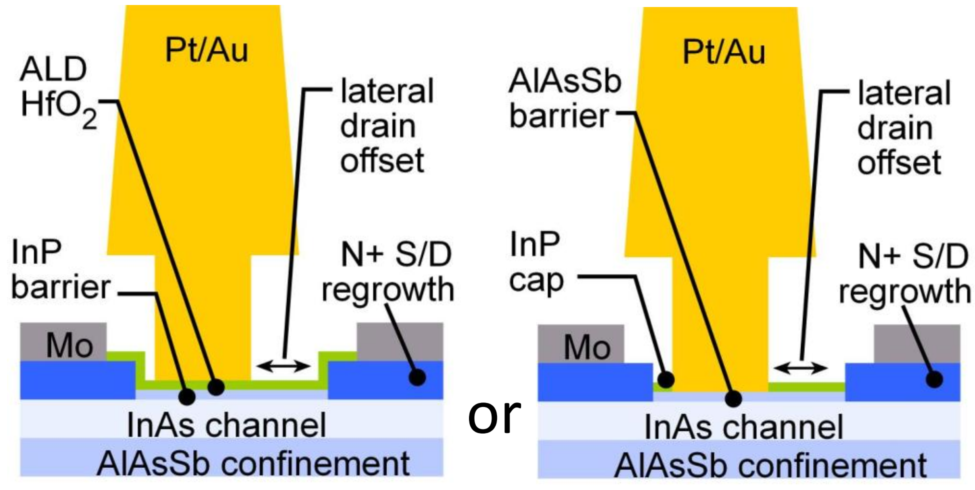
3 THz FETs realized by:

Ultra low resistivity source/drain

High operating current densities

Very thin barriers & dielectrics

Gates scaled to 9 nm junctions



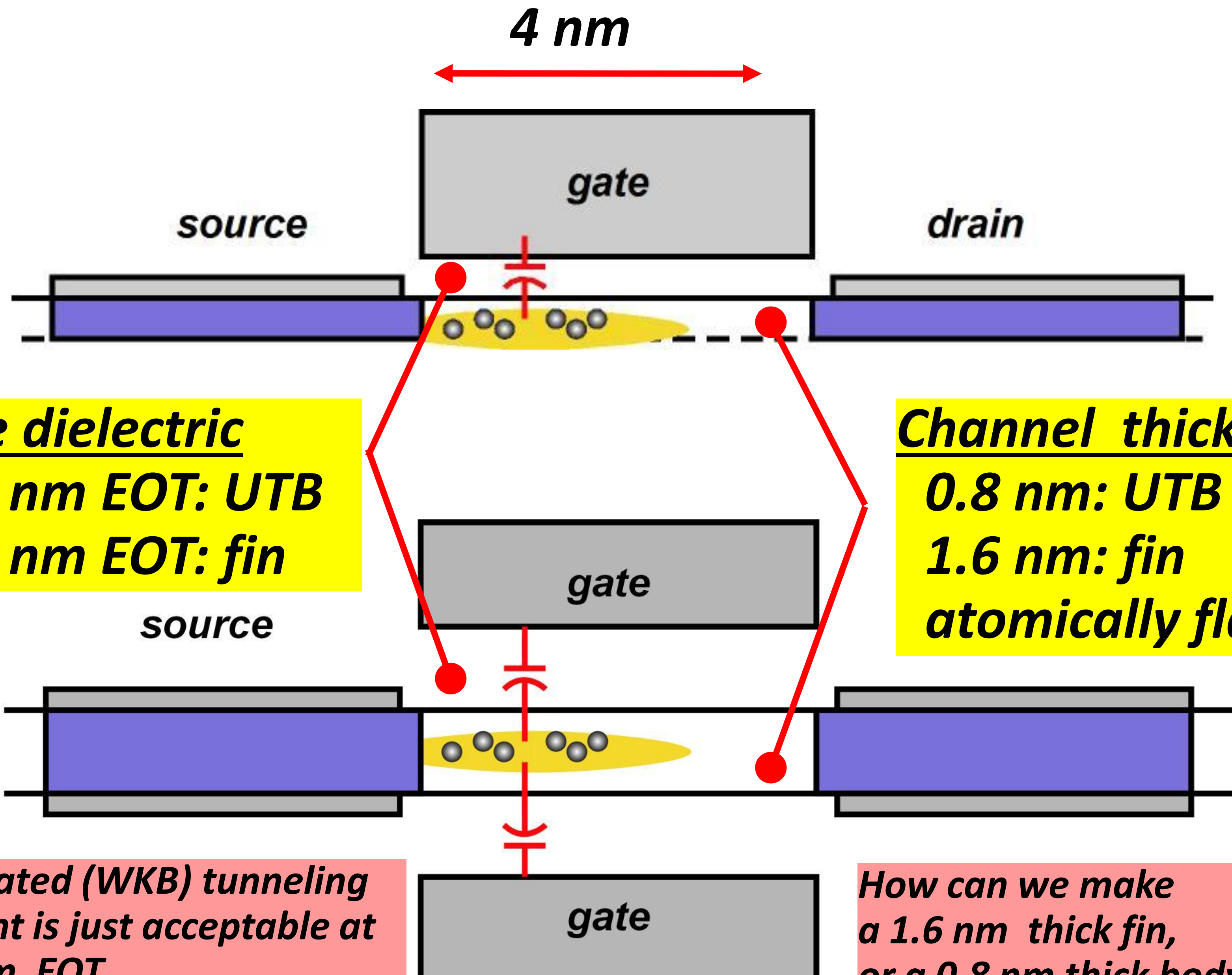
MOSFET high-barrier HEMT

Impact:
Sensitive, low-noise receivers
from 100-1000 GHz.

3 dB less noise →
need 3 dB less transmit power.

gate length	36	18	9	nm
EOT	0.8	0.4	0.2	nm
well thickness	5.6	2.8	1.4	nm
effective mass	0.05	0.08	0.08	times m_0
# bands	1	1	1	--
S/D resistivity	150	74	37	Ω-µm
extrinisic g_m	2.5	4.2	6.4	mS/µm
on-current	0.55	0.8	1.1	mA/µm
f_τ	0.70	1.2	2.0	THz
f_{max}	0.81	1.4	2.7	THz

4-nm / 5-THz FETs: Challenges



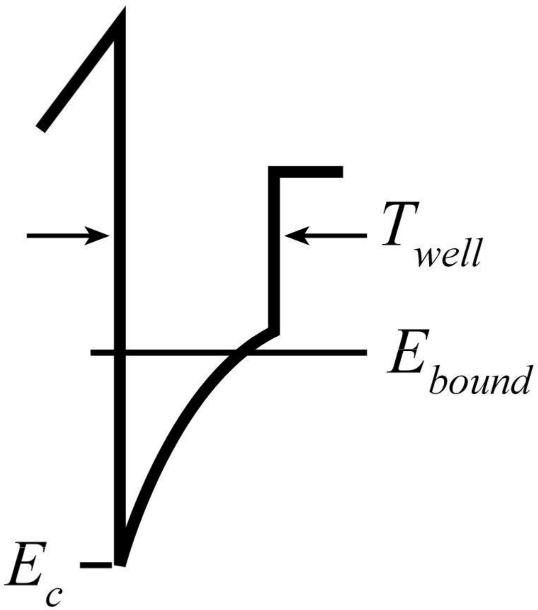
Gate dielectric
0.1 nm EOT: UTB
0.2 nm EOT: fin

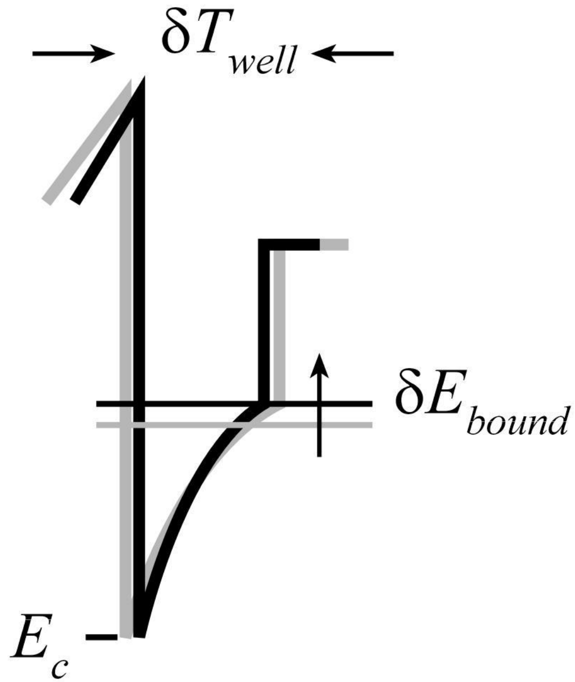
Channel thickness
0.8 nm: UTB
1.6 nm: fin
atomically flat

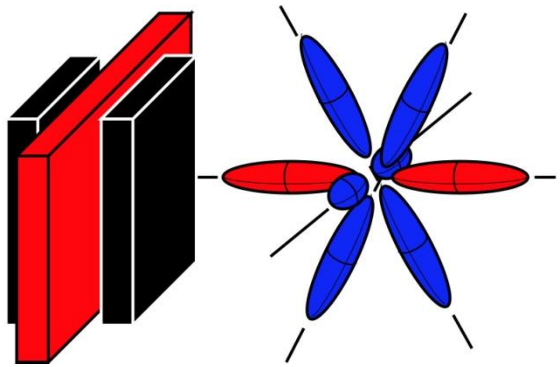
Estimated (WKB) tunneling current is just acceptable at 0.2 nm EOT.

How can we make a 1.6 nm thick fin, or a 0.8 nm thick body ?

Thin wells have high scattering rate





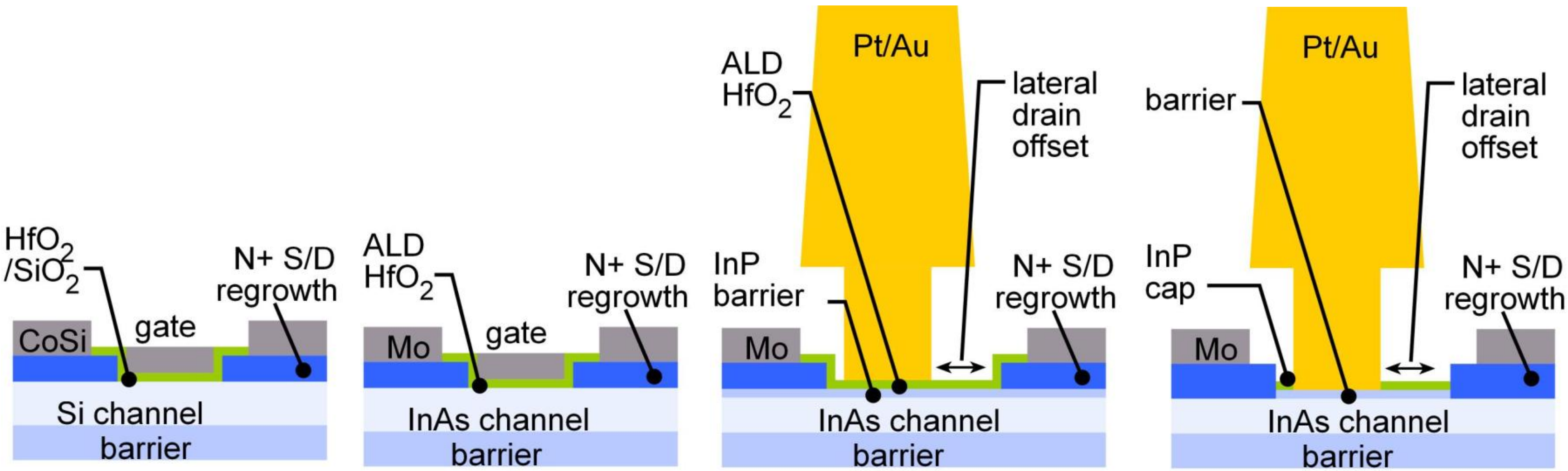


$$\text{Scattering probability} \propto 1/m_q^2 T_{well}^6.$$

Sakaki
APL 51, 1934 (1987).

Need single-atomic-layer control of thickness
Need high *quantization* mass m_q.

III-V vs. CMOS: A false comparison ?



UTB Si MOS **UTB III-V MOS** **III-V THz MOS/HEMT** **III-V THz HEMT**

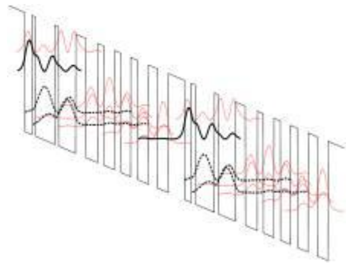
III-V MOS has a reasonable chance of future use in VLSI

The real THz / VLSI distinction:
Device geometry optimized for high-frequency gain
vs. optimized for small footprint and high DC on/off ratio.

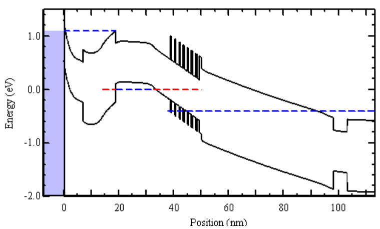
Conclusion

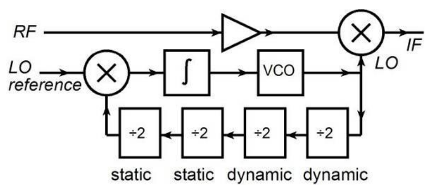
THz and Far-Infrared Electronics

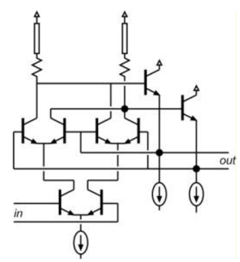
IR today→ lasers & bolometers → generate & detect

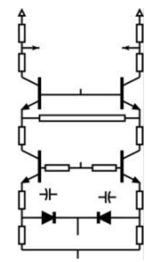



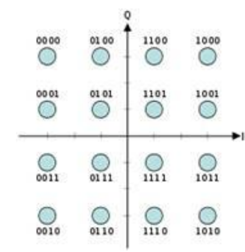

Far-infrared ICs: <u>classic</u> device physics, <u>classic</u> circuit design











It's all about classic scaling:
contact and gate dielectrics...

...wire resistance,...

...heat,...

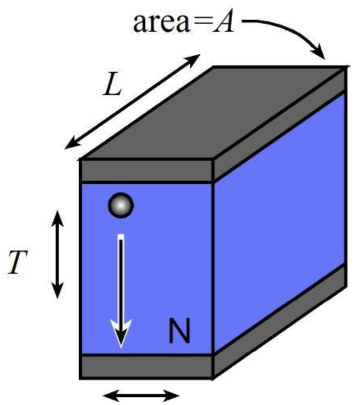
...& charge density.

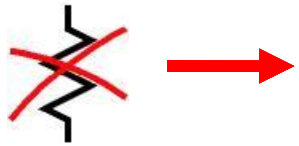
band structure and
density of quantum states
(new!).

Even 1-3 THz ICs will be feasible

(backup slides follow)

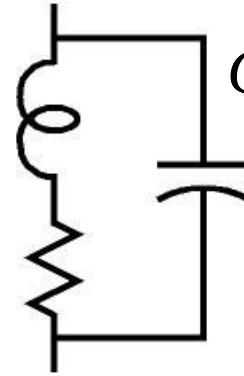
Electron Plasma Resonance: Not a Dominant Limit





$$L_{\text{kinetic}} = \frac{T}{A}\frac{1}{q^2 n m^*}$$

$$R_{\text{bulk}} = \frac{T}{A}\frac{1}{q^2 n m^* \tau_m}$$



$$C_{\text{displacement}} = \frac{\varepsilon A}{T}$$

	dielectric relaxation frequency	scattering frequency	plasma frequency
	$f_{dielecic} = \frac{1/2\pi}{C_{\text{displacement}} R_{\text{bulk}}} = \frac{1}{2\pi}\frac{\sigma}{\varepsilon}$	$f_{scatter} = \frac{1}{2\pi}\frac{R_{\text{bulk}}}{L_{\text{kinetic}}} = \frac{1}{2\pi\tau_m}$	$f_{plasma} = \frac{1/2\pi}{\sqrt{L_{\text{kinetic}} C_{\text{displacement}}}}$
n - InGaAs $3.5 \cdot 10^{19} / \text{cm}^3$	800 THz	7 THz	74 THz
p - InGaAs $7 \cdot 10^{19} / \text{cm}^3$	80 THz	12 THz	31 THz