Formation of Sub-10 nm width InGaAs finFETs of 200 nm Height by Atomic Layer Epitaxy

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As FETs are scaled, the dielectric and semiconductor channel thicknesses must be reduced to suppress short-channel effects. Even using fin field effect transistors (finFETs) and gate all around FETs (GAAFETs), [1],[2], whose electrostatic performance is excellent, at 4nm gate length the channel should be less than 2nm thick. To obtain high drive current per unit IC die area, the fin height should be many times the fin pitch, i.e. tens to hundreds of nm. Dry-etching a fin of few-nm width and > 100 nm height presents severe challenges in control of etch sidewall slope and in minimizing surface damage. Here we report an InGaAs finFET fabrication flow which form fins of sub-10nm width and 200 nm height. Fin width is controlled by atomic layer epitaxial (ALE) growth and by semiconductor selective crystallographic wet etching. We further demonstrate self-aligned source-drain regrowth in this process [3],[4]. This facilitates scaling of the source/drain pitch to small dimensions.

Fabrication starts with MOCVD lattice-matched growth on a (100) SI InP substrate of a 40 nm InP buffer layer (N.I.D), a 20 nm InGaAs etch stop layer (N.I.D) and a 200 nm InP layer (N.I.D). All layers were grown by a Thomas Swan 2" MOCVD reactor at 600 $^{\circ}$C with TBP, TBAs, TMI, and TMG as the metal-organic sources. Ridges were then formed in the InP layer to provide a template for InGaAs fin growth (fig. 1a). The ridges were masked by a SiN hard mask, are oriented along [011], and form vertical (011) sidewalls after wet etching using H_3PO_4:HCL [5], a facet-selective etch.

The channel layers were then grown (fig. 1b) by atomic layer epitaxy (ALE). This permits monolayer control of fin width. The sample was first oxidized by UV ozone and etched in dilute HCl. Lattice-matched InGaAs was then grown in 20 cycles of ALE, yielding a sub-10 nm thick layer. Each ALE cycle includes a 10 sec purge of TMGa and TMI mixture and a TBAs purge. The purges were separated by a 10 sec H_2 purge. Growth was at 450 $^{\circ}$C. The SiN hard mask is present during regrowth to prevent growth on the top surface of the InP ridges.

Dummy gates (fig. 1c) are then defined in Hydrogen silsesquioxane (HSQ) to define the source-drain regions, and the N+ InGaAs source and drain are regrown as described in [4]. To maintain mechanical stability of the InGaAs fins, and to prevent their decomposition during the 600 $^{\circ}$C N+ regrowth, the InP template ridges were not etched prior to the N+ regrowth. The SiN hard mask is then stripped and the fins are liberated from the InP growth template (fig. 1e) by selective wet-etching of the InP in H_3PO_4:HCl. At this point, the N+ regrowth supports the fins. 4 nm HfO_2 gate dielectric and 10 nm TiN gate metal, were then deposited by ALD. The TiN gate metal was etched by CHF_3 chemistry (fig. 2e), and source/drain contacts deposited by liftoff (fig. 2f), completing the process.

TEM images (fig. 2a) show the structural characteristics of the fins. Thicknesses are below 10nm, and the fins are 200 nm high. Electrical characterization has been impeded by large source-drain leakage on the present sample. Present results nevertheless show the feasibility of forming high-aspect-ratio fins of less than 10nm thickness. Thin semiconductor bodies permit gate length scaling to small dimensions, while large ratios of fin height to pitch will greatly increase drive current capability.

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[1] M. Radosavljevic et al., *Electron Devices Meeting, Dec 2011. IEDM'11.*
[2] J. J. Gu et al., *Electron Devices Meeting, Dec 2012. IEDM'12.*
[3] A. D. Carter et al., *Device Research Conference* June. *2011* (pp. 19 – 20).
[4] S. Lee et. al., *VLSI Technology and Circuit Symposia* (Late news) June 2013.
[5] P. Elias et. al., *Indium Phosphide and Related Materials Conference* May *2002* (pp.229 – 231).

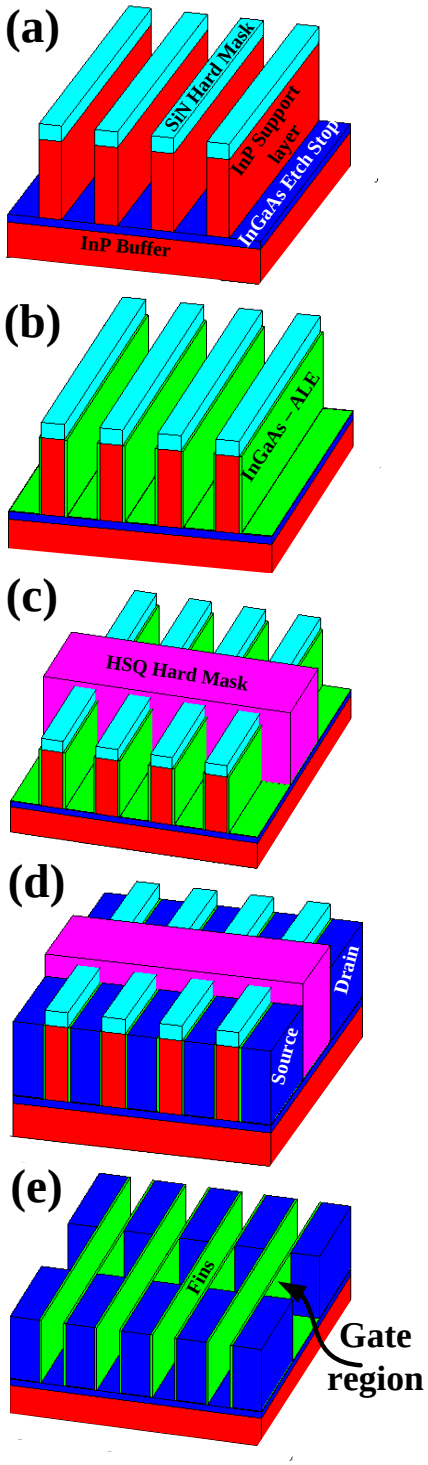

Figure 1: InP template formation (a) along (011), (b) growth of the InGaAs channel on the template sidewall by ALE, (c) patterning of an HSQ dummy-gate to define the fins, and (d) N+ InGaAs source/drain regrowth. The InP template is then removed in HCl to liberate the fins (e).

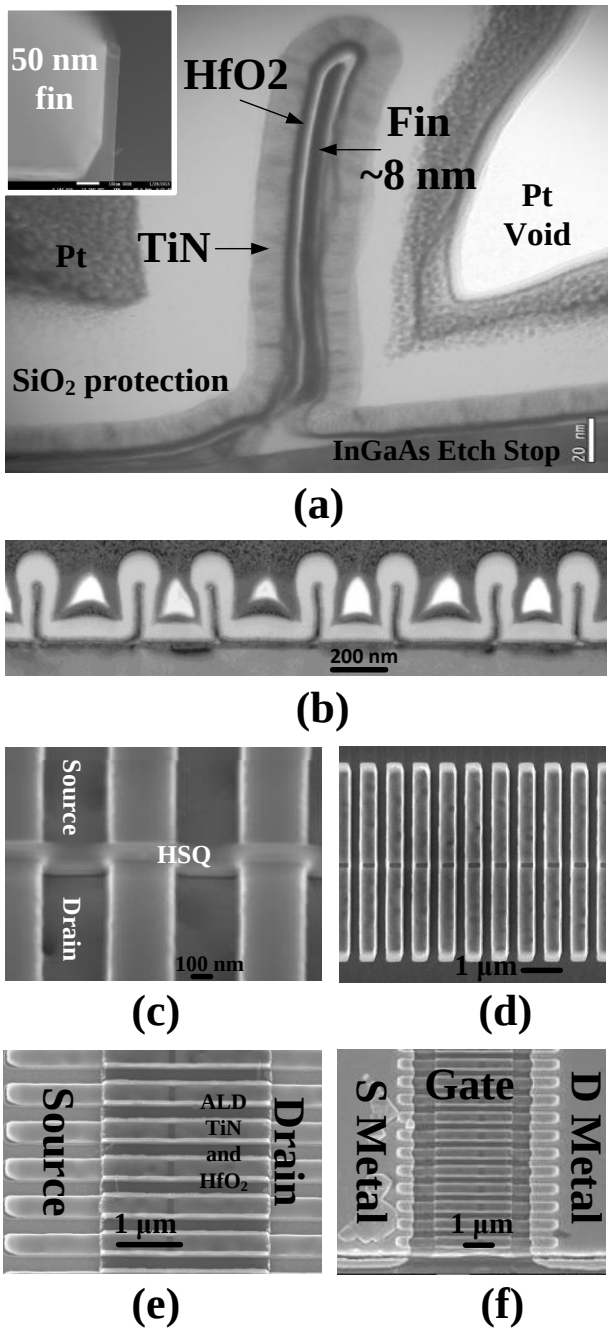

Figure 2: TEM image of a single fin (a) and an array of fins. (b). SEM image of sample immediately prior to S/D regrowth (c), and immediately after etching away the InP template (d). Images immediately prior to (e) and subsequent to (f) source/drain metal liftoff