Formation of Sub-10 nm width InGaAs finFETs of 200 nm Height by Atomic Layer Epitaxy

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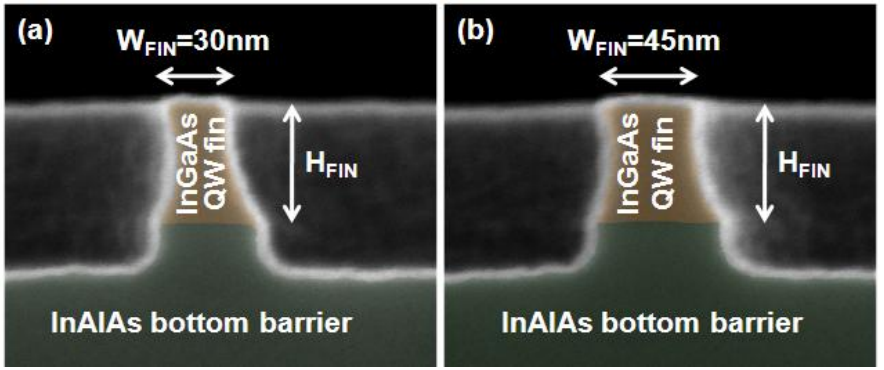
Goal: FinFET with 2-4 nm Body Thickness

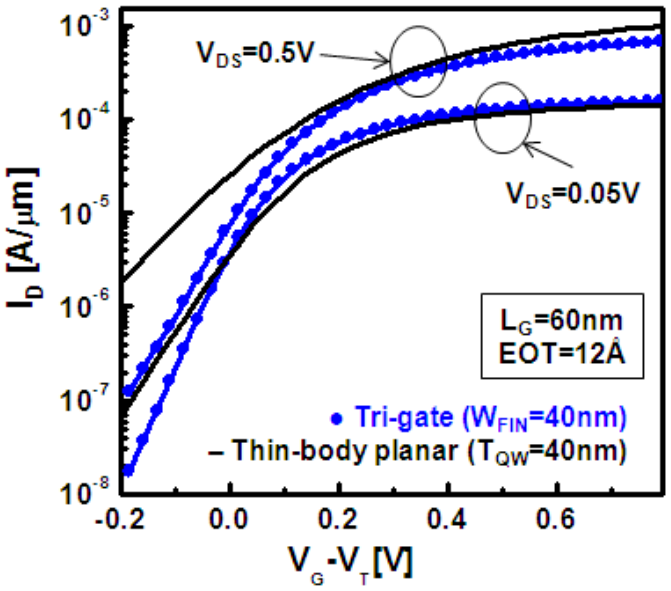
Intel L_g=60nm III-V FinFET (IEDM 2011)



30 nm fin:
too thick at 60 nm gate length

For good electrostatics,
need fin thickness ~ (gate length/2)

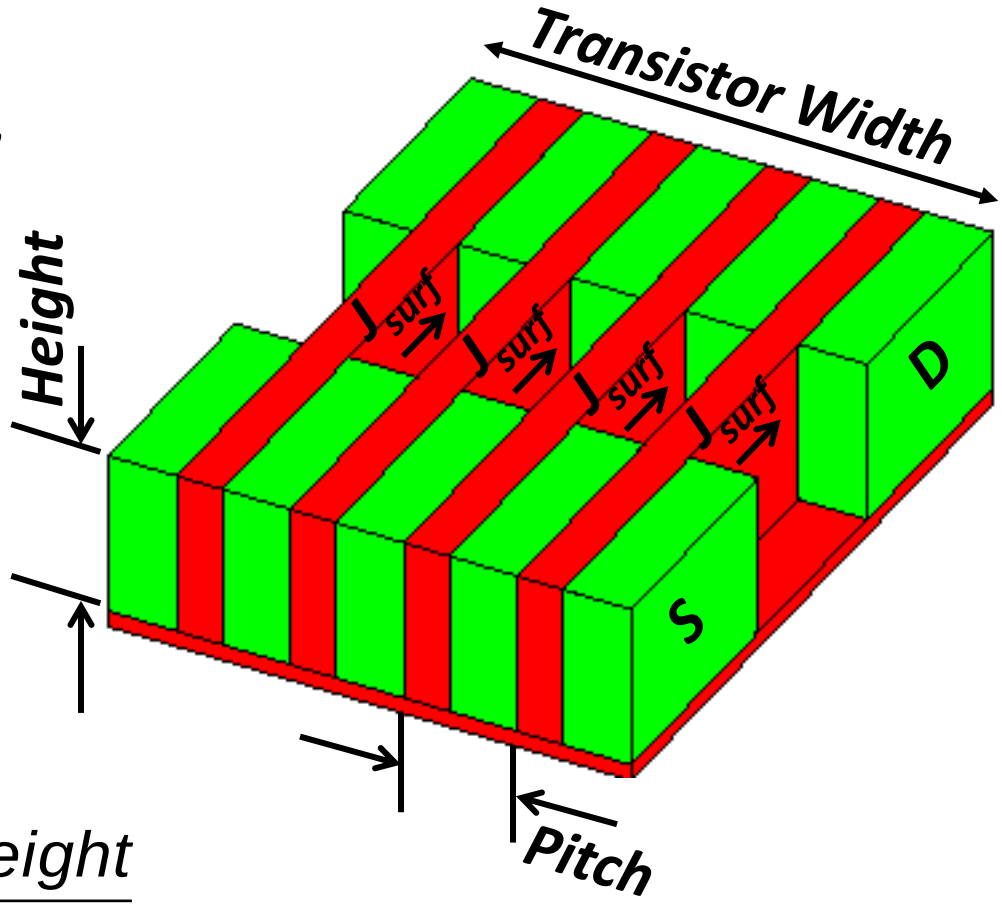
S. H. Park et al., NNIN Symposium Feb 2012.



8nm gate length → need <4 nm thick fin

Goal: Tall Fins for High Drive Current

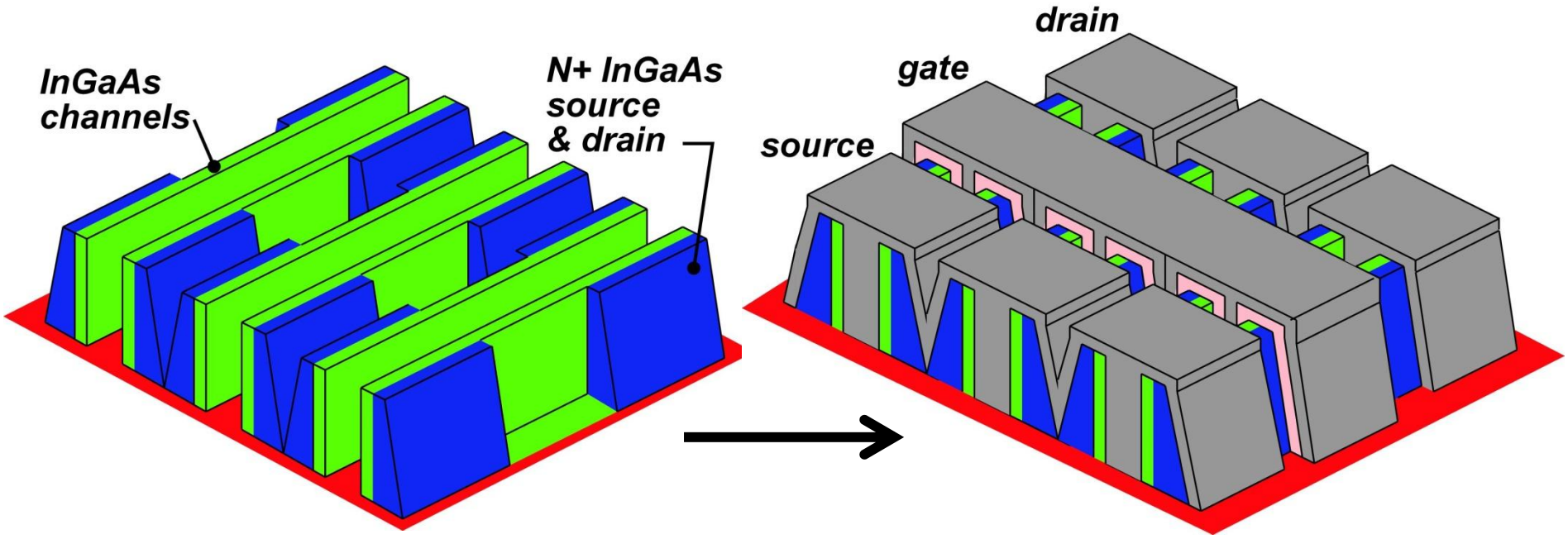
Goal:
large on-current
from small transistor footprint.



$$\frac{current}{transistor\ width} = J_{surface} \cdot \frac{fin\ height}{fin\ pitch}$$

Goal: fin height >> fin pitch (spacing)

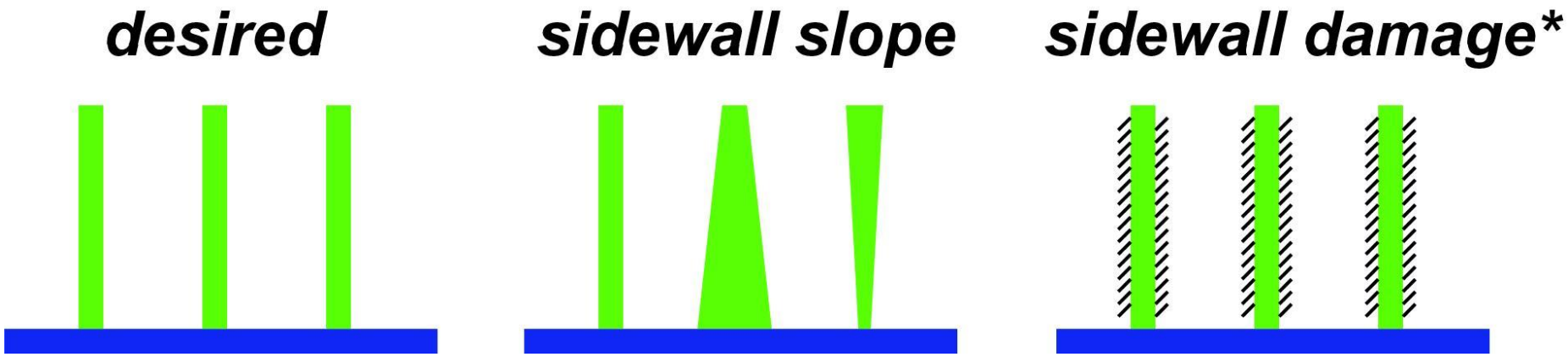
Goal: Fins with Integrated N+ Source/Drain



regrowth→ small S/D pitch → High Integration Density

Why Not Dry-Etch a 2nm Fin ?

Goal: 2-4 nm thickness, 100+ nm height



* ***metallization-induced damage increases D_{it}:***
Burek *et al*, JVST B. 29,4, Jul/Aug 2011;
Dry-etching may well do similar surface damage

serious process challenges

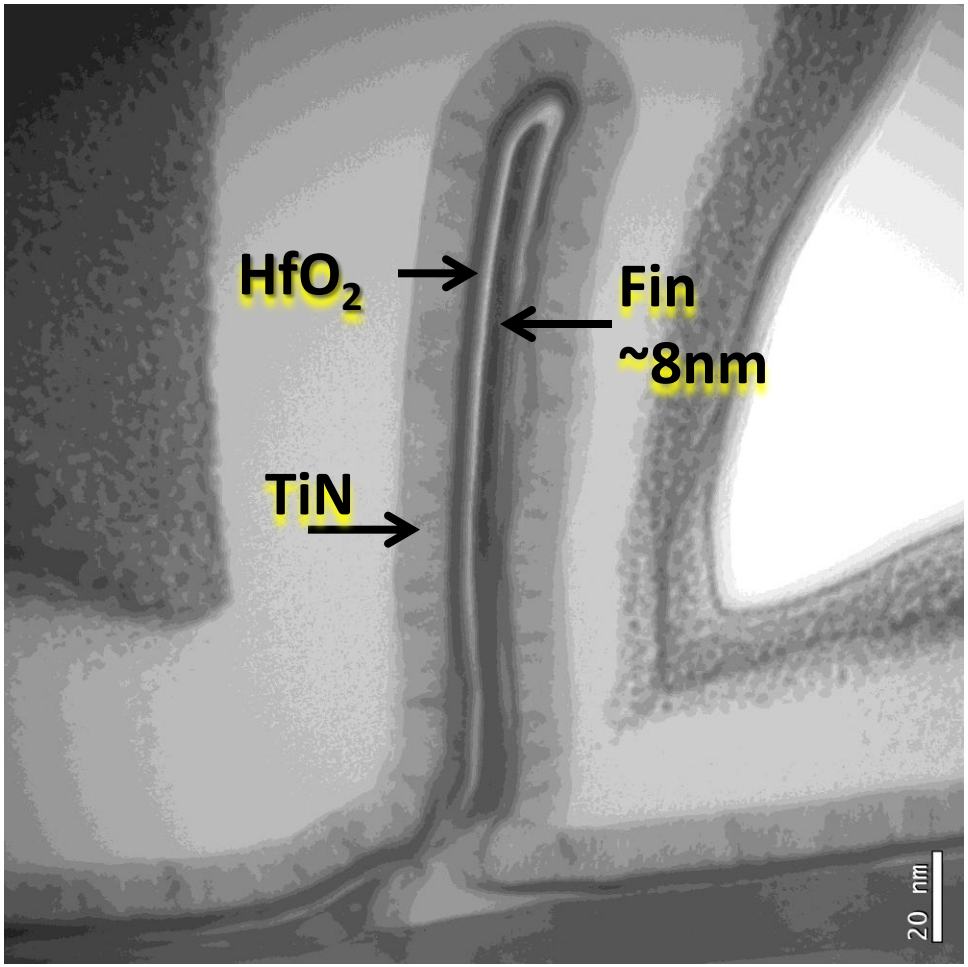
FinFETs by Atomic Layer Epitaxy

Fin thickness defined by Atomic layer epitaxy (ALE)

→ nm thickness control

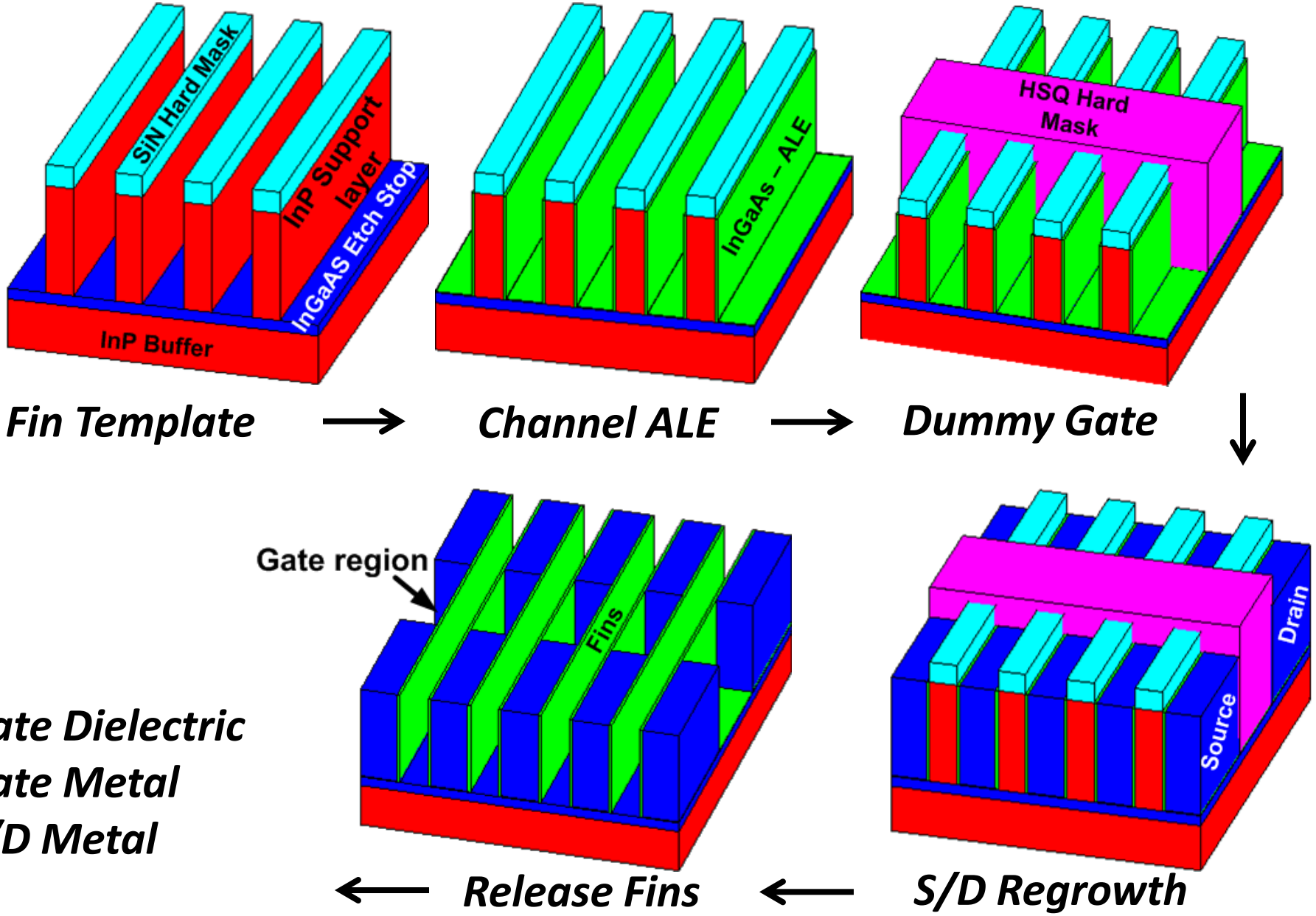
Fin height defined by sidewall growth

→ 200 nm high fins

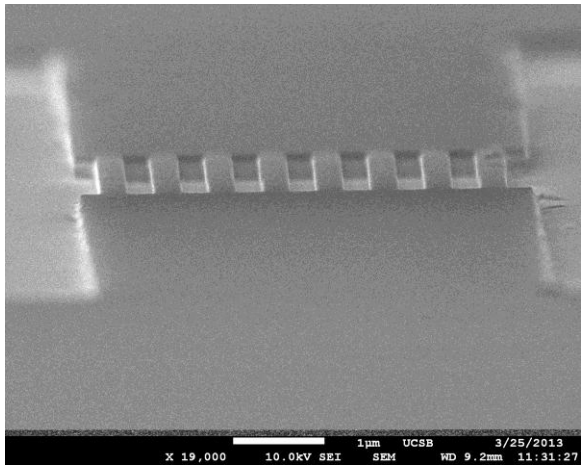


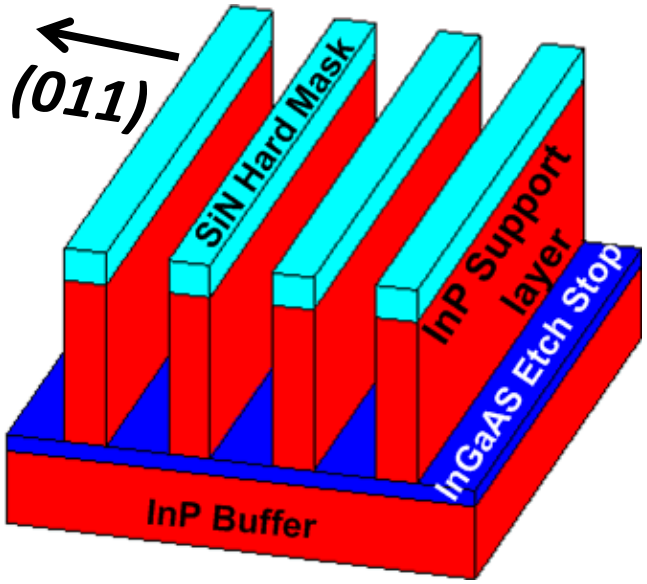
thin, tall fins → few-nm L_g, high currents

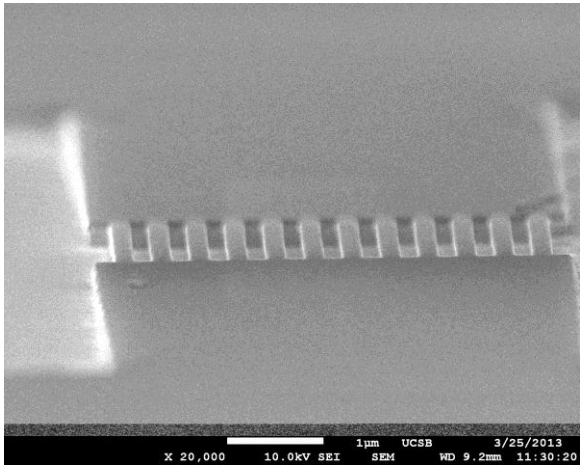
ALE-Defined finFET: Process Flow



Fin Template







SiN hard mask:

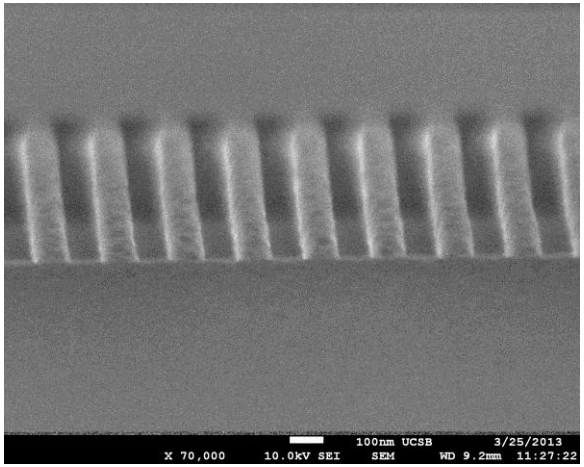
Ridges oriented along [011]

H_3PO_4 : HCL etch:

facet-selective, material-selective

forms vertical (011) sidewalls

stops on InGaAs etch-stop

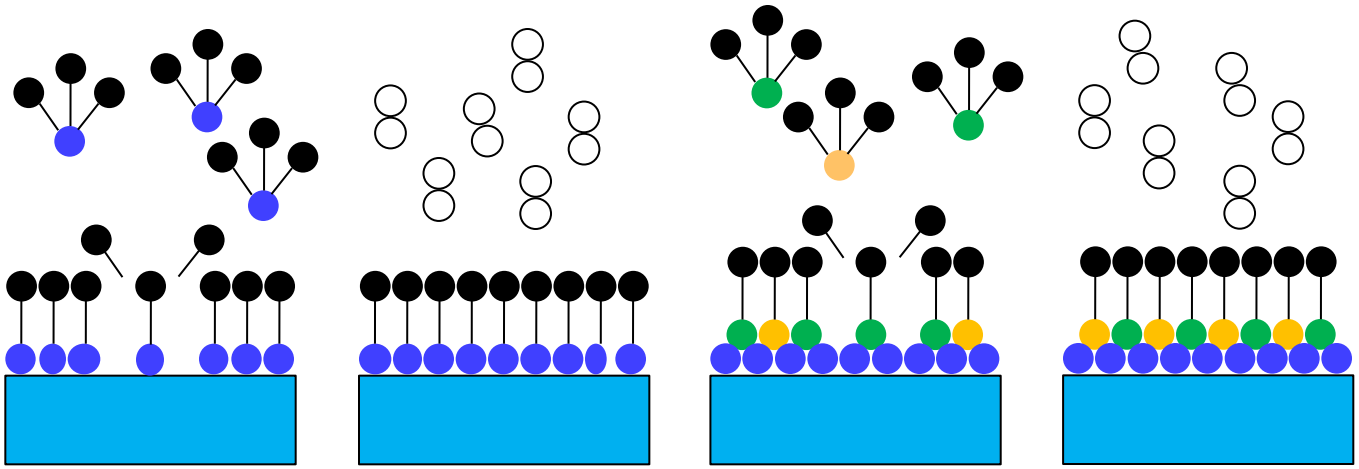


InGaAs etch-stop:

defines template height→ defines fin height

Channel Growth by Atomic Layer Epitaxy

1 monolayer growth per cycle.



← ***InGaAs monolayer ~ 2.9A***

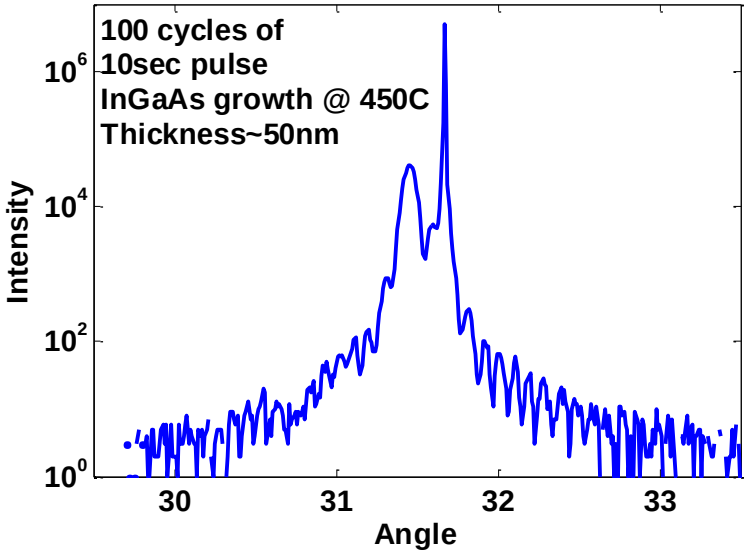
S.P. DenBaars, P.D. Dapkus
Journal of Crystal Growth, 98 (1989)

TBA flow → H_2 flow → TMI+ TMGa flow → H_2 flow

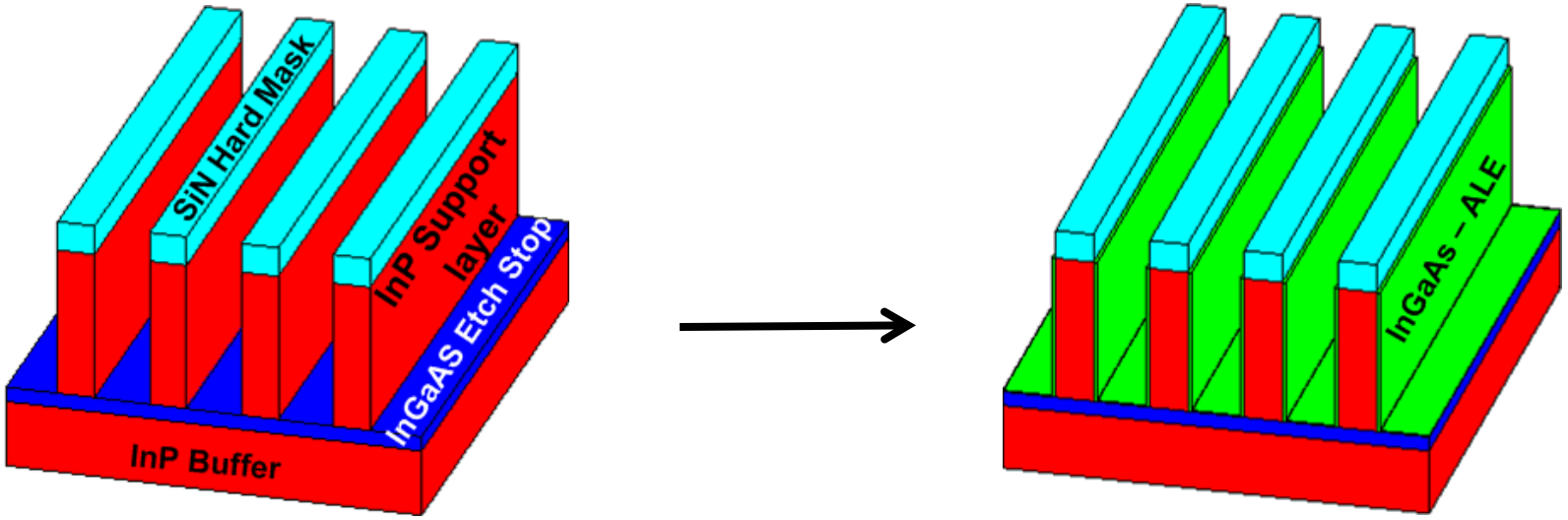
Using UCSB MOCVD :

1.7 Monolayer of InGaAs / Cycle

(Not true ALE mode)



Channel Growth by Atomic Layer Epitaxy



Growth:

lattice-matched InGaAs

20 ALE cycles → <10 nm channel

Masked growth:

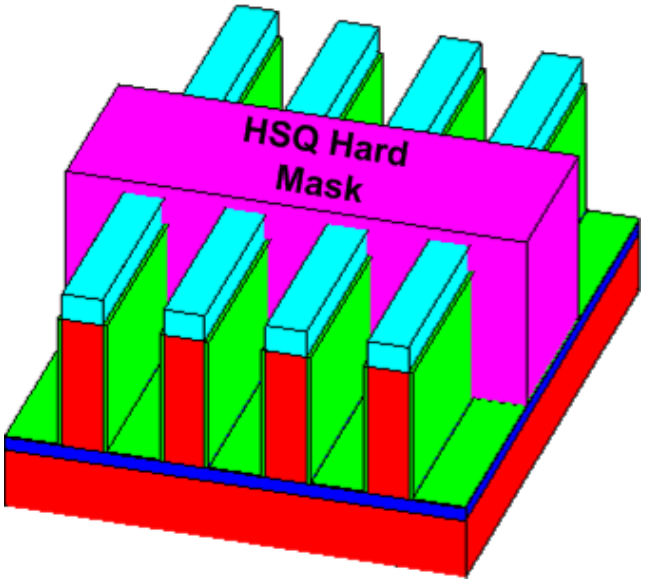
no InGaAs growth on top of template

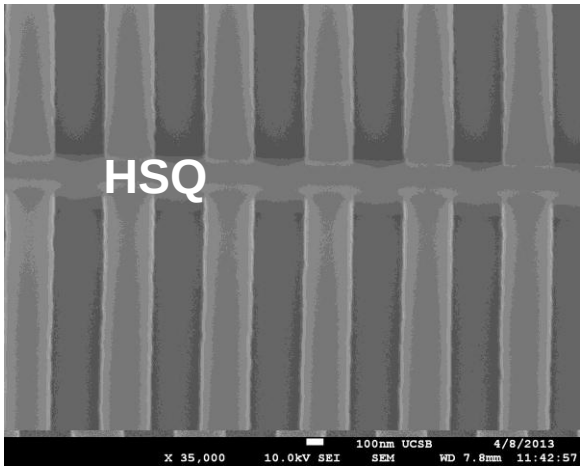
Details:

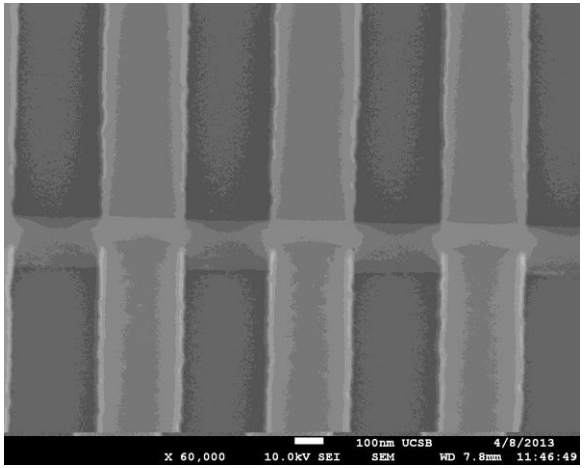
one ALE cycle = 10 sec TMGa/TMI, 10 sec H_2, 10 sec TBAs, 10 sec H_2

450 C growth

Dummy Gate: Patterns Source and Drain





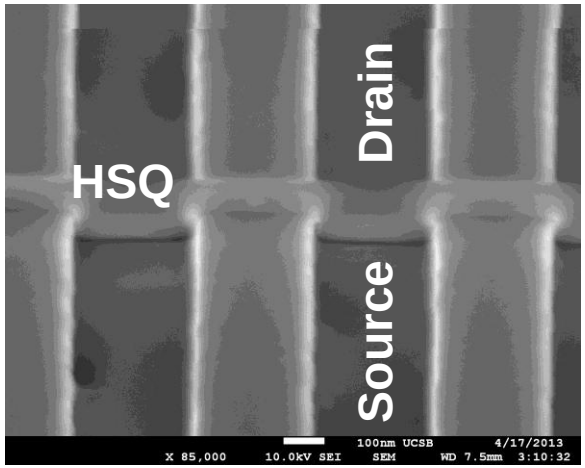


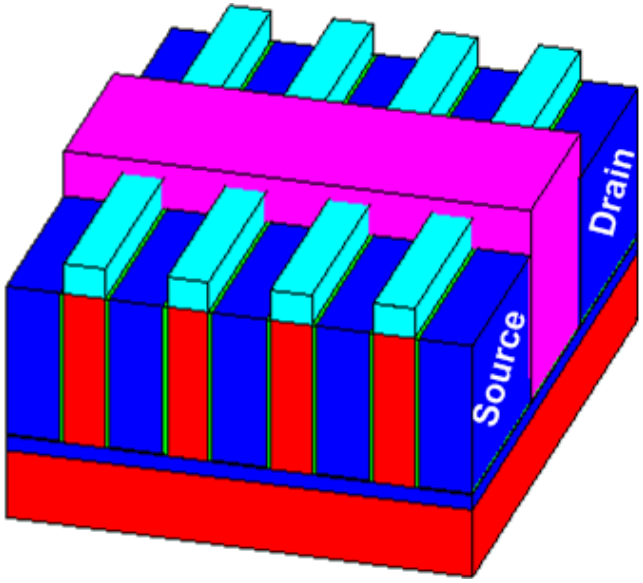
Mask

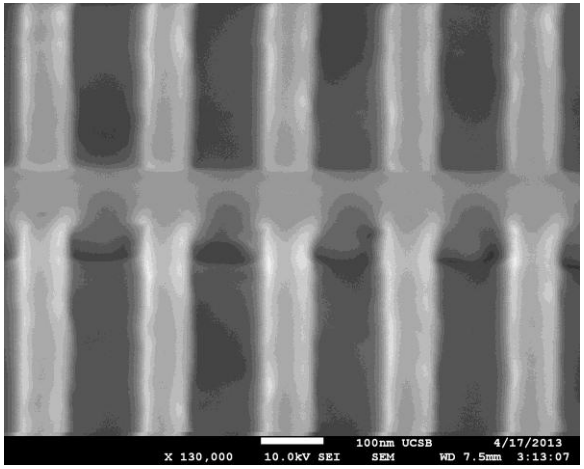
- ***HSQ* : E-beam definable SiO_2***
- ***ALD Al_2O_3 mask sub-layer: adhesion***

****HSQ: Hydrogen silsesquioxane***

Source Drain Regrowth







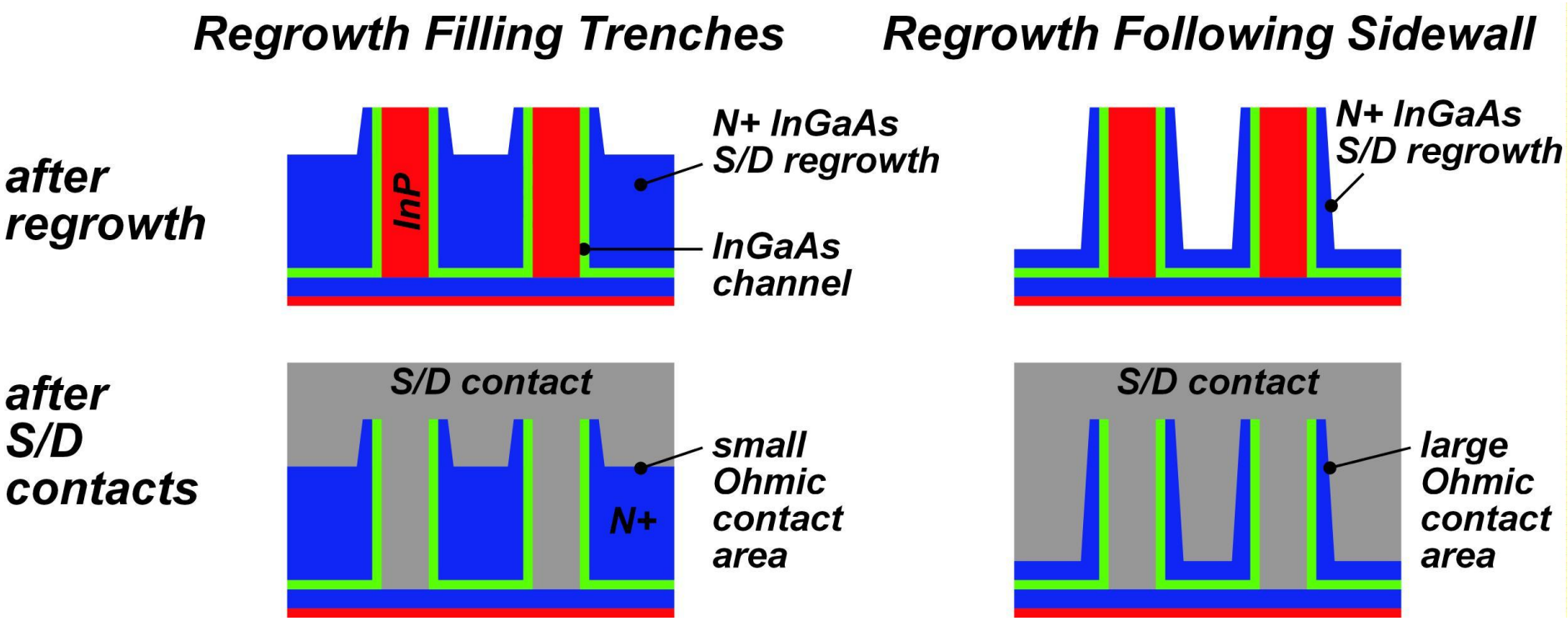
MOCVD Regrowth

600C

lattice-matched N+ InGaAs,

$5*10^{19}/cm^3$ doping

S/D Regrowth: Filling vs. Sidewall Regrowth



Present process:

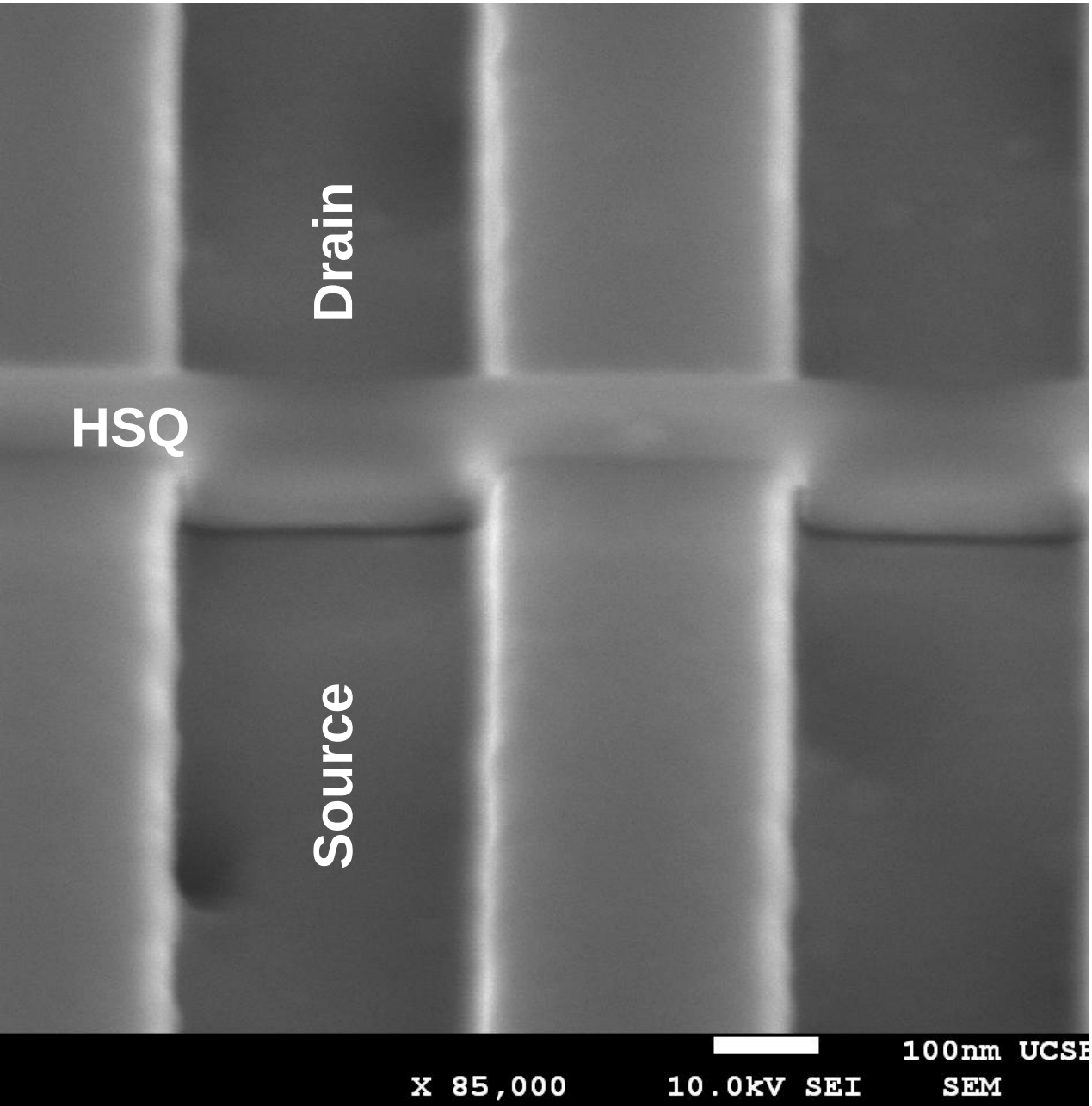
S/D regrowth partly fills spaces between fins

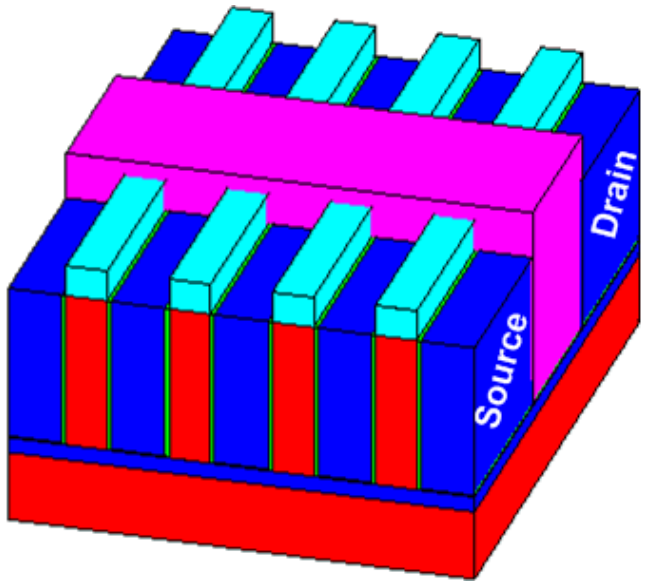
Target process:

S/D sidewall regrowth by ALE

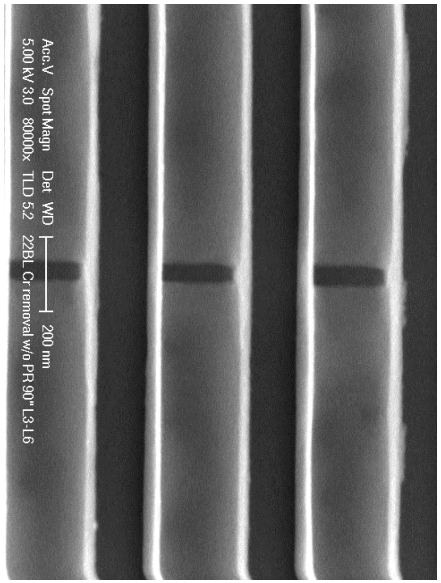
→ large contact area → low access resistance

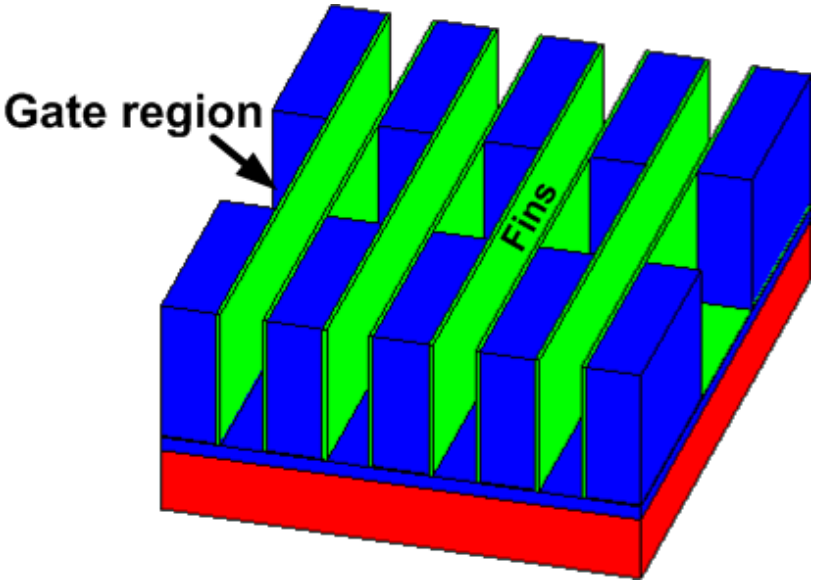
Source Drain Regrowth

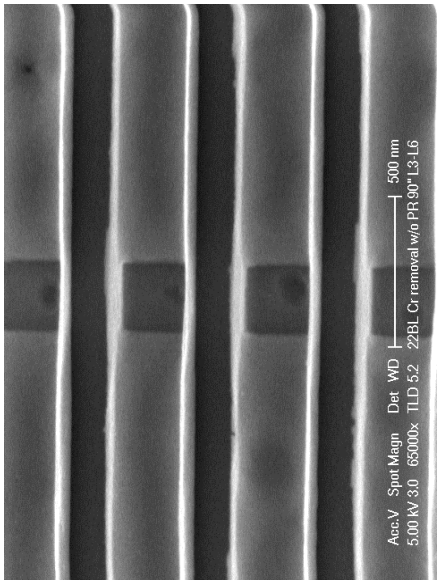




Fin Release



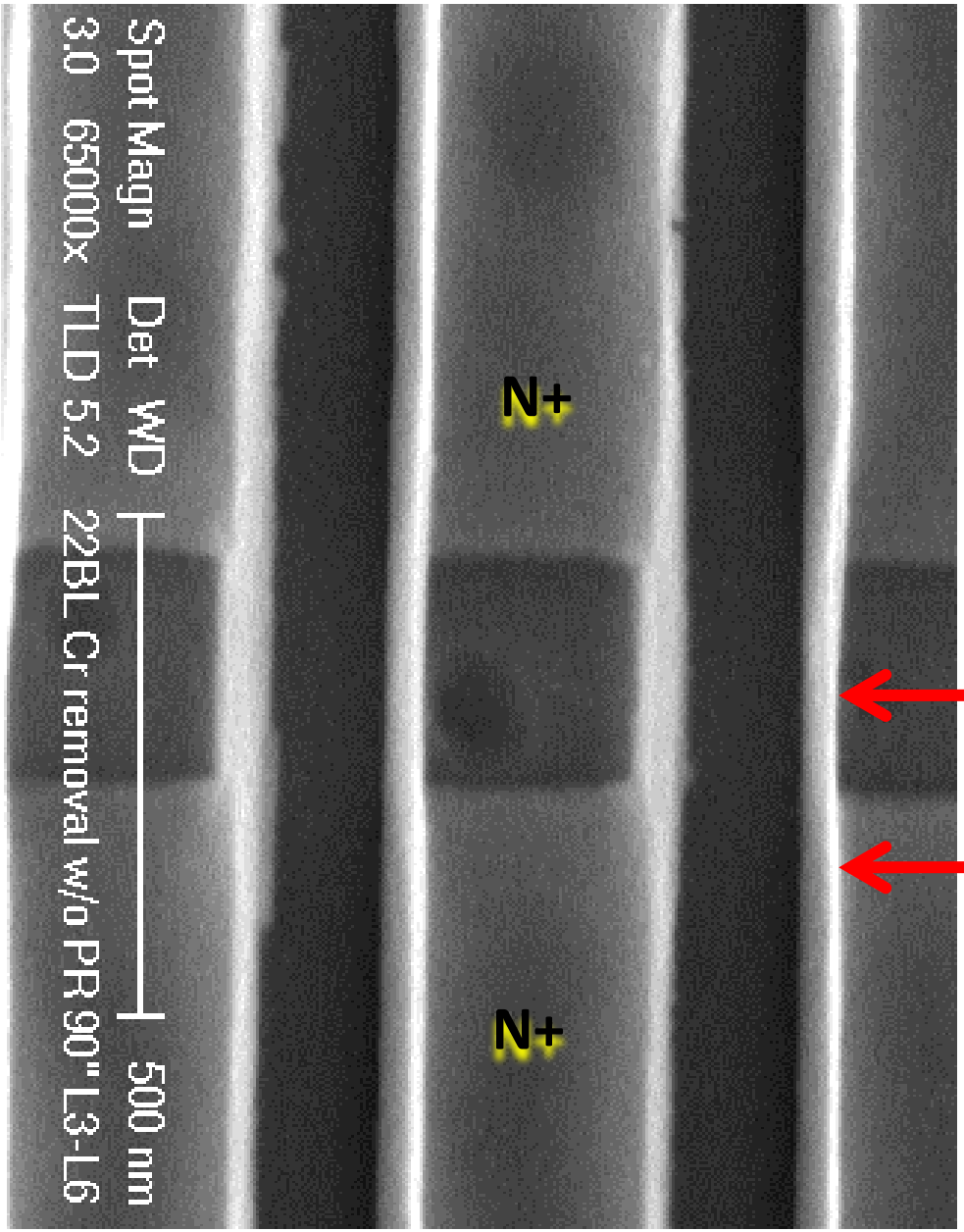


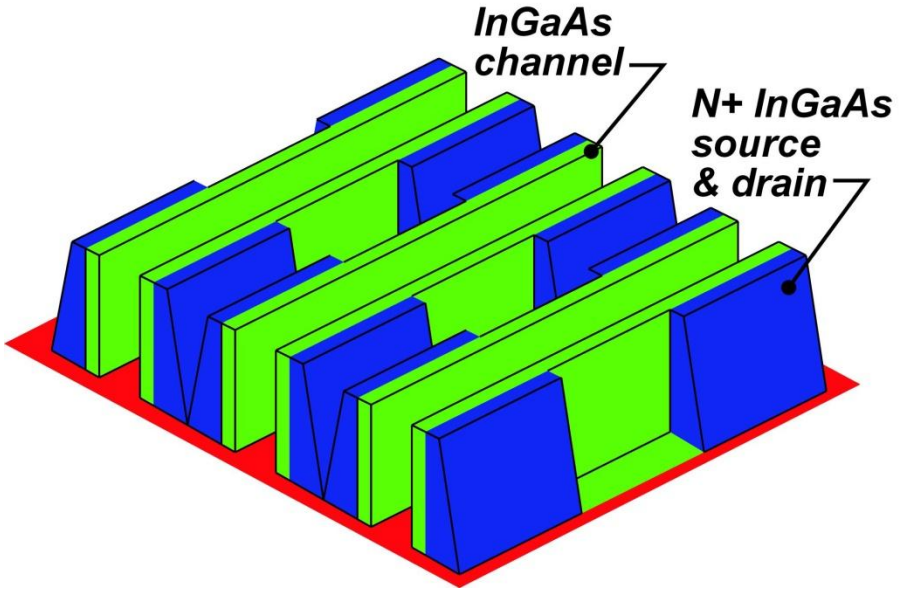


fin release:

- ***H_3PO_4:HCl selective wet-etch***
- ***etches InP***
- ***stops on InGaAs***

Fin Release



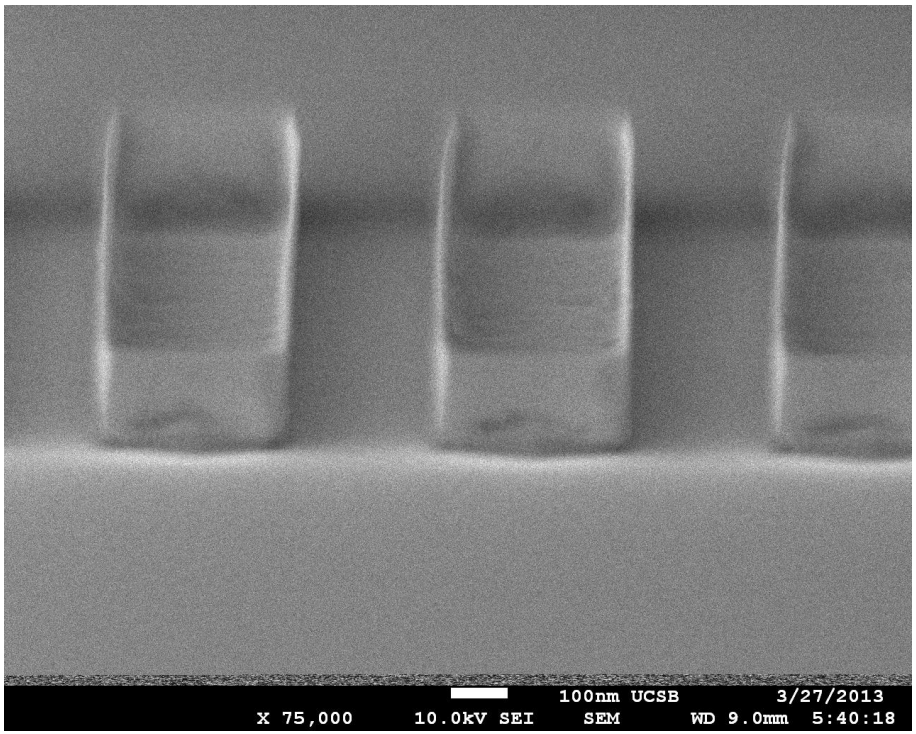


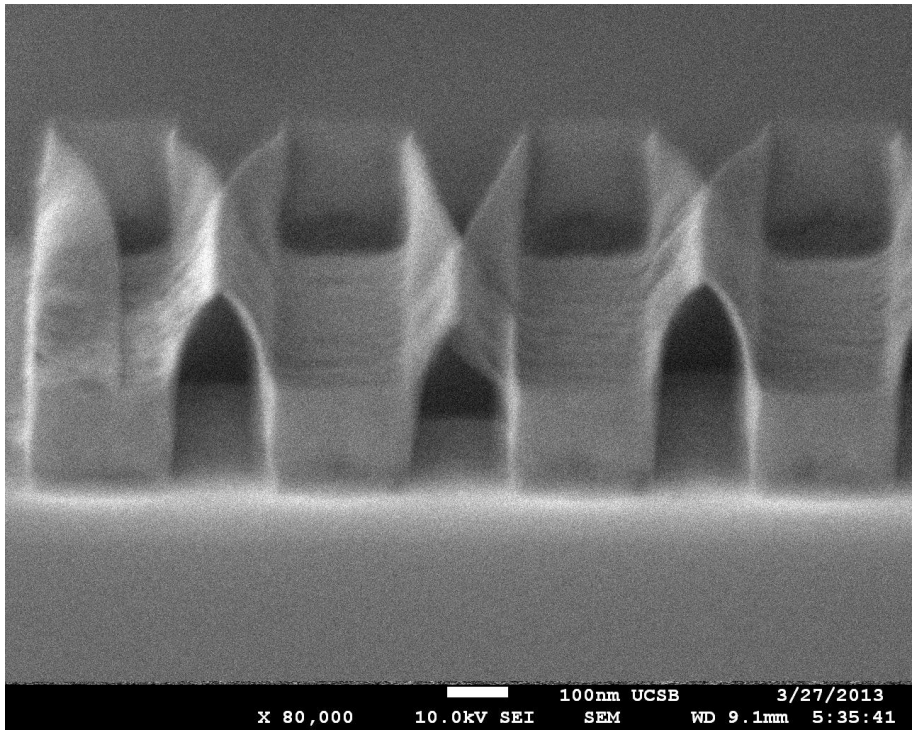
fin <u>without</u> N+ regrowth

fin <u>with</u> N+ regrowth

Why Not Release Fins Before S/D Regrowth ?

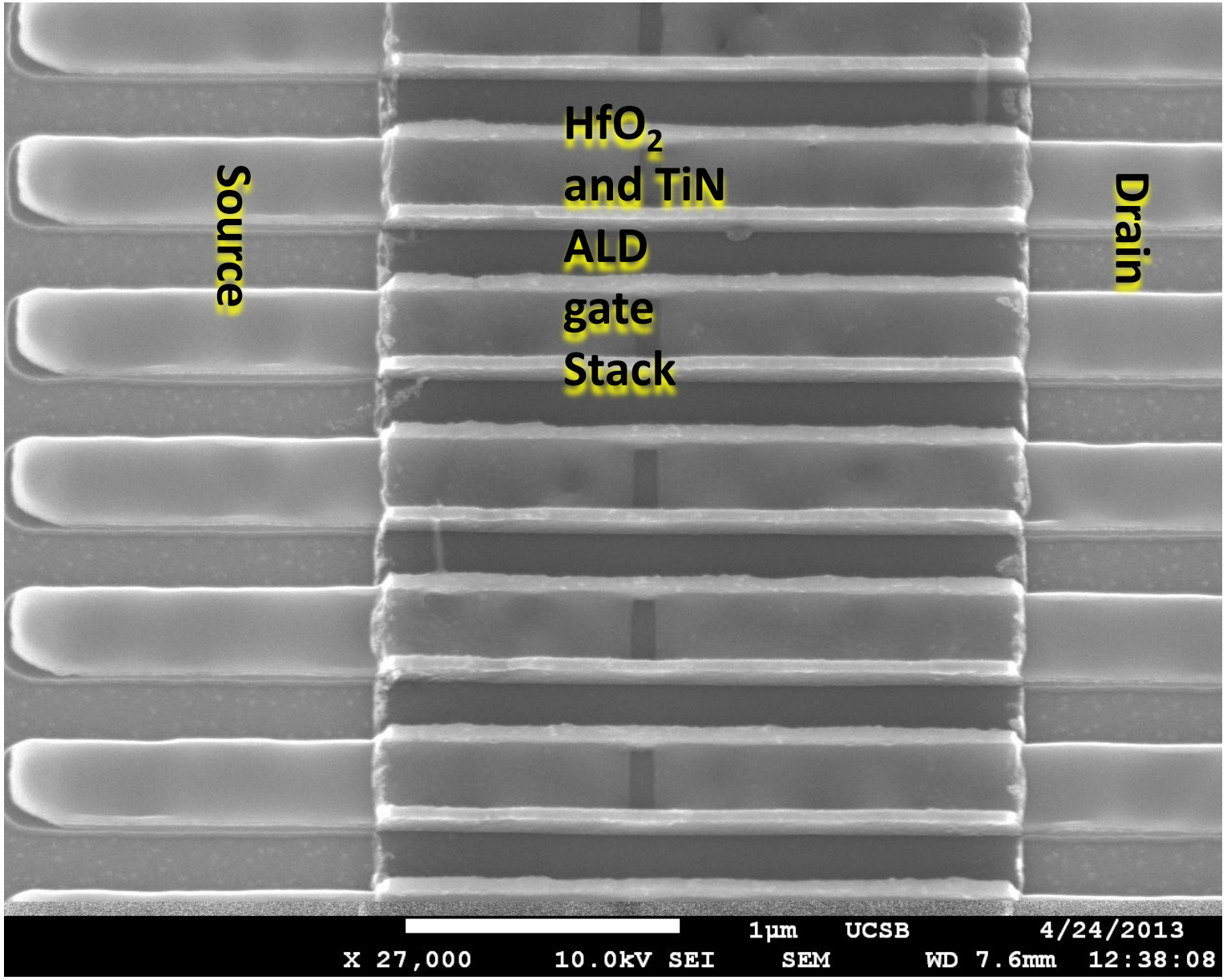
Images of released ~10 nm fins:



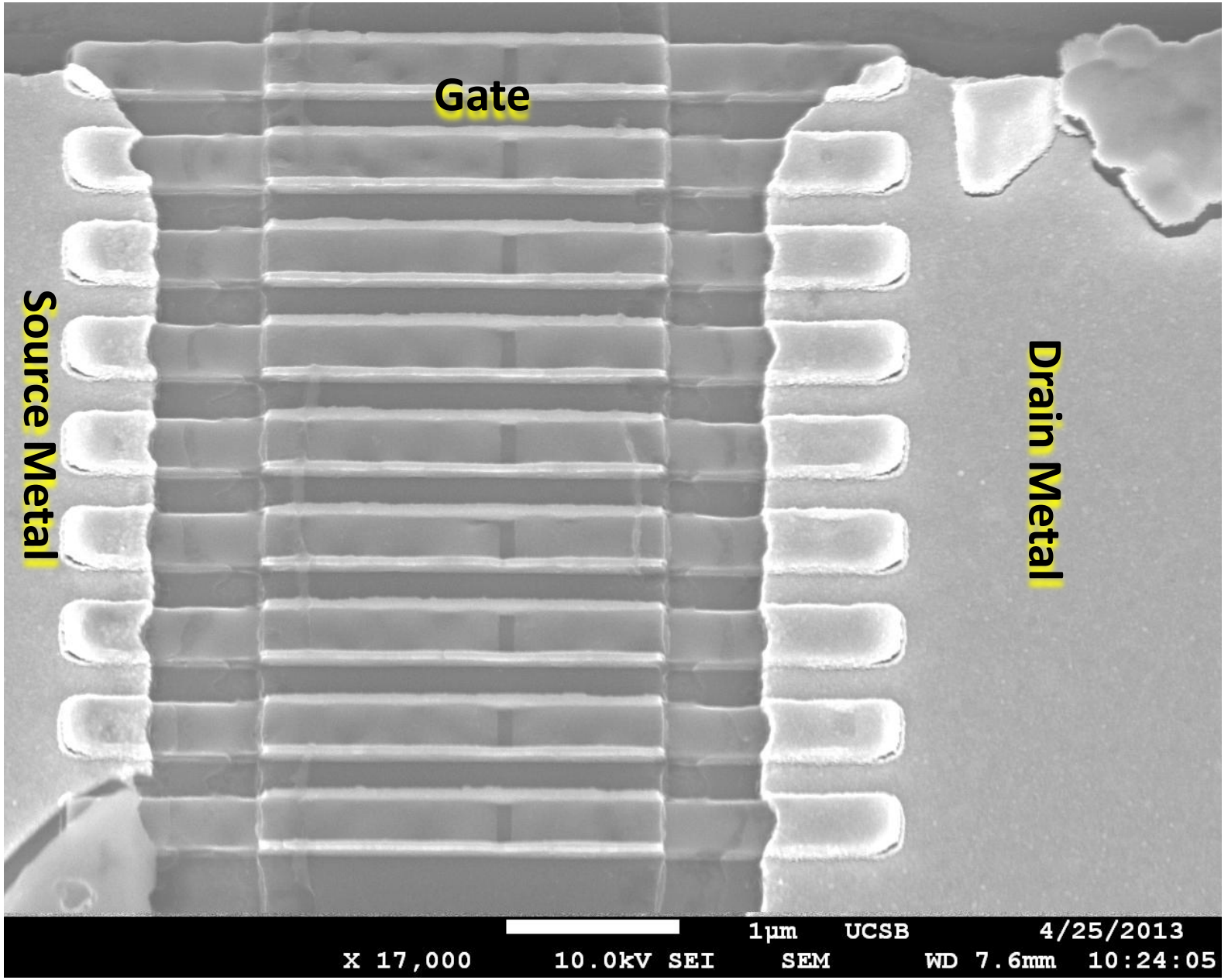


S/D regrowth provides mechanical support

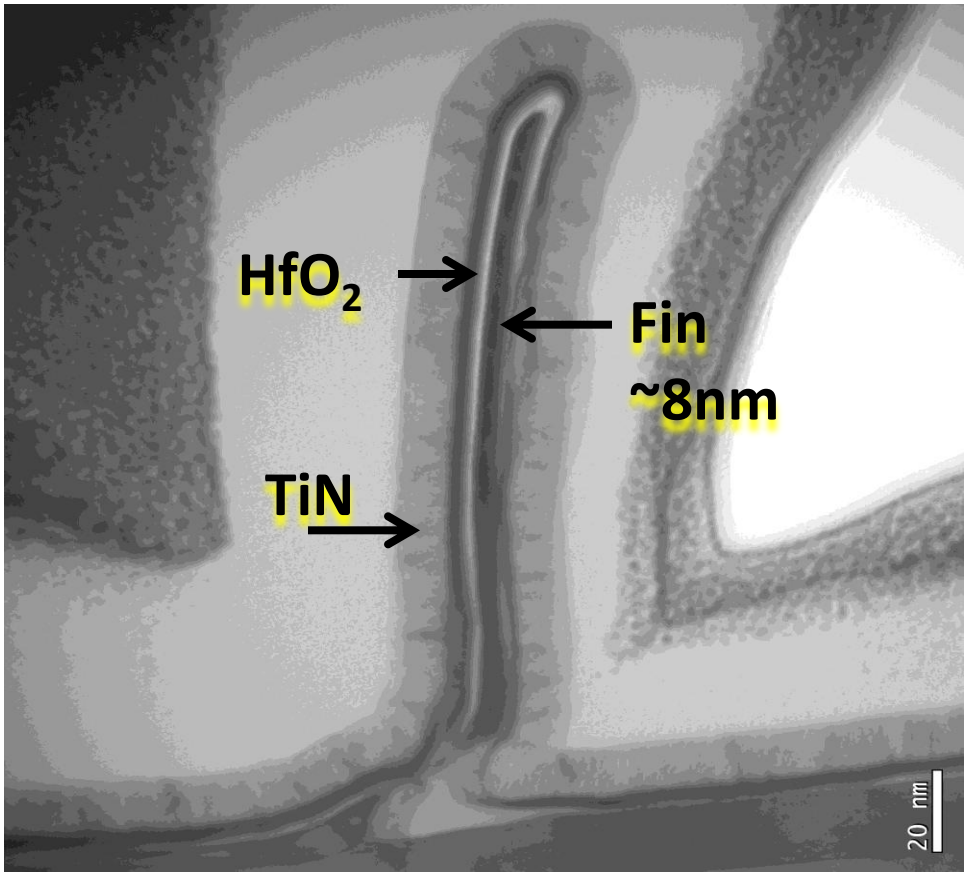
ALD Gate Dielectric, ALD Gate Metal

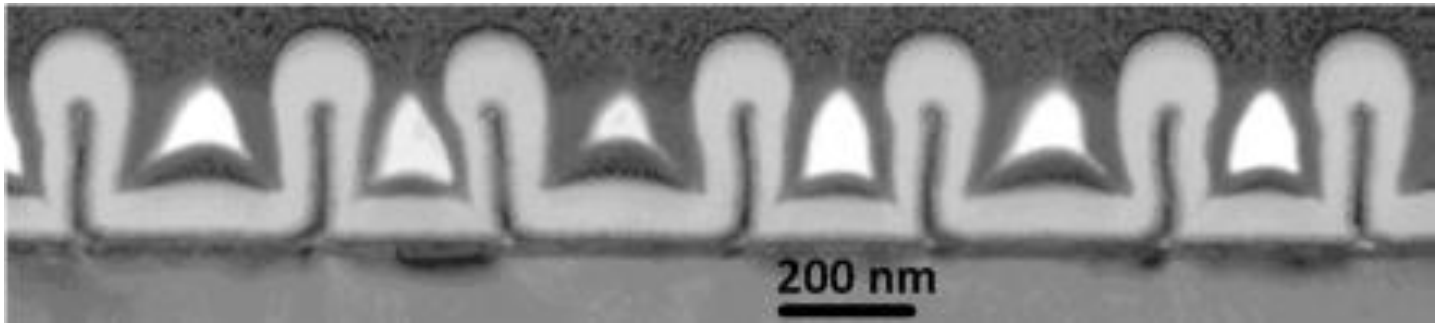


Source and Drain Metal



TEM Images





Where is the DC Data ?

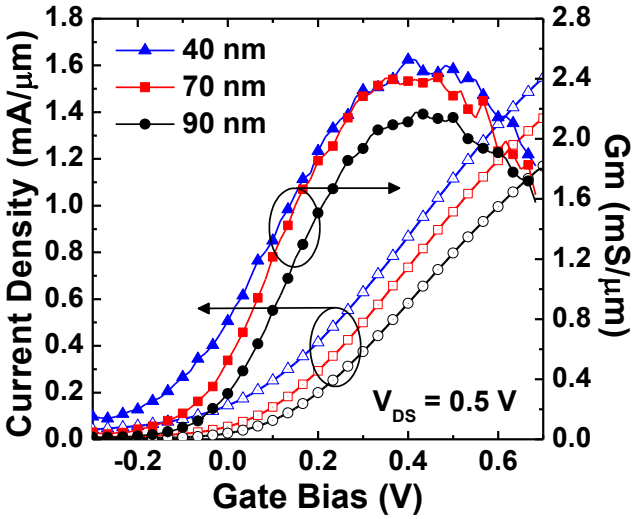
Present finFETs: very high leakage

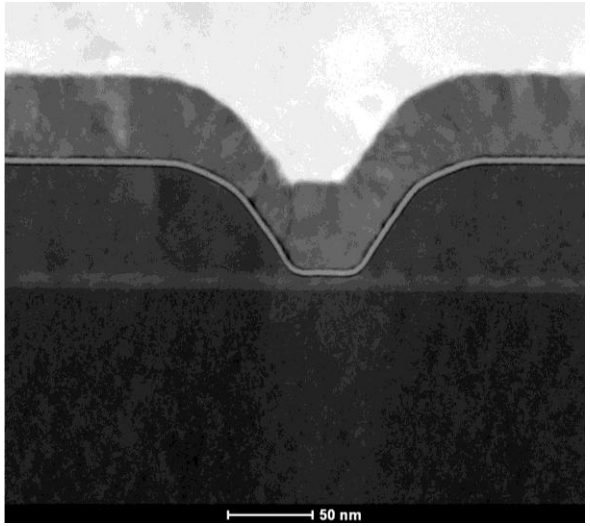
Planar FET: thermal Ni gate
finFET: ALD TiN gate
interface damage ?

Planar FET: 100 interface
finFET: 011 interfaces
ALD surface preparation ?

Planar InAs/InGaAs MOSFET

Lee et al, 2013 VLSI symposium

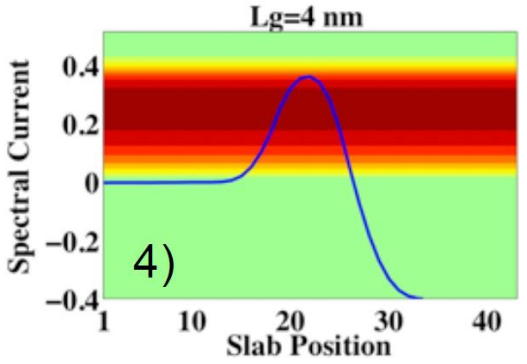




3-D Transistors to Extend Moore's Law

Lundstrom: high S/D tunneling @ 4-7 nm L_g
→ increase m* as L_g decreases

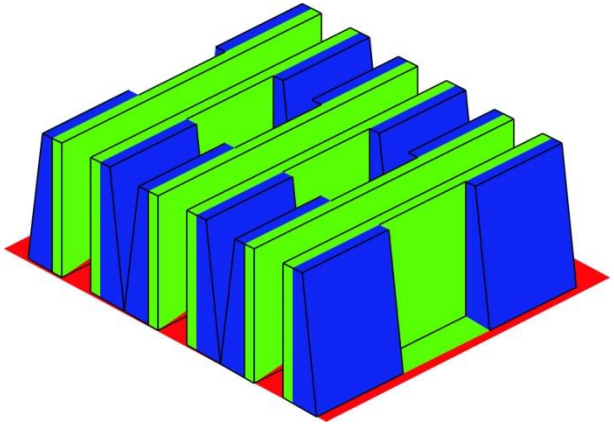
Implication: FETs won't improve with scaling
increased m* → decreased v_{inj}
→ decreased I_{on}, increased CV/I



M. Luisier, ETH Zurich / Purdue

If we scale only to increase the IC packing density, why reduce L_g ?

Alternative: 3-D integration



height>> pitch

...or other geometries...

FinFETs by Atomic Layer Epitaxy

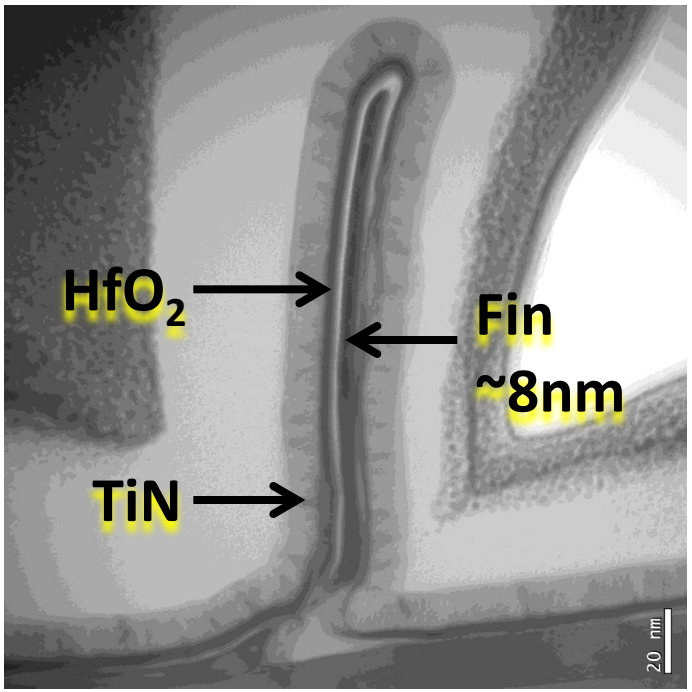
ALE-defined fin

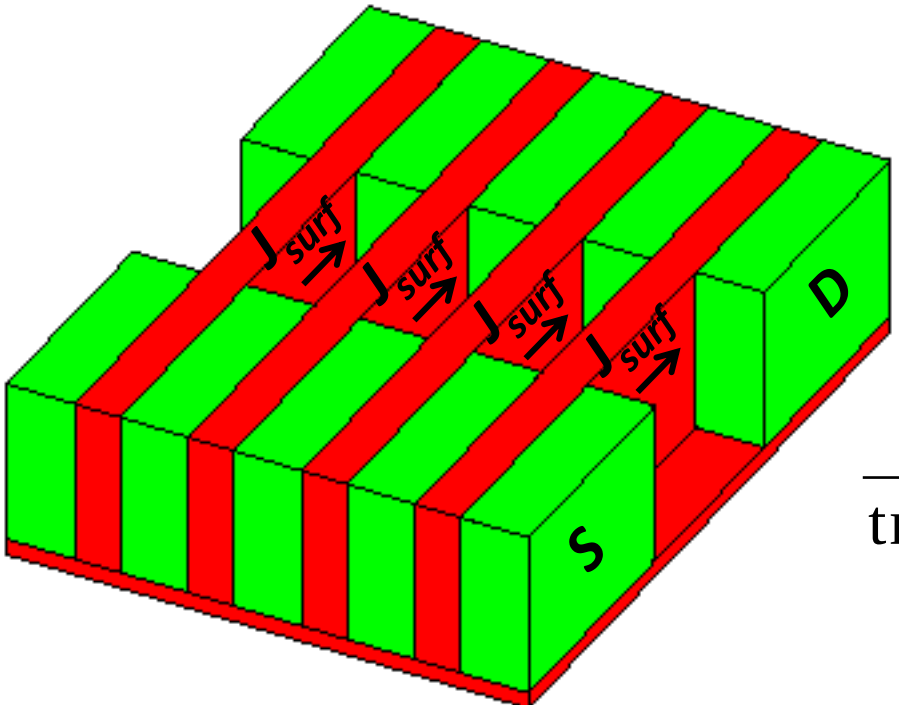
→ few-nm thick channels

→ scaling to 8nm gate length

200 nm fin height

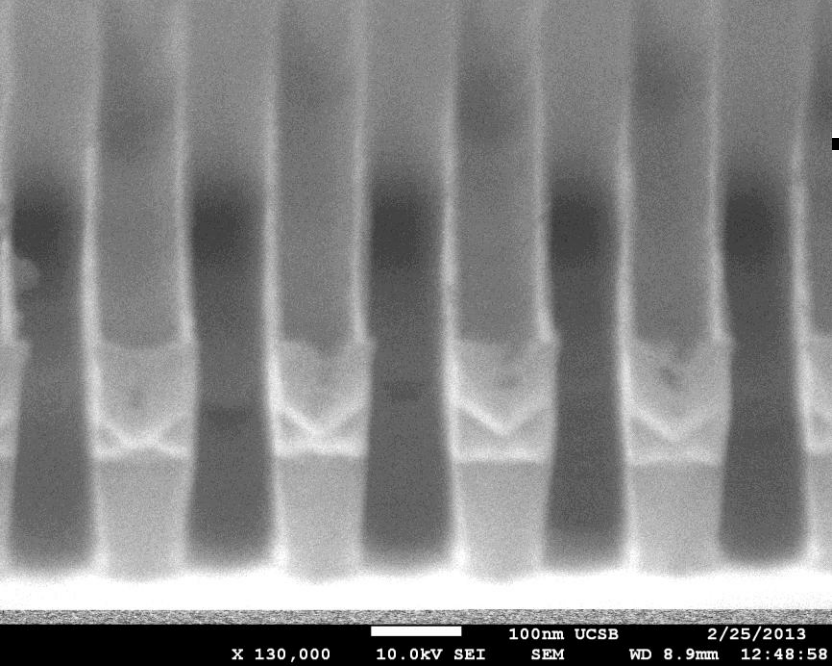
→enhance drive current

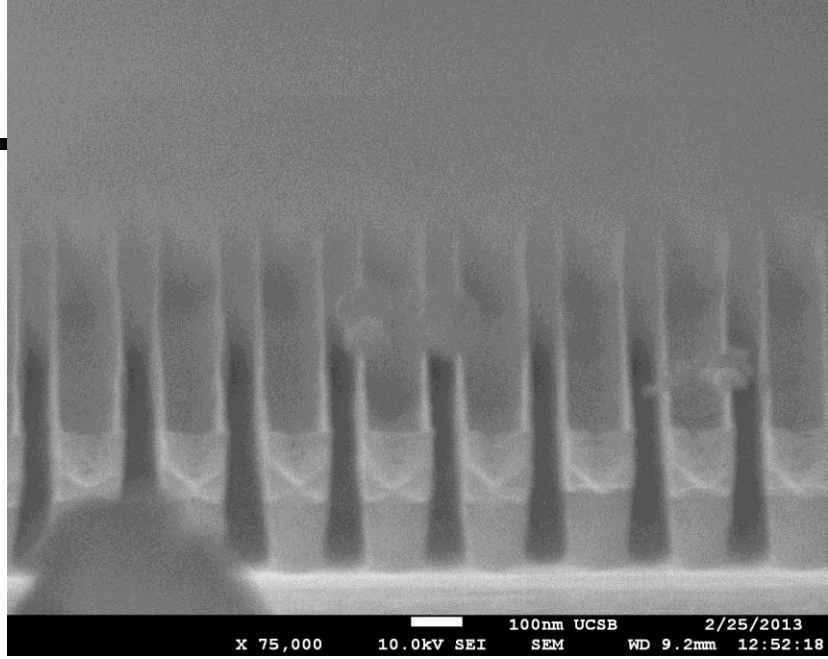




$$\frac{\text{current}}{\text{transistor width}} = J_{\text{surface}} \cdot \frac{\text{fin height}}{\text{fin pitch}}$$

Thank You


100nm UCSB 2/25/2013
X 130,000 10.0kV SEI SEM WD 8.9mm 12:48:58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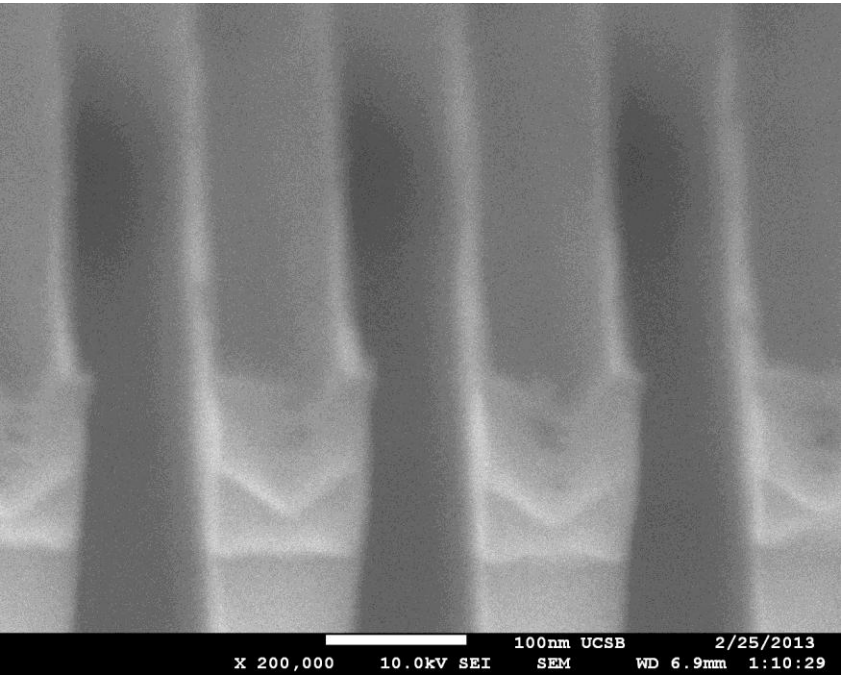
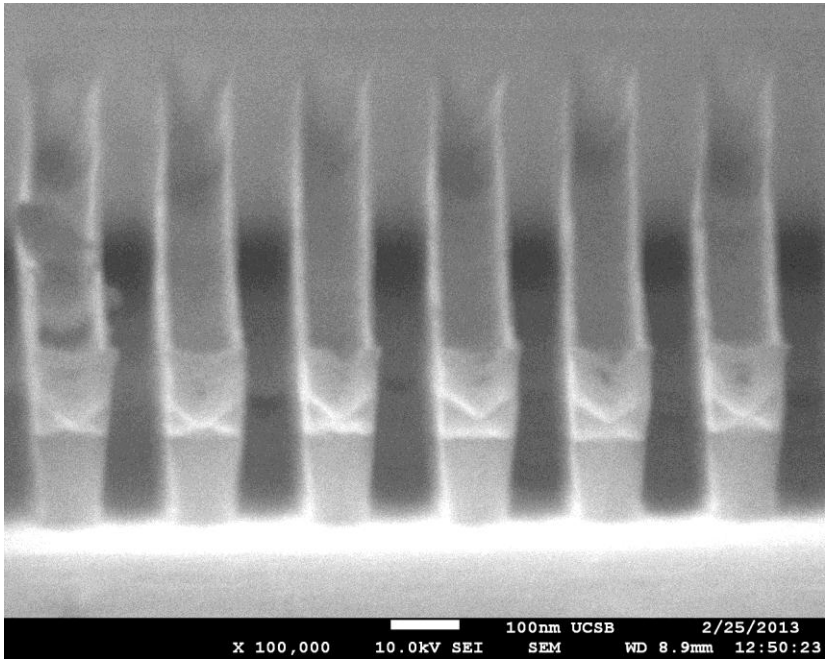

100nm UCSB 2/25/2013
X 200,000 10.0kV SEI SEM WD 6.9mm 1:10:29


100nm UCSB 2/25/2013
X 100,000 10.0kV SEI SEM WD 8.9mm 12:50:23