Monolithic Integration of a High-Speed Widely Tunable Optical Coherent Receiver

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Abstract—In this letter, a monolithically integrated widely tunable optical receiver is demonstrated. A sampled-grating DBR (SG-DBR) laser, an optical 90-degree hybrid, four high-speed uni-travelling-carrier photodetectors and microstrip transmission lines are integrated on a single InGaAsP/InP chip. A 42-nm tuning range and a 35-GHz detector bandwidth are achieved. Experiments show real-time reception of 40 Gb/s BPSK data.

Index Terms—Coherent receiver, photonic integrated devices, optical communications.

I. Introduction

WITH the fast growth of internet data streaming, a lot of recent efforts have been devoted to the research of coherent communications, which allows higher transmission capacity and higher sensitivity. As a key component of coherent communications, the demand for an integrated dual-quadrature coherent receiver with an integrated local oscillator (LO) is increasing dramatically.

Previous work has shown many coherent receiver designs [1]–[5] and some of them are already commercialized [4], [5]. However, in most of these coherent receiver designs the LO laser is usually not integrated monolithically [1], [4] mainly because of the limitation of the integration platforms. The work in [2], [3] demonstrated dual-quadrature coherent receivers with a LO laser integrated. However, the photodetector bandwidths are limited by the quantum-well PIN detector epitaxial structure.

In this letter, we will demonstrate a coherent receiver with a widely-tunable LO laser and high-speed uni-travelling-carrier (UTC) photodetectors integrated monolithically. Although this is a single-polarization coherent receiver, by combining two
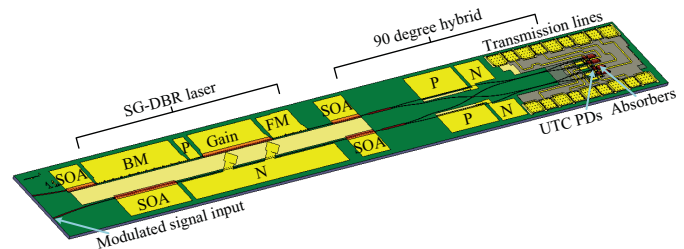
Fig. 1. To-scale picture of the PIC. The components are labeled (P: phase shifter. BM: back mirror. FM: front mirror. N: N contact and N pads).

such devices with an off-chip polarization splitter and rotator, a dual-polarization receiver can be achieved [3].

II. PIC Design

As mentioned above, a widely-tunable sampled-grating DBR (SG-DBR) laser [6], an optical 90-degree hybrid, four UTC photodetectors (PDs), and electrical transmission lines are monolithically integrated on an InGaAsP/InP photonic integrated circuit (PIC). The structure of the PIC is shown in Fig. 1. It has the same relative dimensions as the real device. The device size is 4.3 mm by 0.54 mm.

The grating sections of the SG-DBR laser are periodically blanked to generate comb-like reflection peaks. By careful design of the front and back mirrors, the reflective peak spacings are slightly different, which enables a sensitive frequency tuning of the lasing peak. The SG-DBR laser can sweep quasi-continuously across the whole optical C band (40 nm) [6].

The 90-degree hybrid design is shown in Fig. 1. It uses two 1-by-2 multi-mode interference (MMI) couplers as the first stage, which split the LO and the incoming signal into two paths, respectively. The symmetry of 1-by-2 MMI coupler ensures equal splitting. Directional couplers are used as the second stage couplers in the 90-degree hybrid, because they have minimum reflection and perfect 180 phase relation between the two outputs, regardless of splitting ratio. In a design aspect, a decrease of waveguide width will increase the coupling coefficient, while, on the other hand, the increase of the gap width will decrease the coupling coefficient. In real cases, the gap will increase when the waveguide width shrinks, and vice versa. The spacing between the waveguides is accurate, independent from fabrication errors. Thus by choosing the right waveguide spacing, these two effects can be canceled to
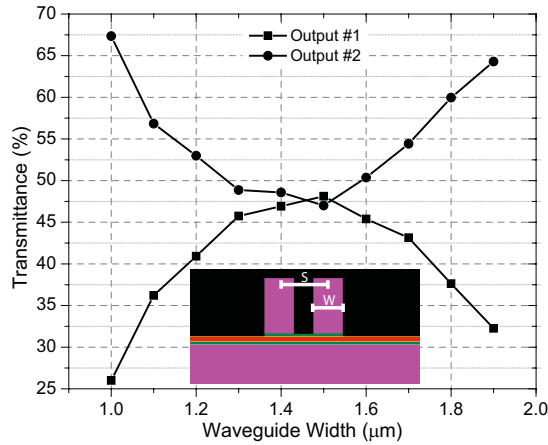
Fig. 2.   Simulated transmittance of the directional coupler. Outputs #1 and #2 represent the output power ratios from the two output waveguides, respectively, compared to the launched power. The x axis is the waveguide width (W), and the spacing between two waveguides (S) is 2.5 μm.
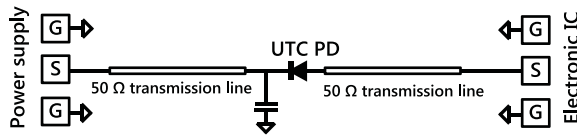

Fig. 3.   Circuit schematic diagram of the PD bias circuit on PIC.

first order, and the directional coupler dimensions can be very tolerant to waveguide width variation caused by fabrication. The waveguide etching depth is also a key factor for directional coupler fabrication. A surface ridge waveguide structure has been chosen, and a selective wet etch is used to finish the waveguide etching, as will be discussed in Section III. The etching depth is defined by metal-organic vapour phase epitaxy (MOCVD) growth, the accuracy of which is within 2% for each epitaxial layer.

The directional coupler design is shown in Fig. 2. By varying the waveguide width and fixing the waveguide spacing, the coupling ratio is shown. With a 0.3 μm fabrication error (from 1.3 to 1.6 μm), a decent splitting ratio (better than 47% : 53%) can be achieved according to the beam-propagation method simulation, as shown in Fig. 2. The radiation loss is around 5% from the waveguide bends and tapers on two sides of the directional coupler, which have also been taken into account in the simulation. The designed directional coupler has the following parameters: length = 145 μm, waveguide width (W) = 1.5 μm, waveguide spacing (S) = 2.5 μm.

Four UTC PDs are also integrated on this PIC as well as microstrip transmission lines. For our design, the UTC PDs have voltage supplies to both N and P-contacts [7]. The circuit model is shown in Fig. 3. P and N contacts are led to ground-signal-ground (GSG) pads on the edges of the PIC by transmission lines, and capacitors are also integrated to provide a high frequency ground on the PIC. The capacitance is around 1 pF, which is more than 50 times that of the UTC PD junction capacitance. The thickness of the absorber layer is designed to be 150 nm so that the effective index matches the fundamental mode in the waveguide, which enables the light

to couple into the absorber layer and therefore get absorbed quickly. The doping level of the absorber is also graded from 5×10^{17} to 2×10^{18} cm^{-3} to facilitate the electron transport in the absorber. The collector thickness is optimized to be 250 nm to get faster coupling and lower junction capacitance. With a size of 20 μm long and 3 μm wide, the designed quantum efficiency is above 95%, and with a 50 Ω load the 3-dB bandwidth can be above 50 GHz, depending on the contact resistance.

As shown in Fig. 3, two transmission lines need to be integrated for each UTC PD, and therefore there are totally 8 transmission lines on the PIC. Bisbenzocyclobutene (BCB) is used as the dielectric layer. An Au ground plane is needed beneath the BCB as the RF ground. In order to partially compensate the inductance introduced by wirebonds, the GSG pads are designed to be slightly capacitive. The GSG pad schematic can be found in Fig. 5. The pitch size is 100 μm, and signal pad size is 75-by-75 μm. The electromagnetic simulation results can be found in [7].

III. PIC FABRICATION

The PIC is designed and fabricated based on a semi-insulating (SI) InGaAsP/InP substrate and centered-quantum-well (CQW) waveguide structure [8]. The fabrication starts with the base epitaxial wafer, which contains a 1.1 Q (InGaAsP quaternary material with photoluminescence peak at 1.1 μm) N-contact layer, N-cladding layer, waveguide layers, CQWs, and 450 nm thick InP as the buffer layer for the quantum well intermixing process [9]. After an alignment marks etch, a patterned phosphorus ion-implant is carried out to define the active/passive areas on the wafer. The sample is then annealed at 675 $^{\circ}$C, and in consequence the photoluminescence (PL) peak of the implanted areas have a blue shift of around 130 nm, while the un-implanted areas stay almost the same. Therefore, the active (PL peak: 1550 nm) and passive (PL peak: ~1420 nm) areas are defined. After removing the implant buffer layer and the stop etching layer, a blanket MOCVD UTC-PD regrowth is carried out. Using Si_3N_4 as a hard mask, UTC layers are then removed from most of the wafer by wet etch, left in only the places where UTC PDs will be defined in the later steps. Gratings for the SG-DBR laser are then defined using electron-beam lithography, and a Methane-Hydrogen-Argon (M/H/A) reactive-ion-etch (RIE) is used to etch the gratings. The grating pitch size is 238 nm, and the etching depth is 80 nm into the top waveguide layer. A scanning electron microscope (SEM) picture of the finished gratings is shown in Fig. 4(a). Following the grating step, a second blanket MOCVD regrowth is fulfilled. The P-cladding layer, P-InGaAs contact layer, and top InP sacrificial layer are grown. The full epitaxial structure is shown in Table I. The rows with a shaded background show the UTC layers, and the normal waveguide structure contains all the layers except the UTC layers.

Following the second regrowth is the waveguide definition, which consist of multiple dry etches and wet etches. M/H/A RIE is used for the waveguide dry etching, and it etches through the top InP sacrificial layer and the contact layer.
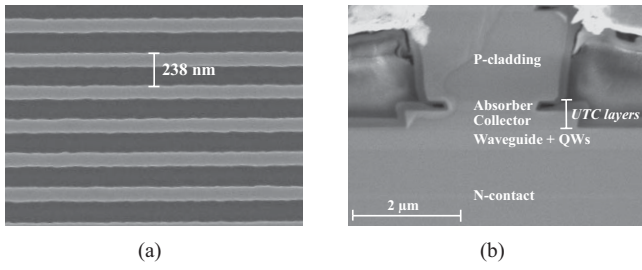
Fig. 4. (a) An SEM picture of the gratings with a pitch size of 238 nm. (b) An SEM picture of the cross section of a fully-fabricated UTC photodetector.

TABLE I

FULL EPITAXIAL STRUCTURE

No.	Material	Thick (nm)	Doping (cm^{-3})	Function
1	InGaAs:Zn	150	2E19	P-contact
2	InP:Zn	1800	5E17-1E18	P-cladding
3	InP:Zn	200	5E17-1E18	P-cladding
4	InGaAs:Zn	50	2E18	**Absorber**
5	InGaAs:Zn	50	1E18	**Absorber**
6	InGaAs:Zn	50	5E17	**Absorber**
7	InGaAs	8	UID	Band smooth
8	1.24Q	16	UID	Band smooth
9	InP	6	UID	Band smooth
10	InP:Si	7	1E18	Band smooth
11	InP	250	UID	**Collector**
12	InP:Si	30	1E18	Subcollector
13	1.33Q:Si	20	1E17	Etch stop layer
14	InP:Si	5	8E16	Regrowth layer
15	InP:Si	30	5E16-8E16	Regrowth layer
16	1.3Q:Si	105	5E16	Waveguide
17	10 QWs	153	UID	Quantum Wells
18	1.3Q:Si	105	1E17	Waveguide
19	InP:Si	850	1E18	N-cladding
20	1.1Q:Si	100	1E18	N-contact
21	InP:Si	1000	1E18	N-cladding
22	InP:Fe			SI Substrate

Fig. 5. Cross sections of the fabricated PIC.

TABLE II

UTC LAYER ETCHING PROCESS

Etch Steps	Removed UTC Layer	Removed Waveguide Layer
InGaAs wet etch	InGaAs absorber	~25 nm 1.3 Q layer
M/H/A dry etch	1.24 Q layer	~25 nm 1.3 Q layer
InP wet etch	InP collector layer	Negligible
M/H/A dry etch	1.33 Q layer	~30 nm 1.3 Q layer
InP wet etch	InP regrowth layer	Negligible
Summary	All UTC layers	~80 nm waveguide layer

An HCl-based wet etch is applied to finish the waveguide definition, and the etch stops accurately at the top waveguide layer. At this point, the gap of the directional coupler needs to be protected. A 10-nm atomic layer deposition (ALD) Al_2O_3 film and a 100-nm plasma-enhanced chemical vapor deposition (PECVD) Si_3N_4 film are deposited. The ALD Al_2O_3 film is used as a stop etch for the Si_3N_4 dry etch. After protective Si_3N_4 definition, the Al_2O_3 film in open areas is removed by a strong base, AZ400K developer. After that, several M/H/A RIE and wet etches are carried out alternatively to remove the UTC layers beside the UTC PDs. The to-be-etched UTC layers, from top to bottom, are layer 4 - 15 shown in Table I. Several wet etches and dry etches are carried out alternatively, and the processing steps are shown in Table II, in which H_2SO_4:H_2O_2:H_2O (1:1:10) is used for InGaAs wet etch, and HCl:H_3PO_4 (1:3) is used for InP wet etch. During these etches, the normal waveguide is also etched around 80 nm into the waveguide layer (No. 16 in Table I) except the protected directional coupler gaps. The cross section of a UTC detector is shown in Fig. 4(b). The undercut of the InGaAs absorber is because of the wet etch. It is also noticed that the collector is wider than the P-cladding layer, which is mainly caused by the masking of the top of the waveguide during the dry etch process.
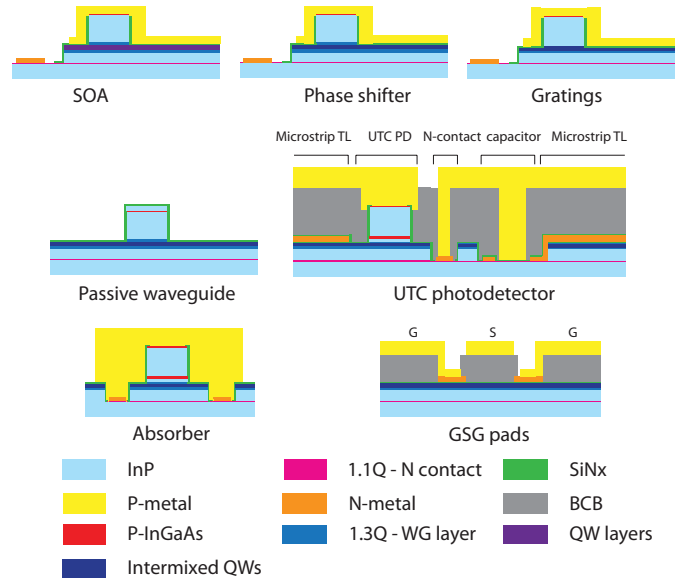
Finally, the wafer is thinned down, and backside metallization is carried out. After cleaving and facet anti-reflective coating, the samples are ready for testing. The whole process includes 2 MOCVD regrowths, > 20 lithographies, and 2 ion implantations. The schematics of the cross sections of the fully fabricated PIC are shown in Fig. 5, and an SEM picture of the PIC can be found in Fig. 6.

IV. TESTING RESULTS

The PIC has been fully characterized. The SG-DBR laser covers from 1541 nm to 1583 nm without temperature tuning. The optical spectra of the super-modes are shown in Fig. 7(a). The side-mode suppression can be further improved if the output power is higher. The preliminary result shows a self-heterodyne linewidth of around 10 MHz [7], [10], and the low-frequency linewidth drift is within 100 MHz. The output power can be as high as 20 mW without the boosting amplifier. The ac response of the phase diode of the SG-DBR has also been
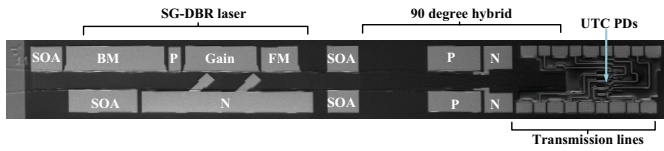
Fig. 6.   An SEM picture of the fabricated PIC. The components are labeled (P: phase shifter. BM: back mirror. FM: front mirror. N: N contact and N pads).
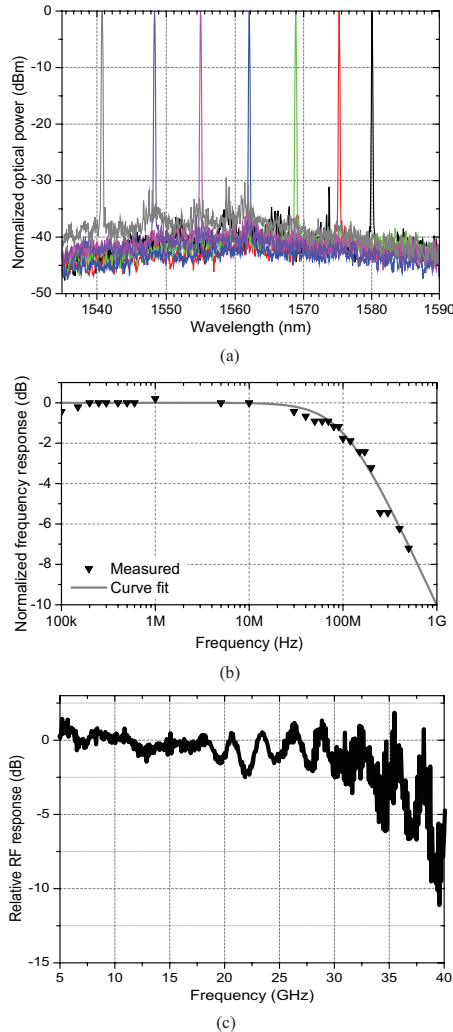

Fig. 7.   (a) Optical spectra of the SG-DBR laser lasing at different mirror super-modes. The resolution bandwidth is 0.1 nm. (b) Relative frequency response of the phase section diode in the SG-DBR laser. (c) Shows optical-electrical response of the UTC PD. The 3-dB bandwidth is 35 GHz [12].

characterized by measuring the modulation side peaks after applying a small RF signal on the phase diode. The relative E-O response is plotted in Fig. 7(b). The pole at 100 MHz is introduced by the minority carrier lifetime ($\sim$1.6 ns). The low-frequency tuning sensitivity is around $5 - 10$ GHz/mA, depending on how the lasing cavity mode is aligned to the mirror reflectivity. The relative fast RF response of the phase section diode is favorable for opto-electrical feedback systems [7], [10], [11].

The UTC photodetector is measured by a lightwave component analyzer, and it shows a 35 GHz 3-dB bandwidth

with -2 Volts bias as shown in Fig. 7(c). It is measured with the device wirebonded. By direct probing on chip, similar results have been observed. The main limit of the RF bandwidth is from the high contact resistance, which can be solved by increasing the doping level of P-InGaAs or by improving the surface preparation before P-contact metal deposition.

Since the phase relation of the 90-degree hybrid is adjustable by injecting current into the on-PIC phase shifter, the output phase is exact. The power imbalance is within 5%.

A system measurement is also carried out. By using this integrated coherent receiver PIC, an optical Costas receiver is built, and 40 Gbit/s BPSK demodulation is achieved. The bit error rates from 20 Gbit/s up to 40 Gbit/s are measured [7], [10].

V. Conclusion

In summary, a highly-integrated widely-tunable optical dual-quadrature coherent receiver has been demonstrated. An SG-DBR laser, a 90-degree hybrid, four UTC photodetectors and microstrip transmission lines are integrated monolithically. Device characterization and system measurements are shown.

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