Record Extrinsic Transconductance (2.45 mS/μm at V_{DS} = 0.5 V) InAs/$In_{0.53}Ga_{0.47}As$ Channel MOSFETs Using MOCVD Source-Drain Regrowth

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Abstract: We report InAs/$In_{0.53}Ga_{0.47}As$ channel MOSFETs using source-drain regrown contact and surface digital etching. A device with 40 nm-L_g shows 2.45 mS/μm extrinsic peak transconductance g_m at V_{DS} = 0.5 V and 214 Ω-μm R_{on}. A long-channel device (L_g = 510 nm) exhibits 1.06 mS/μm g_m at V_{DS} = 0.5 V and 93 mV/dec at V_{DS} = 0.05 V. At all gate lengths, the devices exhibit the highest extrinsic g_m among published results on III-V MOSFETs and MOSHEMTs.

Introduction: Due to the excellent electron transport properties, $In_xGa_{1-x}As$-based MOSFETs have been widely investigated as promising candidates for future VLSI [1]-[7]. Among various design prototypes, substitutional-gate with source-drain (S/D) regrowth can be considered a viable design scheme at sub-10 nm node since it enables heavily-doped S/D regions without dry-etching of a gate metal stack, or "trench" etching with etch-stop layers. In such a device, however, performance can be degraded by damage to the channel surface during regrowth [8]. Here, we demonstrate InAs/$In_{0.53}Ga_{0.47}As$ MOSFETs using MOCVD S/D regrowth and a substitutional-gate process. Employing surface digital etching [7]-[8], one can remove the damaged semiconductor surface and also control the channel thickness with nearly nanometer precision. The devices fabricated show the highest peak extrinsic transconductance (g_m) at all gate lengths among reported III-V MOSFETs.

Device Fabrication: The epitaxial layers, grown on a semi-insulating InP substrate by molecular beam epitaxy, consist of the following: a 400 nm unintentionally doped $In_{0.52}Al_{0.48}As$ buffer/barrier layer, a 3 nm Si-doped (3.9×10^{12} cm^{-2}) $In_{0.52}Al_{0.48}As$ pulse doping layer, a 3 nm $In_{0.53}GaAs$ bottom cladding layer, a 5 nm InAs channel (strained), a 3 nm $In_{0.53}Ga_{0.47}As$ top cladding and a 5 nm Si-doped ($4\text{-}5\times10^{19}$ cm^{-3}) $In_{0.53}Ga_{0.47}As$ cap. To form dummy gates, 50 nm SiO_2 was deposited by PECVD and patterned by e-beam lithography and ICP dry etching. Immediately prior to loading into the MOCVD chamber for S/D regrowth, the surface was oxidized by UV ozone exposure and then etched in dilute HCl. 60 nm Si-doped (4×10^{19} cm^{-3}) $In_{0.53}Ga_{0.47}As$ was selectively grown on the n+ cap layer. Device mesas were defined by wet-etching, and the dummy gates removed in buffered oxide etch (BOE). The exposed n+ cap and upper cladding layer were etched through multiple cycles of UV ozone exposure as oxidation and dilute HCl dip as surface oxide removal [8]-[10]. Immediately after removing the InGaAs surface oxide from the last cycle of UV ozone exposure in BOE, the sample was transferred into the ALD chamber, pre-cleaned/passivated by a cyclic N_2 plasma and TMA *in-situ* treatment, and subsequently ~3.6 nm HfO_2 gate dielectric deposited [11]. The sample was then annealed for 15 minutes at 400 °C in forming gas. 20 nm/100 nm Ni/Au was thermally deposited as the gate electrode. Subsequently, 20 nm/100 nm Ti/Pd/Au was lifted off for source/drain metallization. Fig. 1 shows a schematic cross-section of the device.

Results and Discussion: Fig. 2 shows a cross-sectional STEM for a 40 nm-L_g device. The HR-TEM inset of Fig. 2 confirms that ~0.5 nm interfacial layer is formed by N_2 plasma and TMA treatment and the channel of the device has 5 nm InAs, which is not relaxed, and 3 nm $In_{0.53}Ga_{0.47}As$. Fig. 3 shows a simulation of the energy band structure and the charge density at V_{GS} = 0.5 V by 1D Poisson-Schrödinger solver. The transfer characteristics of short channel devices are shown in Fig. 4. The devices with 40, 70, and 90 nm-L_g show 2.45, 2.40 and 2.16 mS/μm peak extrinsic g_m at V_{DS} = 0.5 V, respectively. All chips on the test sample (30 dies) show a similar performance (<10% variability). Fig. 5 shows the output characteristics of a 40 nm-L_g device. Its maximum drain current density is 1.95 mA/μm at V_{GS} = 1.4 V and V_{DS} = 0.5 V and its on-resistance is 214 Ω-μm. Fig. 6 shows the subthreshold characteristics of short channel devices. The subthreshold swings (SS) of devices with 40, 70, 90 nm-L_g are ~155, 115 and 110 mV/dec at V_{DS} = 0.05 V and ~400, 235, and 190 mV/dec at V_{DS} = 0.5 V, respectively. The gate leakage current is negligible, $<10^{-3}$ A/cm^2 at all gate biases measured, as shown in the inset of Fig. 6. The transfer and subthreshold characteristics of a long channel (L_g = 510 nm) device are shown in Fig. 7. The device shows 1.05 peak extrinsic g_m at V_{DS} = 0.5 V and the minimum SS of ~93 mV/dec at V_{DS} = 0.05 V. From transmission line method (TLM) measurements, shown in Fig. 9, 4.7 Ω-$μm^2$ S/D metal contact resistivity and ~25 Ω/square sheet resistance of the regrown S/D contact layer are extracted. Considering the gap between S/D metal contact and the channel, shown in inset of Fig. 9, S/D access resistance (R_{SD}) is determined to be ~82 Ω-μm, which degrades g_m by ~8% . Fig. 9 shows dependency of SS and threshold voltage, which was extracted from linear extrapolation, against gate length. The devices with short L_g, less than 100 nm, exhibit poor short channel effects, which may be attributed to back-barrier conduction due to heavy pulse doping. Fig. 10 shows R_{on} in terms of gate length. Despite a relatively large gap between the S/D metal and the channel (~1.2 μm for each side) due to non-self-aligned S/D metal contacts, the device shows very low R_{on} at all gate lengths. As a benchmark, Fig. 11 compares extrinsic peak g_m versus L_g with other published III-V MOSFETs and MOSHEMTs. This result is the best III-V MOSFET/MOSHET extrinsic g_m at all gate lengths at a given low supply voltage (V_{DS} = 0.5 V), almost equaling that of InAs HEMTs.

Conclusion: We have demonstrated InAs/$In_{0.53}Ga_{0.47}As$ channel MOSFETs using MOCVD regrown S/D and surface digital etching. The device with 40 nm-L_g shows excellent on-state performance of 2.45 mS/μm peak extrinsic g_m at V_{DS} = 0.5 V.

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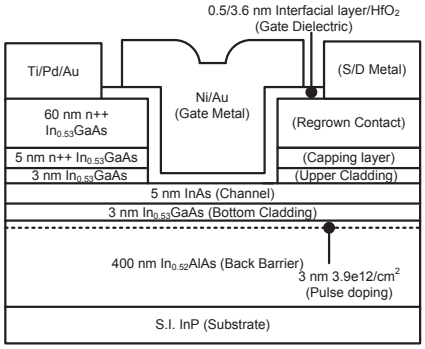

Fig. 1. Schematic cross-section of InAs/$In_{0.53}$GaAs MOSFET with MOCVD S/D regrowth and surface recess etching.

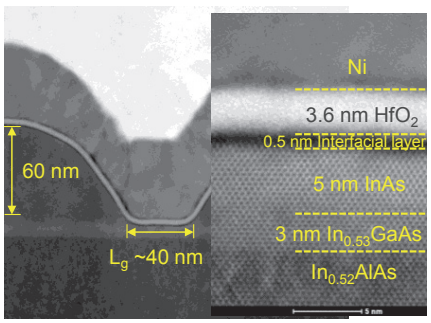

Fig. 2. Cross-sectional STEM of a 40 nm-L_g device. ~0.5 nm interfacial layer, ~3.6 nm HfO_2 and 5/3 nm InAs/$In_{0.53}$GaAs channel.

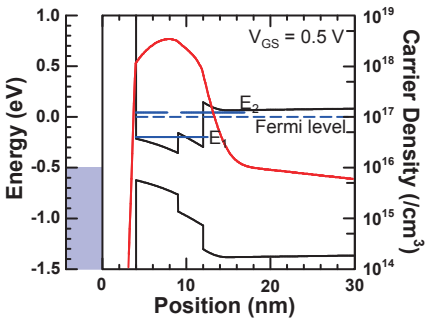

Fig. 3. Energy band structure and charge distribution at V_{GS} = 0.5 V by 1D Poisson -Schrödinger simulation.

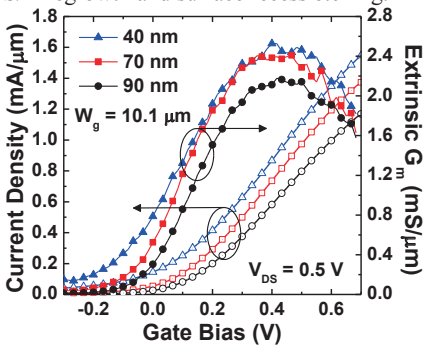

Fig. 4. Transfer characteristics of short channel devices (40/70/90 nm-L_g).

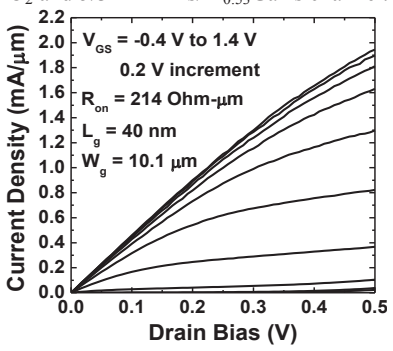

Fig. 5. Output characteristics of a 40 nm-L_g device.

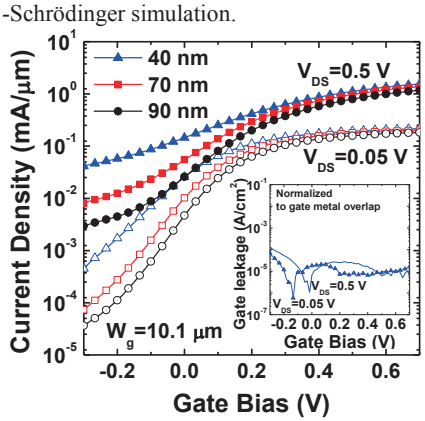

Fig. 6. Subthreshold characteristics of short channel devices (40/70/90 nm-L_g) and gate leakage current for the 40 nm-L_g device.

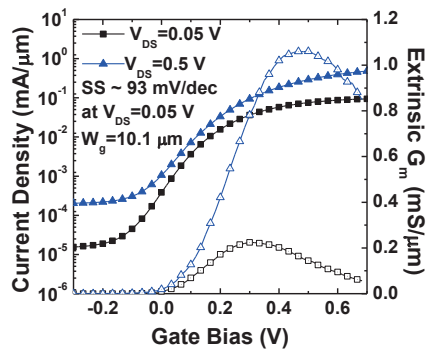

Fig. 7. Subthreshold characteristics of a 510 nm-L_g channel device. The minimum SS is ~93 mV/dec at V_{DS} = 0.05 V.

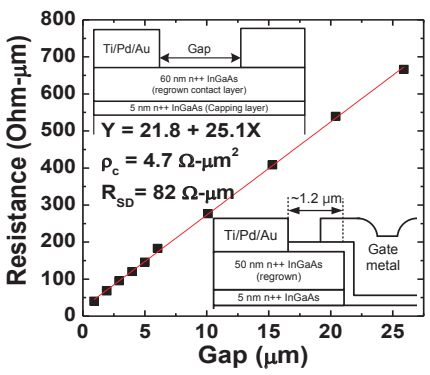

Fig. 8. TLM measurements of the regrown S/D contact layer.

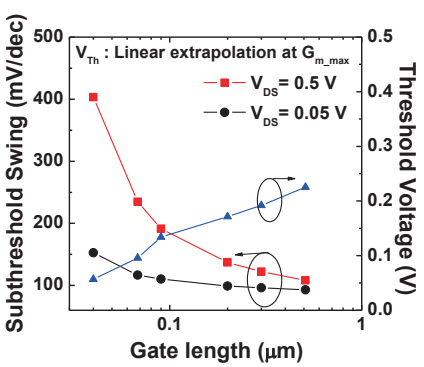

Fig. 9. Subthreshold Swing with respect to the gate length for V_{DS} = 0.05 V and 0.5 V.

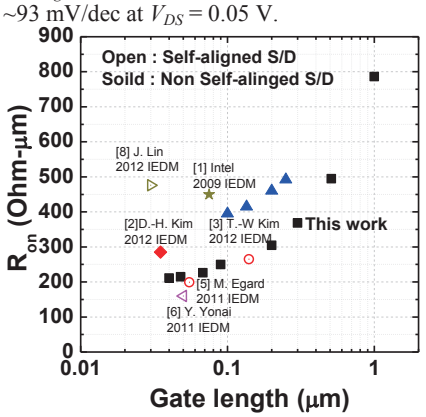

Fig. 10. On-resistance (R_{on}) with respect to the gate length. R_{on} is very low, particularly given the non-self-aligned S/D contacts.

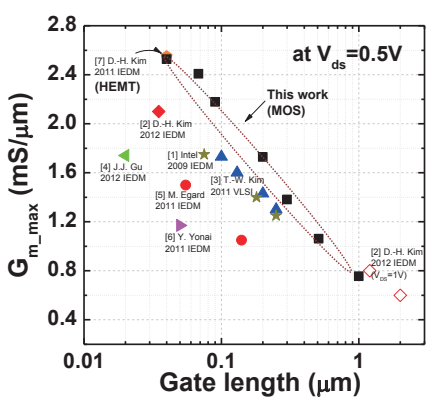

Fig. 11. Peak extrinsic g_m vs. gate length for III-V MOSFETs and MOSHEMTs. Data for a record HEMT is also shown.