Millimeter-Wave Series Power Combining Using Sub-Quarter-Wavelength Baluns

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***Abstract*—We present a new millimeter-wave power-combining technique using transmission-line baluns which both connect transistor outputs in series and inductively tune the transistor output capacitances. The baluns are much shorter than a quarter-wavelength $(\lambda/4)$, hence are more compact and have less insertion loss than a $\lambda/4$ balun. We introduce one topology providing an even number of series connections, including 2:1 and 4:1, and a second topology providing either an even or odd number of series connections. We then analyze segmented transformer power-combiners as a set of multi-conductor transmission-lines, and explore the relationship between transformer and transmission-line balun power-combiners. We demonstrate the technique with 2:1 and 4:1 series-connected designs implemented in a 0.25 μm InP HBT process. At 86 GHz, a single-stage power amplifier (PA) using the 2:1 baluns exhibits 30.4% peak PAE, 20.37 dBm output power $(P_{\rm out})$ and 23 GHz 3-dB bandwidth from a 448×816 $\mu\rm m^2$ die. A two-stage PA using the 2:1 baluns exhibits 30.2% PAE, and 23.14 dBm $P_{\rm out}$ from an 824×816 $\mu\rm m^2$ die. At 81 GHz, a two-stage PA with 4:1 series output power-combining exhibits 23.4% PAE, and 26.7 dBm (470 mW) $P_{\rm out}$ from a 1,080 $\times$ 980 $\mu\rm m^2$ die.**

***Index Terms*—Balun, mm-wave, power amplifier, power combiner, sub-quarter wavelength, transformer, transmission line.**

I. Introduction

THE mm-wave bands will enable future high speed wireless communication links and high resolution radars. Propagation losses are high [1], [2], particularly in foul weather, hence high power amplifiers (PAs) are needed for long transmission range [3]. High PA efficiency reduces power-supply and heat-sink costs, while high power per unit die area reduces IC costs and enables integration into monolithic arrays. Compact, efficient power-combining is necessary for high power-added efficiency (PAE) and small die area. Classical corporate transmission-line power-combiners occupy large die area [4]–[6], and the combining losses of these can be significant. Power can be combined using on-wafer transformers using a combination of turns ratio and a segmented primary loop [7]–[10] with multiple inputs to transform impedances. With the transformer combiners, the challenges are low inductor Q, significant parasitic series inductance and inter-winding capacitance, and port imbalances. Power can also be combined using direct transistor series-connection with local negative feedback [11]–[14]. Series connection enables low-loss power-combining in a small die; with this technique the challenges are maintaining a uniform voltage distribution and unity current gain, so that all transistors compress at the same RF drive level, as is necessary for high linearity and high efficiency. Power can be also combined on-wafer using baluns, either in LC form or using quarter-wave multi-conductor transmission-lines [15], [16]. Because such quarter-wavelength baluns are long, power-combiners using them occupy considerable die area. Further, the associated transmission-line losses can be high.

In [17] we introduced a new power-combining technique using sub-quarter-wavelength baluns for series-connected power-combining. 86 GHz PAs using the technique were demonstrated using a 0.25 μm InP heterojunction bipolar transistor (HBT) technology [18], [19]. A single-stage design using 2:1 series connection exhibited 30.4% peak PAE, 20.37 dBm output power $(P_{\rm out})$, while two-stage PA with 2:1 series connection exhibited 30.2% PAE and 23.14 dBm $P_{\rm out}$ from an 824×816 $\mu\rm m^2$ die. In [20] we reported an 81 GHz, two-stage PA with 4:1 series output power-combining exhibiting 23.4% PAE and 26.7 dBm (470 mW) $P_{\rm out}$ from a 1,080 $\times$ 980 $\mu\rm m^2$ die.

Here we will in greater detail describe the principles of series-connected power-combining using sub-quarter-wave baluns. We will extend the technique of [17] to designs providing an even number of series connections, considering specifically the 2:1 and 4:1 series-connected cases. Abandoning the balanced (balun) structure, we will also describe a three-port device using three-conductor transmission-lines and describe a second, related, power-combining topology which can provide either an even or odd number of series connections.

In transformer power-combiners using segmented primary windings [7]–[10], multiple transistors drive the transformer input, hence the voltage driving the primary winding is the sum of N transistor output voltages, i.e. the transistor outputs are connected in series. We therefore then analyze segmented transformer power-combiners as a set of multi-conductor transmission-lines, and explore the relationship between transformer and transmission-line balun power-combiners. In this analysis,

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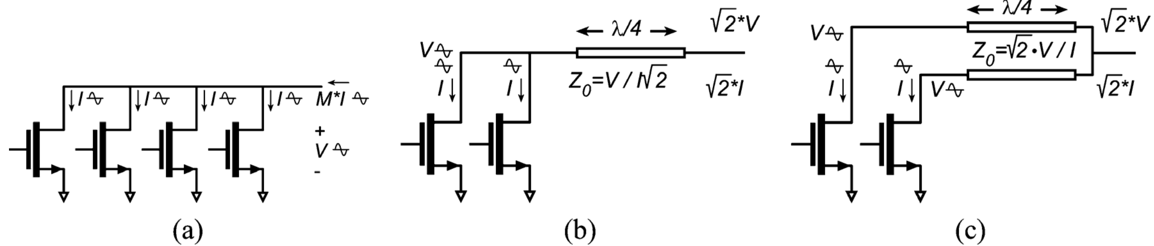

Fig. 1. Idealized parallel-connected power-combining (a) increases the output power but requires a low load impedance. This low impedance can be obtained with either a transmission-line transformer (b), or equivalently, a corporate transmission line power combiner (c).

the combination of transformer series winding inductances and inter-winding capacitances are identified as transmission-line elements, while port imbalances are seen to arise in part from transmission-line delays. With appropriate selection of the transmission-line impedances and of the input phase distribution, and in the absence of skin-effect losses, the transformer can provide the desired N:1 impedance transformation and zero insertion loss, i.e. the effects of the transformer LC parasitics on efficiency and on the impedance transformation ratio are eliminated. Designed in this manner, design of an N:1 segmented transformer corresponds closely to that of an N:1 series-connected power-combiner using sub-quarter-wave baluns.

II. Parallel and Series Power Combining

Millimeter-wave transistors have small carrier transit delays, hence mm-wave HBTs have thin collector depletion regions [21] and mm-wave FETs have short gates and small gate-drain spacings [22]. Breakdown voltages are therefore low. Given some maximum (breakdown) voltage $V_{\max}$ and minimum (saturation) voltage $V_{\min}$, and with some maximum current $I_{\max}$ (proportional to the HBT emitter area or FET gate width), highest output power and highest collector/drain efficiency in a class-A power amplifier are obtained if the transistor is loaded by an LR parallel network where $R_{L,\mathrm{opt}}=(V_{\max}-V_{\min})/I_{\max}$ and where $j\omega L=-1/j\omega C_{\mathrm{out}}$, where C_{out} is the transistor output capacitance.

Increasing $I_{\max}$ by connecting M transistors in parallel (or by increasing the HBT emitter junction area or FET gate width up to the limits of acceptable parasitics within the transistor) increases the output power (Fig. 1)

$$P_{\mathrm{out}}=\frac{1}{8}M\cdot(V_{\max}-V_{\min})\cdot I_{\max}. \tag{1}$$

Unfortunately, as we increase the output power, the optimum load resistance $R_{L,\mathrm{opt}}$ decreases

$$R_{L,\mathrm{opt}}=(V_{\max}-V_{\min})/MI_{\max}. \tag{2}$$

With low $R_{L,\mathrm{opt}}$, large impedance transformation ratios are required, using combinations of transmission-line impedance-transformers, and Wilkinson or corporate transmission-line power-combiners. As the parallel (Fig. 1) power-combining ratio M becomes large, skin-effect insertion loss and die area both increase, while the power-combiner bandwidth decreases. In combination, the large die area and the degraded efficiency limit the feasible mm-wave output power per die.

Power can also be combined [11]–[14] by using a combination of direct N:1 series and M:1 parallel connections (Fig. 2(a)). The output voltage is increased N:1, the output current increased M:1, and the output power increased NM:1. Critically, the optimum load resistance is now $R_{L,\mathrm{opt}}=(V_{\max}-V_{\min})\cdot N/MI_{\max}$. With similar numbers of parallel and series connections, the load impedance can be maintained close to the characteristic impedance of on-wafer transmission-lines, i.e. $\sim 50\,\Omega$. Minimal impedance-tuning, with its associated loss and die area, is therefore required, and series-connected PAs can be compact. Gate drive voltages in the series-connected stack are derived by local voltage negative feedback (Fig. 2(b)) with $(1:2),(2:3),\ldots,(N-1:N)$ voltage-division ratios, forcing $(2:1),(3:2),\ldots,(N:N-1)$ local voltage gains hence a uniform voltage distribution within the stack. Inductors tune the combined shunt capacitive loading of the voltage-dividers and transistor junction capacitances, so that the current gain of each stage is unity. With direct series connection, the design challenges are maintaining the desired $(2:1),\ldots,(N:N-1)$ local voltage gains and desired unity local current gains, so that all transistors compress at the same RF drive level, as is necessary for high linearity and high efficiency. In contrast, if baluns are used for series-connections, each transistor driver within the amplifier has an identical design. Absent significant port imbalances within the combiner, all transistors will compress at the same RF drive level.

III. Three-Conductor Transmission-Lines and Baluns

We connect transistors in series using sub-quarter-wavelength baluns. Before considering the baluns, we will first consider the properties of the three-conductor transmission-lines from which the baluns are constructed.

Fig. 3 shows a three-conductor coaxial transmission-line. Intermediate conductor m_2 fully surrounds inner conductor m_3 and shields it from outer conductor m_1. With dielectric constants ϵ_r and conductor radii r_1, r_2, and r_3, the line supports two independent transmission-line modes. The first corresponds to a voltage between m_2 and ground, with characteristic impedance $Z_{0,1-2}=(\eta_0/2\pi\epsilon_r{}^{1/2})\ln(r_1/r_2)$, while the second corresponds to voltage between m_3 and m_2, with characteristic impedance $Z_{0,2-3}=(\eta_0/2\pi\epsilon_r{}^{1/2})\ln(r_2/r_3)$. Note that these two voltage modes are excited in series.

For ICs, a three-conductor transmission-line can be realized in planar form (Fig. 4). The planar and coaxial structures differ significantly in that there is imperfect shielding between m_1 and m_3. Although an imperfect description of most integrated cir-

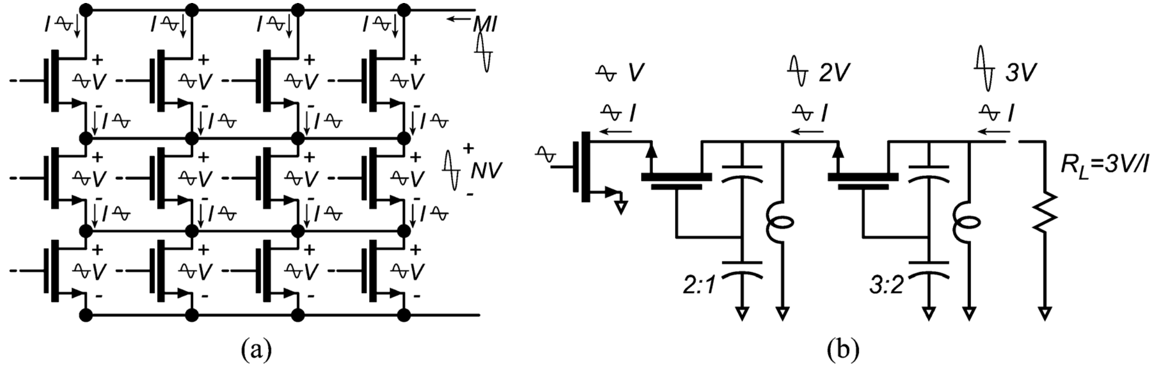

Fig. 2. Power amplifier (a) with combined N:1 series and M:1 parallel connections providing NM:1 increased output power and a load impedance transformed by the ratio N/M:1. Gate drive voltages within the series-connected stack are derived (b) from local capacitive voltage feedback networks with associated inductive tuning. The figure neglects DC bias.

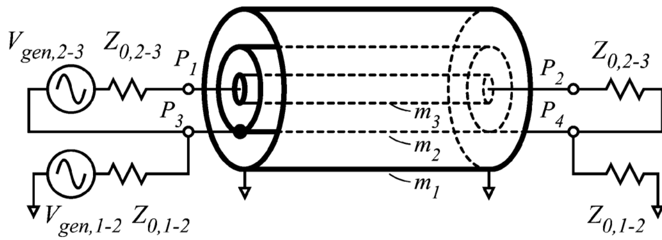

Fig. 3. Three-conductor coaxial cable supporting independent transmission-line modes between m_3-m_2 and m_2-*ground*.

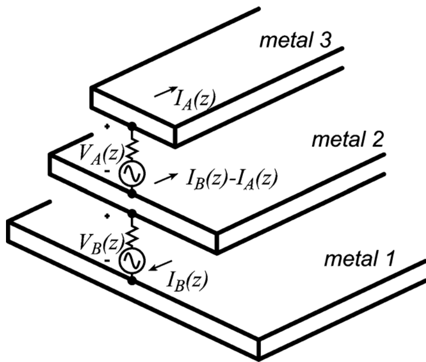

Fig. 4. Definition of voltages and currents on the three-conductor transmission-line.

cuits, we will simplify analysis by assuming that all conductors are surrounded by a uniform dielectric of permittivity $\epsilon_r\epsilon_0$. For transmission-lines of constant cross-section in the direction of propagation, this then results in TEM propagation.

Voltage differences $V_A(z)$ and $V_B(z)$ then propagate according to

$$\begin{aligned} V_A(z) &= V_3(z) - V_2(z) = {V_A}^+ e^{-j\beta z} + {V_A}^- e^{+j\beta z} \\ V_B(z) &= V_2(z) - V_1(z) = {V_B}^+ e^{-j\beta z} + {V_B}^- e^{+j\beta z} \\ I_A(z) &= {I_A}^+ e^{-j\beta z} - {I_A}^- e^{+j\beta z} \\ I_B(z) &= {I_B}^+ e^{-j\beta z} - {I_B}^- e^{+j\beta z} \end{aligned} \tag{3}$$

where the wave currents are related to the wave voltages through a characteristic admittance matrix,

$$\begin{bmatrix} {I_A}^{+/-} \\ {I_B}^{+/-} \end{bmatrix} = \begin{bmatrix} Y_{0,AA} & Y_{0,AB} \\ Y_{0,BA} & Y_{0,BB} \end{bmatrix} \begin{bmatrix} {V_A}^{+/-} \\ {V_B}^{+/-} \end{bmatrix}. \tag{4}$$

As noted by Pozar [23], given TEM propagation, the electrical characteristics of coupled lines can be completely determined from the effective capacitances between the lines and the velocity of propagation. This implies that with zero capacitive coupling between m_1 and m_3, there is zero coupling between the m_1-m_2 and m_2-m_3 transmission-lines. To simplify analysis, we assume that the m_3 conductor is well-shielded from the m_1 conductor by m_2, hence the coupling terms both vanish, i.e. $Y_{0,AB} = Y_{0,BA} = 0$. In this case $1/Y_{0,AA} = Z_{0,2-3}$ and $1/Y_{0,BB} = Z_{0,1-2}$ become the characteristic impedances of the two propagating transmission-line modes, one between m_2 and m_3 and the second between m_1 and m_2. Given the uniform dielectric, all mode propagation constants β and phase velocities $v_p = \omega/\beta = c/{\epsilon_r}^{1/2}$ are equal. Again, the two voltage modes are excited in series.

Fig. 5 shows potential three-conductor transmission-lines for IC applications. To ensure that m_3 is well-shielded from m_1, the three-conductor transmission-line of Fig. 5(a) uses upper and lower microstrip lines with m_2 much wider than m_3. If the vertical separation between the m_1 and m_2 wiring planes is small, this then results in a low characteristic impedance $Z_{0,1-2}$ and high skin-effect losses for the associated propagating mode. $Z_{0,1-2}$ can be increased (Fig. 5(b)) by providing an opening in the m_1 ground plane beneath the transmission-line, although because of the current-crowding at the conductor edges, losses in the resulting elevated coplanar waveguide line mode between m_1 and m_2 remain relatively high. Adding m_3 sidewalls, connected to the m_2 transmission-line by closely-spaced periodic vias (Fig. 5(c) and (d)), improves shielding between m_3 and m_1. In the sub-quarter-wavelength balun power-combiner, losses are dominated by the skin effect. The structure of Fig. 5(d) provides moderate $Z_{0,1-2}$ and low loss at mm-wave frequencies if the vertical separation between the m_1 and m_2 wiring planes is at least 3–4 μm; otherwise the structures of Fig. 5(c) is preferable. Fig. 6 shows simulations of the three-conductor transmission-lines of Fig. 5(b) (upper microstrip line with lower elevated coplanar waveguide) and Fig. 5(c) (upper microstrip line with side shields and lower elevated coplanar waveguide). Each structure has length of $\lambda/8$ at 80 GHz, and ports are defined, as in Fig. 4. The sidewalls increase the isolation between the m_1-m_2 and m_2-m_3 transmission-line mode from 23.1 dB to 33.9 dB.

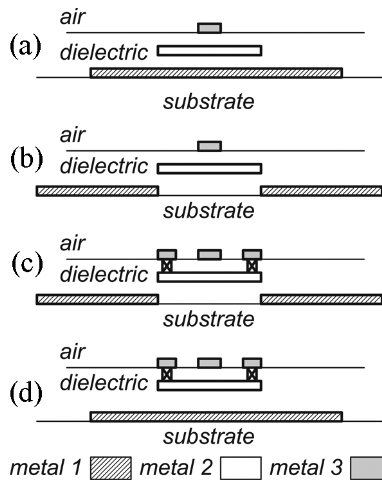

Fig. 5. Cross-sections of tri-conductor transmission-lines with (a) upper and lower microstrip lines, (b) upper microstrip line and lower elevated coplanar-waveguide, (c) upper microstrip line with side shields (sidewalls) and lower elevated coplanar-waveguide, and (d) upper microstrip line with side shields and lower microstrip line.

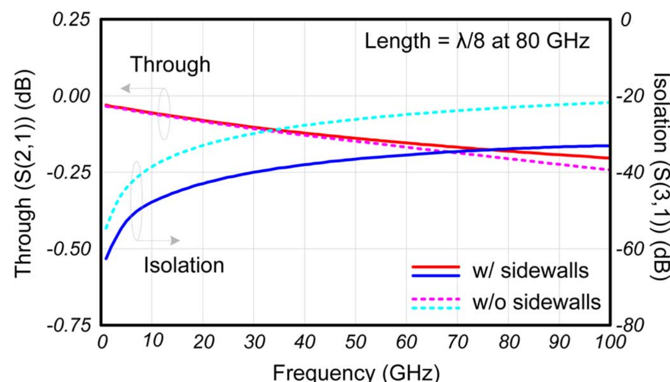

Fig. 6. Simulation of the three-conductor transmission lines of length $\lambda/8$, with and without sidewalls, i.e. in the geometries of Fig. 5(b) and (c), and with port connections as in Fig. 4. Cross-sectional dimensions are as in Fig. 11. At 80 GHz, the sidewalls increase the transmission-line mode isolation from 23.1 dB to 33.9 dB.

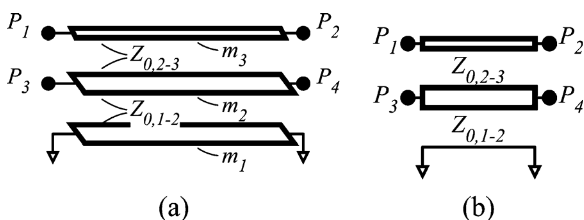

Fig. 7. (a) Three-conductor transmission-line and (b) its circuit schematic symbol.

The three-conductor transmission-lines, whether coaxial (Fig. 3) or planar (Figs. 4 and 5), are represented in circuit schematics by the symbol shown in Fig. 7.

IV. Sub-Quarter-Wavelength Baluns for Series Combining

Baluns constructed from the three-conductor transmission-lines of Figs. 4 and 5 can be used for series-connected power-combining. These power-combiners are similar to wide-band Marchand baluns, but unlike the Marchand design which uses $\lambda_g/4$ lines [24], the power-combiners reported here use line sections much shorter than $\lambda_g/4$, a quarter of a guide wavelength. In these sub-quarter-wave designs, power-combining losses are greatly reduced simply because of greatly reduced transmission-line length. The required die area is similarly reduced. The sub-quarter-wave design introduces shunt inductive loading at the ports connecting to the transistors, loading which is tolerated by absorbing it into the amplifier output tuning network, thereby tuning the transistor output capacitance. To maintain phase balance, an identical balun is used on the PA input. Note that balun port-port imbalances will result in different amplifier cell drive levels, and should therefore be kept small.

First consider [17] a 2:1 series power-combiner, Fig. 8(a), using tri-plate transmission-lines. The structures of Fig. 5 are employed; the m_2 conductor is much wider than the m_3 conductor, shielding m_3 from m_1 to assure P_2 to P_3 balance. There are microstrip lines of impedance $Z_{0,1-2}$ between m_1 and m_2 and of impedance $Z_{0,2-3}$ between m_2 and m_3.

The 2:1 power-combiner, Fig. 8(a), is understood using the equivalent circuit of Fig. 8(b). Signal sources V_1 and V_2, voltage generators of some nonzero output impedance, are connected in series between conductors m_2 and m_3, a 50 Ω transmission-line connected to the 50 Ω load. V_1 and V_2 each see a 25 Ω load. V_1 and V_2 are also loaded in parallel by the shunt-stub impedance $Z_{\text{stub}} = jZ_{0,1-2}\tan\theta_2$ from the short-circuited transmission-line stubs between m_1 and m_2.

If the sources (V_1 and V_2) driving the balun are each M parallel-connected transistors of maximum voltage swing $(V_{\max} - V_{\min})$, and maximum current drive $MI_{\max}$, then each parallel transistor combination should be loaded by an LR parallel network with load resistance $R_{L,\text{opt}} = (V_{\max} - V_{\min})/MI_{\max}$ and load inductance $j\omega L = -1/j\omega MC_{\text{out}}$, where C_{out} is output capacitance of an individual transistor. The number M of parallel transistors, hence $I_{\max}$, are adjusted until $R_{L,\text{opt}} = 25$ Ω, and the balun length θ_2 is adjusted to set $Z_{\text{stub}} = -1/j\omega MC_{\text{out}}$. Each HBT power cell has 2:1 larger junction area, and 2:1 larger $I_{\max}$, than a device sized to directly drive 50 Ω with appropriate shunt inductive tuning. The output power is therefore increased 4:1.

The 4:1 series-connected design, Fig. 8(c), has the equivalent circuit of Fig. 8(d). The four sources V_1-V_4 are connected in series across the 50 Ω amplifier load. Each source sees a 12.5 Ω load, again loaded in parallel with Z_{stub}. Design therefore consists of adjusting the number of parallel HBTs, and hence $I_{\max}$, until $R_{L,\text{opt}} = 12.5$ Ω, and then adjusting the balun length θ_2 until $Z_{\text{stub}} = -1/j\omega MC_{\text{out}}$. The HBT power cells now have 4:1 larger junction area, and 4:1 larger $I_{\max}$, than a device sized to directly drive 50 Ω, hence the total output power is increased 16:1. The line connecting V_2 and V_3 must have 25 Ω impedance, and the phases of (V_1, V_2) must differ those of (V_3, V_4) by the delay of the line connecting V_2 and V_3, the latter requirement satisfied by using an identical input power-splitter.

A full 2:1 series-connected amplifier (Fig. 9(a)) consists of an output power-combining network constructed from

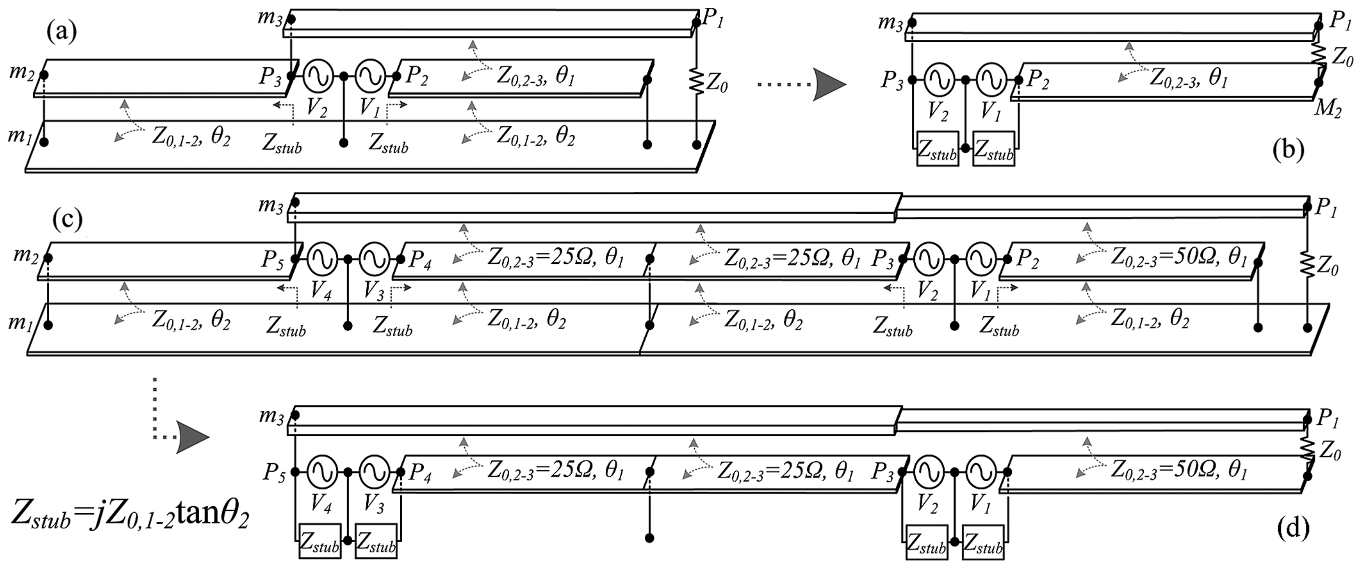

Fig. 8. Sub-quarter-wavelength balun concepts: (a) 2:1 balun structure, (b) 2:1 balun reduced circuit model, (c) 4:1 balun structure, and (d) 4:1 balun reduced circuit model. Note that in this, and subsequent figures, the transistor outputs are represented as AC generators (V_1-V_4); the nonzero output impedance of these generators is taken to be implicit.

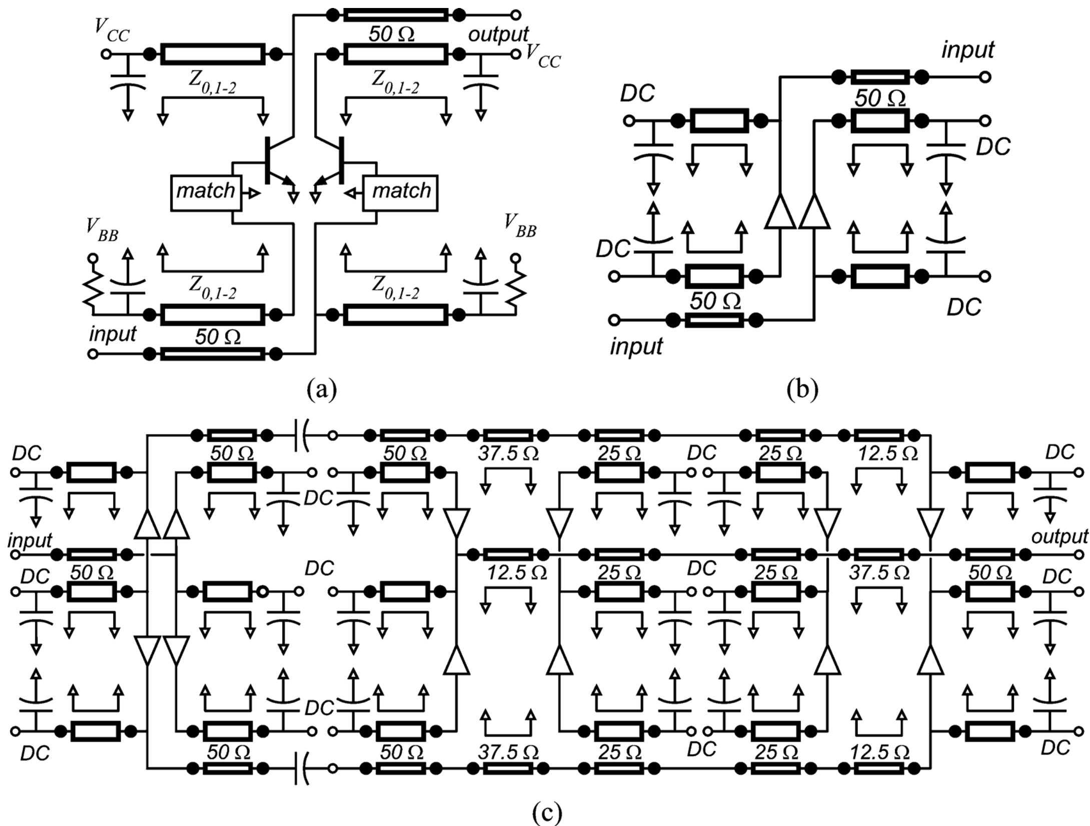

Fig. 9. Detailed circuit diagram (a) of the 2:1 series-connected design showing bias connections, input-matching, and output shunt inductive tuning using the sub-quarter-wave balun, and (b) its block-level representation. Block level (c) representation of a 4:1 series-connected design with pre-driver stage. Each of the eight output cells drives 25 Ω.

sub-quarter-wave baluns, a similar input power-dividing network, an array of transistor power cells, each containing many parallel transistor fingers, and each with an input impedance-matching network. Transistor DC bias is provided through the baluns, with the m_2 conductors AC-grounded by capacitors at the balun terminal ports. Fig. 9(b) shows a block-level representation of the 2:1 series-connected amplifier, where the power transistors and their input matching networks and bias networks are compactly represented by amplifier symbols. Details of the 2:1 design and experimental results will be described subsequently.

Fig. 9(c) shows a similar block-level representation of a 4:1 series-connected design [20]. The input driver stage uses 2:1 series splitter and combiners, and has two separate RF outputs

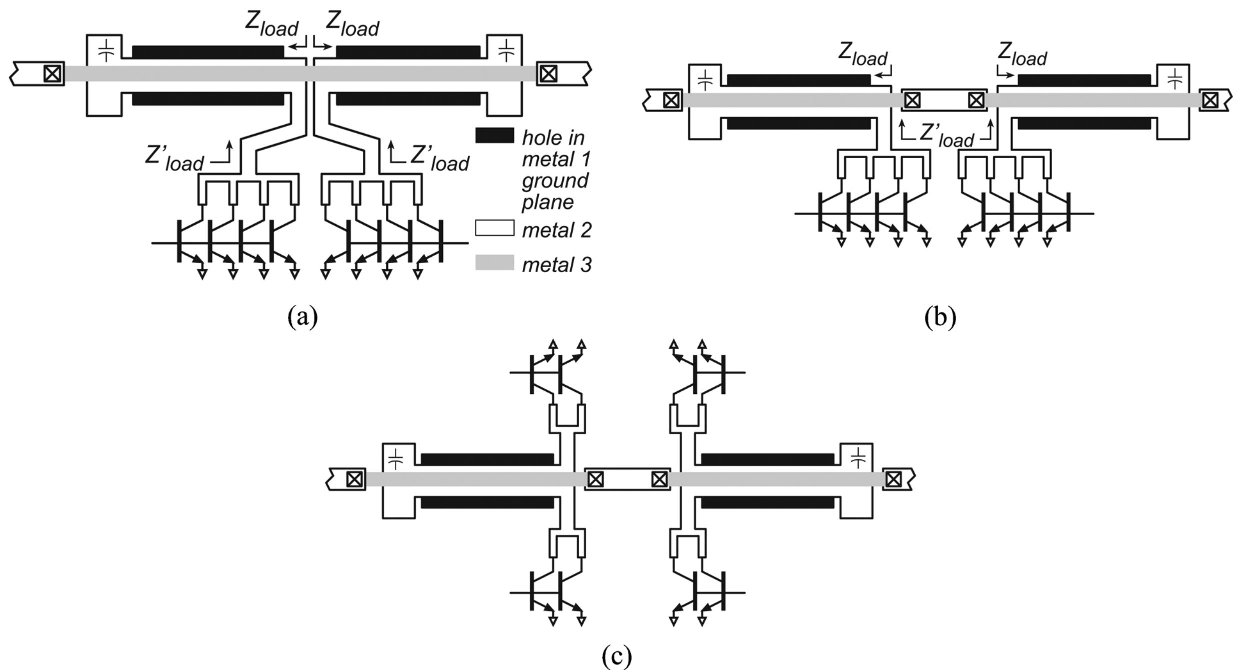

Fig. 10. Details of balun feed design. With a large series-connection ratio, the transistors occupy a large die area, and long interconnect leads are required (a). Feed inductances are reduced by separating (b) the two halves of the balun with a transmission-line section, and are further reduced (c) by driving the balun from both sides.

driving the two inputs of the main PA stage. In the main power amplifier stage, each RF input is split by a 4:1 series-connected balun network, dividing the total input power among eight HBT cells. The HBTs cells are then connected into four pairs, four above and four below the output power-combiner of Fig. 9(c), with each pair driving one port of the output combiner. Each port of the 4:1 output balun presents a 12.5 Ω load shunted by the balun m_1-m_2 inductive stub. Because each balun port is driven by two parallel transistor gain cells, each transistor gain cell sees a 25 Ω load shunted by twice the stub inductance. Regarding sensitivity to the transistor cell nonuniformity, variations in the individual amplifier gain of ±0.8 dB relative to the main gain cause less than ±0.51 dB variations in the overall amplifier S_{21}. Similarly, variations in the individual amplifier phase of ±15 degrees cause less than ±0.3 dB variations in the overall amplifier S_{21}. Detail of the 4:1 design, and experimental results, will again be presented in the next section.

In the 4:1 series-connected designs of Fig. 9(c), short two-conductor transmission-lines (37.5 Ω and 12.5 Ω) are inserted between the left and right three-conductor structures within the baluns. Further, the 12.5 Ω ports of the balun are driven in parallel by pairs of transistor power cells. Both these design details are driven by the need to minimize transmission-line length, and the associated series inductance, between the transistor power cells and the balun port (Fig. 10). Particularly with the 4:1 series-connected design, the balun port impedances are low, and many parallel transistors are required to provide the correct $R_{L,\mathrm{opt}}$ to correctly interface to the balun port. The transistors consequently occupy significant die area, and the interconnect leads between the transistors and the balun ports may be long (Fig. 10(a)). The associated transmission-line series inductance increases the impedance (Z'_{load} vs. Z_{load}) presented to the transistors, decreasing the feasible output power. Lead lengths between the transistors and the balun port can be reduced by separating (Fig. 10(b)) the two halves of the balun with a matched-impedance two-conductor transmission-line section, and are further reduced (Fig. 10(c)) by driving the balun from both sides. Both these design features are indicated in the schematic of Fig. 9(c).

V. 2:1 and 4:1 Series Combiners: Design and Results

High-efficiency W-band 2:1 and 4:1 series power-combined PAs were designed into a 0.25 μm InP HBT process; in this process, HBTs with a 6 μm × 0.25 μm emitter finger exhibit $\mathrm{BV_{CEO}} = 4.5$ V, $f_{\max} = 859$ GHz, and $f_\tau = 392$ GHz at a bias condition of $V_{\mathrm{CE}} = 1.8$ V and $J_E = 6$ mA/μm^2 emitter current density [19]. There are three Au interconnect planes, m_1, m_2, and m_3 (top) of 1 μm, 1 μm, and 3 μm thicknesses. A 5 μm thick dielectric ($\epsilon_r = 2.7$) separates m_3 and m_2, while 1 μm of dielectric separates m_2 and m_1. The process provides 0.3 fF/μm^2 MIM capacitors and 50 Ω/square thin-film-resistors (TFR).

The PAs use tri-plate baluns with a transmission-line cross-section in the form shown in Fig. 5(c). Transistor DC bias networks are integrated into the balun itself by providing m_1-m_2 short-circuits through capacitors at the balun ports. Details of the balun layout are shown in Fig. 11.

The schematic is as shown previously in Fig. 9(a). Design starts with a previously-reported [25] HBT power transistor unit cell having four 6 μm × 0.25 μm emitter fingers, with the emitter, base, and collector leads connected by short lumped leads. The power transistor unit cell has $f_{\max} = 525$ GHz and $f_\tau = 285$ GHz at the PA bias condition of $V_{\mathrm{CE}} = 2.5$ V and $J_E = 4.2$ mA/μm^2. A power cell with $R_{L,\mathrm{opt}} = 25$ Ω is

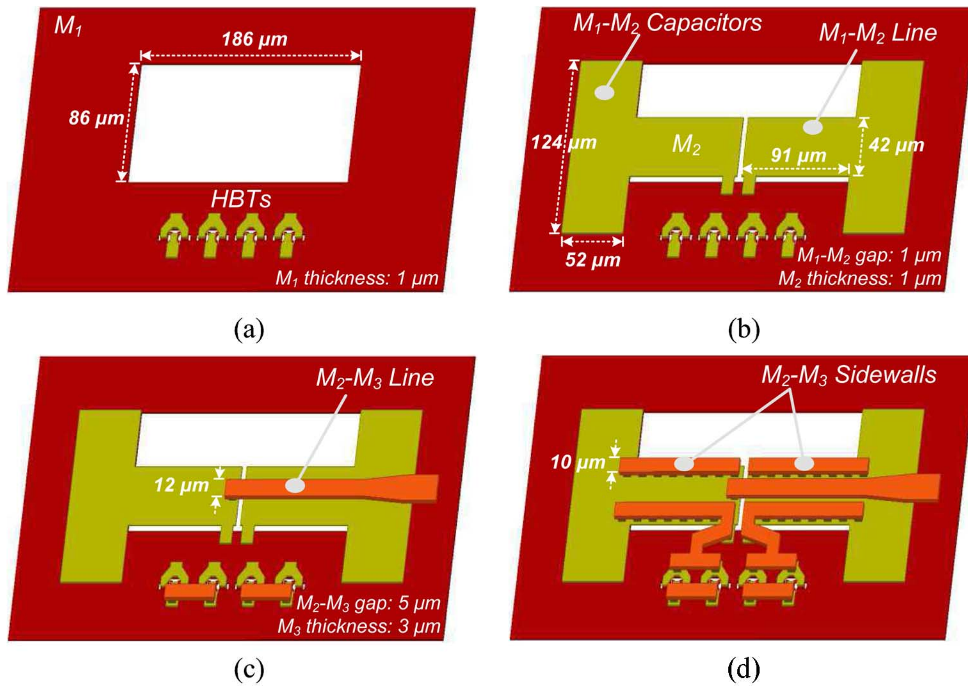

Fig. 11. Details of the 2:1 balun physical layout showing (a) metal 1, (b) metal 2 including DC bias capacitors, (c) the transmission-line in metal 3, and (d) the final structure with sidewalls.

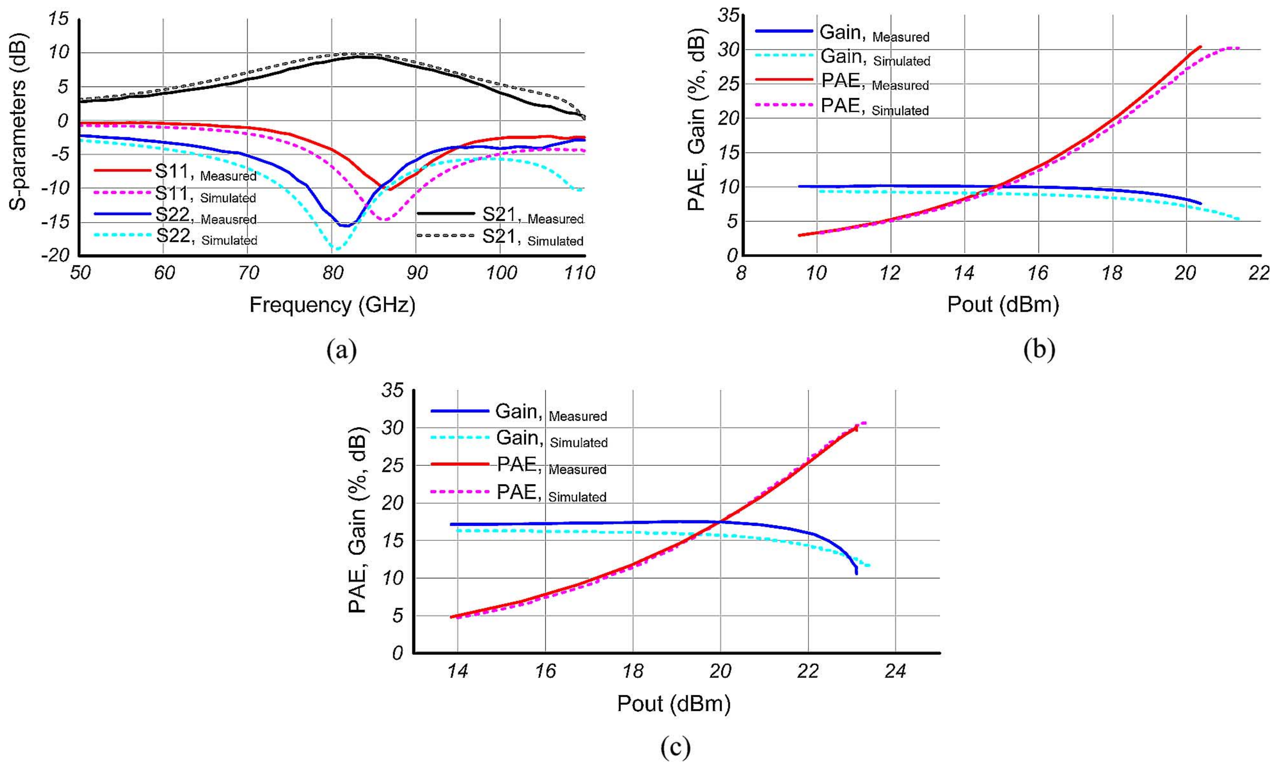

Fig. 12. Measured and simulated 2:1 PA results: (a) S-parameter results for the single-stage PA, (b) PAE and gain vs. output power for the single-stage PA and (c) PAE and gain vs. output power for the two-stage PA.

formed by connecting in parallel with controlled-impedance lines and two such four-finger power cells. Note that with 2:1 series connection the impedance presented at the port of the combiner is 25 Ω.

Transistor inputs are matched by two-section LC networks, and an emitter-buffered active bias circuit increases the DC collector current as output power increases [26], this enhancing thermal stability. Bias is slightly below class-A.

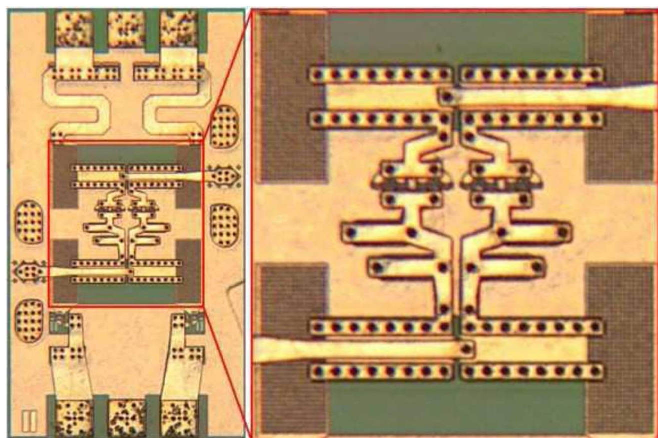

Fig. 13. Die photograph of an 86 GHz power amplifier IC with 2:1 series power-combining. On the right is an image of the core of the circuit.

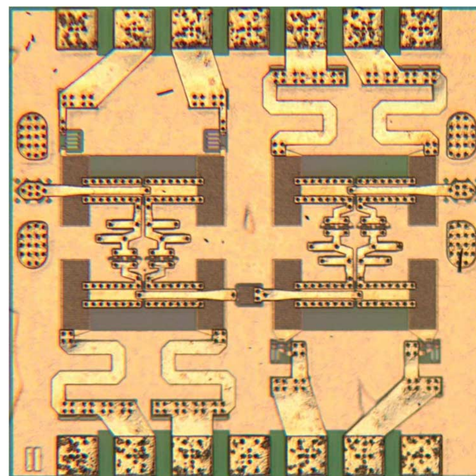

Fig. 14. Die photograph of a two-stage power amplifier using 2:1 series power-combining.

Fig. 12 shows measured 2:1 PA IC performance. The zero-signal bias conditions are $V_{\mathrm{CC}} = 2.5$ V, $I_C = 50$ mA, and $I_B = 2$ mA; the collector bias current increases under RF drive. Small-signal S-parameter measurements (Fig. 12(a)), show a 9.4 dB maximum S_{21} at 83 GHz with 23 GHz 3 dB bandwidth.

Fig. 12(b) shows the gain and PAE of the single-stage amplifier as a function of output power at an 86 GHz signal frequency. The single-stage PA exhibits 30.4% peak PAE at 20.4 dBm (108.8 mW) output power. Fig. 13 shows a die photograph of the single-stage design. The total chip area is 448×816 $\mu\mathrm{m}^2$, while the IC core area (excluding DC feed lines and RF pads) is 290×310 $\mu\mathrm{m}^2$. The power density, i.e. the output power per unit total die area is 294 mW/mm^2, while the output power per unit IC core die area is 1,210 mW/mm^2.

A two-stage PA IC (Fig. 14) with each stage having 2:1 series combining was also designed and fabricated. Zero-signal DC bias points for the first stage are $V_{\mathrm{CC}} = 3$ V and $I_C = 30$ mA, and for the second stage are $V_{\mathrm{CC}} = 3$ V and $I_C = 50$ mA. Under RF signal drive, the instantaneous operating voltage can exceed the common-emitter breakdown voltage $\mathrm{BV_{CEO}}$, and hence the second stage could support a 3.0 V DC bias. Fig. 12(c) shows the gain and PAE of the two-stage amplifier as a function of output power, again at an 86 GHz signal frequency. The PA shows 30.2% peak PAE at 23.14 dBm (206 mW) output power. The total die area is 824×816 $\mu\mathrm{m}^2$, while the core area is 660×310 $\mu\mathrm{m}^2$. The output power per unit total die area is 307 mW/mm^2, while the output power per unit IC core die area is 1,006 mW/mm^2.

In on-wafer measurements, a separate test structure of the 2:1 series combiner shows 0.52 dB insertion loss at 86 GHz, and less than 0.68 dB insertion loss between 60 GHz and 105 GHz. Note again that the 2:1 series connection, at fixed transistor maximum voltage swing, provides 4:1 power-combining. Note also that this attenuation includes the losses associated with inductive tuning of the transistor capacitive output impedance. Further, electromagnetic simulations of this combiner show less than 0.15 dB amplitude imbalance and less than 2.7 degree phase imbalance throughout W-band (75 to 110 GHz). The common mode rejection ratio of the balun, in electromagnetic simulation, is better than 32 dB over 75 to 110 GHz.

Fig. 15 shows the measured performance for the PA IC (Fig. 16) using the 4:1 series-combiner. The zero-signal bias currents are 60 mA and 400 mA for the 1st and 2nd stages. The PA exhibits (Fig. 15(a)) 17.5 dB gain S_{21} at 81 GHz, >11.5 GHz 3-dB bandwidth, and input and output return losses (S_{11}, S_{22}) better than -10 dB over a 10 GHz bandwidth. In 81 GHz large signal measurements at $V_{\mathrm{CC}} = 2.75$ V (Fig. 15(b)), the PA IC exhibits 26.7 dBm (470 mW) maximum output power, 23.4% peak PAE, and 443 mW/mm^2 output power per unit die area. Excluding the DC feed lines and the IC pad area associated with RF pads, the output power per unit die area is 1,020 mW/mm^2.

Measurements of separate test structures of the 4:1 series combiner show 0.92 dB insertion loss at 81 GHz, and less than 1.32 dB insertion loss between 75 GHz and 103 GHz. Note again that the 4:1 series connection, at a fixed transistor maximum voltage swing, provides 16:1 power-combining, and that the losses associated with the series combiner include losses associated with inductive tuning of the transistor output capacitance.

Tables I and II summarize the comparisons of the recent millimeter-wave power combiners and power amplifier results.

VI. Series-Combining With an Odd Number of Stages

The power amplifier designs of Fig. 9 rely on the symmetric balun structure of Fig. 8; these designs demand series-combining with an even number of stages. Power-combining with an arbitrary number of stages, even or odd, can be obtained by abandoning the symmetric balun (Fig. 8) and instead using its constituent three-conductor elements as voltage-summation devices.

Fig. 17 shows the basic voltage-summation three-port. The device is formed (Fig. 17(a)) from a three-conductor line, generally much shorter than a quarter of a guide wavelength, with one port short-circuited. A transistor with output capacitance C_{out} (Fig. 17(b)) will be connected to P_3 (but not P_2) of the voltage summation three-port. The short-circuited stub between m_1 and m_2 can be represented by its inductance L_{stub} (Fig. 17(c)). At

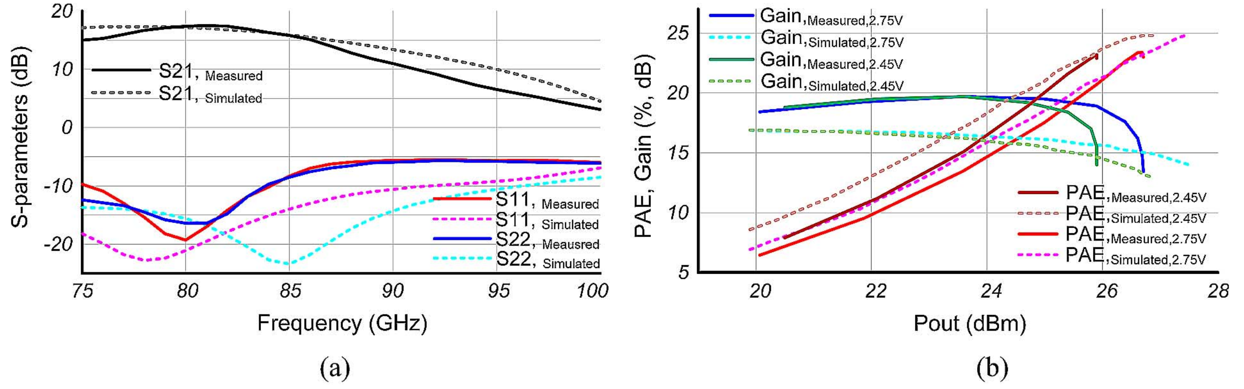

Fig. 15. Measured and simulated results for the power amplifier with 4:1 series power combining: (a) S-parameter results for the two-stage power amplifier, and (b) PAE and gain vs. output power for the two-stage power amplifier.

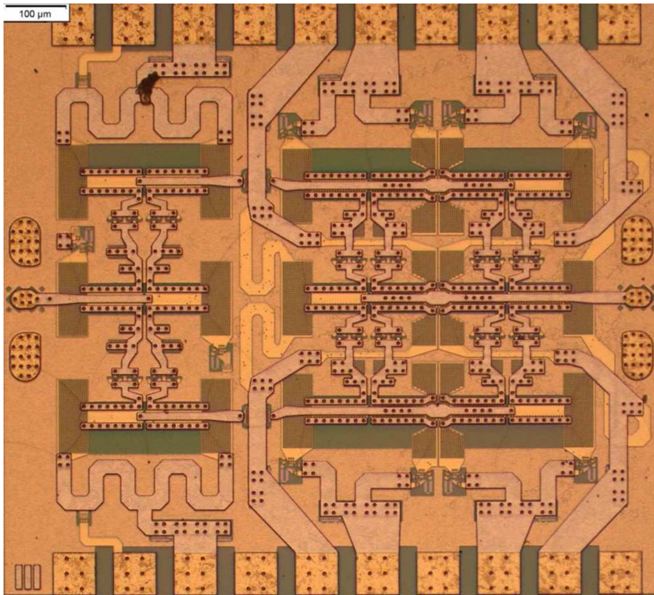

Fig. 16. Die photograph of the two-stage power amplifier using 4:1 series power-combining.

TABLE I
SUMMARY OF RECENT MM-WAVE POWER COMBINERS

Ref.	Tech.	Type	N-way	Freq. (GHz)	IL (dB)	Size (mm^2)
This work [17]	0.25 µm InP HBT	Sub-λ/4 TL	2:1	86 (60-105)	0.52 (0.68)	0.03
This work [27]	0.25 µm InP HBT	Sub-λ/4 TL (ring)	2:1	86 (60-110)	0.50 (0.63)	0.04
This work [20]	0.25 µm InP HBT	Sub-λ/4 TL	4:1	87 (75-103)	0.91 (1.32)	0.06
[10]	0.13 µm BiCMOS	TF	4:1	60 77/79	0.73* 1.20*	0.015
[28]	0.18 µm BiCMOS	TF	8:1	83.5 (70.5-85)	1.25 (0.80*)	0.02#
[29]	65 nm CMOS	TF	4:1	60	0.63*	0.02#
[30]	90 nm CMOS	Wilkinson	2:1	60	0.54	0.08
[31]	40 nm CMOS	Series/ parallel TF	4:1	75 (65-90)	0.92* (1.0)	0.05#
[32]	90 nm CMOS	TL	4:1	60 (55-65)	1.09* (1.25*)	-
[33]	0.18 µm CMOS	Marchand	2:1	57	3.40	0.55
[34]	InGaP /GaAs	Marchand	2:1	(15-45)	(1.50)	0.40

*Simulation results, #Area estimated by chip image. IL: insertion loss, TF: transformer, and TL: transmission-line. Parentheses in the frequency and insertion loss columns indicate worst-case insertion loss over the indicated bandwidth.

the amplifier center frequency, $C_{\rm out}$ and $L_{\rm stub}$ are in resonance and the port signal generators V_2 and V_3, voltage generators of some nonzero output impedance, drive the transmission-line element in series.

Using the voltage-summation three-ports of Fig. 17(a), a power amplifier with 3:1 series-connections can be formed (Fig. 18(a)). In the equivalent-circuit representation (Fig. 18(b)), each transistor power cell $(V_1\text{-}V_3)$ is connected in series across the 50 Ω load; the load impedance for each power cell is 16.7 Ω shunted by the LC parallel network formed from the stub inductance $L_{\rm stub}$ and the transistor output capacitance $C_{\rm out}$.

Fig. 19 compares the performance of the 3:1 series-connected designs of Fig. 18 with the 4:1 series-connected designs of Fig. 9(c), with Fig. 19(a) and (b) showing the gain-frequency characteristics (S_{21}) and the transistor load impedance, inclusive of loading by $C_{\rm out}$, of the 3:1 series-connected design. Similarly Fig. 19(c) and (d) show (S_{21}) and the transistor load impedance of the 4:1 series-connected design. In the simulations of the 3:1 design, the transistor is treated as an ideal unilateral gain element with matched 16.7 Ω input impedance, and unity power gain when loaded with a $R_{L,\rm opt} = 16.7$ Ω load impedance, while simulations of the 4:1 design assume a matched 12.5 Ω output impedance. Because for power transistors $R_{L,\rm opt}$ is typically small in comparison with the transistor small-signal output impedance, both simulations assume a transistor small-signal output impedance of $5 \cdot R_{L,\rm opt}$. In these simulations $Z_{0,1-2} = 50$ Ω. The simulations with $\lambda/4$ lines correspond to $C_{\rm out} = 0$ fF, while the simulations with $\lambda/16$ lines corresponds to $C_{\rm out} = 96$ fF for the both 3:1 and 4:1 cases.

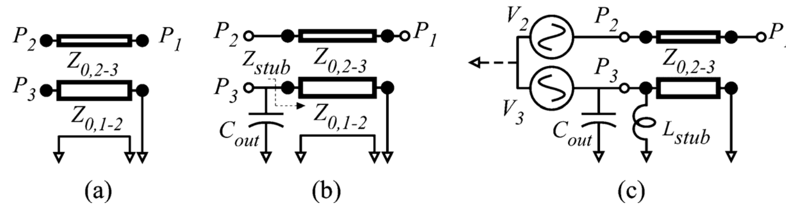

Fig. 17. Three-conductor transmission-line as a three-port voltage-summation device: (a) three-conductor line with one port short-circuited, (b) device with transistor output capacitance resonating with the stub inductance, and (c) equivalent circuit with shorted m_1-m_2 line represented by L_{stub}. The port input voltages V_2 and V_3 drive the line input in series.

TABLE II
SUMMARY OF RECENT MM-WAVE POWER AMPLIFIERS

Ref.	Tech. f_{max} / f_τ (GHz)	Freq. (GHz)	BW (GHz)	Max. S_{21} (dB)	P_{out} (dBm)	Peak PAE (%)	V_{CC} or V_{DD} (V)	Size (mm^2)	mW /mm^2
This work [17]	0.25 µm InP HBT 525 / 285	86	23	9.4	20.4	30.4	2.5	0.37 0.09*	294 1210*
This work [27]	0.25 µm InP HBT 525 / 285	86	33	10.2	20.8	35.0	2.5	0.43 0.14*	285 858*
This Work [20]	0.25 µm InP HBT 525 / 285	81	>11.5	17.5	26.7	23.4	2.75	1.06 0.46*	443 1020*
[4][c)]	0.14 µm GaN HEMT	91	7+	16.0	30.8	>20.0	17.5	2.25	530
[5][c)]	0.14 µm GaN HEMT 230 / 97	95	10+	18.0+	31.5+	20.5+	12.0	-	-
[10]	0.13 µm BiCMOS 270 / 240	62 84	>10 >8	20.6 27.0	20.1 18.0	18.0 9.0	1.8 2.5	0.72 0.68	142 93
[14][s)]	45 nm SOI CMOS	89	10+	10.3	15.8	11.0	2.8	0.37 0.05*	103 760*
[28]	0.18 µm BiCMOS 250 / 170	78	8.9	18.3	14	2.0	3.2	0.85*	29*
[29]	65nm CMOS	60	9	20.3	18.6	15.1	1.0	0.28*	256*
[30][c)]	90nm CMOS	60	8	20.6	19.9	14.2	1.2	1.76	55
[31]	40nm CMOS	80	15.2	18.1	20.9	22.3	0.9	0.19*	647*

*IC core area (excluding DC feed lines and RF pads), +Value estimated from figure, c)Corporate transmission-line power-combiners, s)Stacked PA.

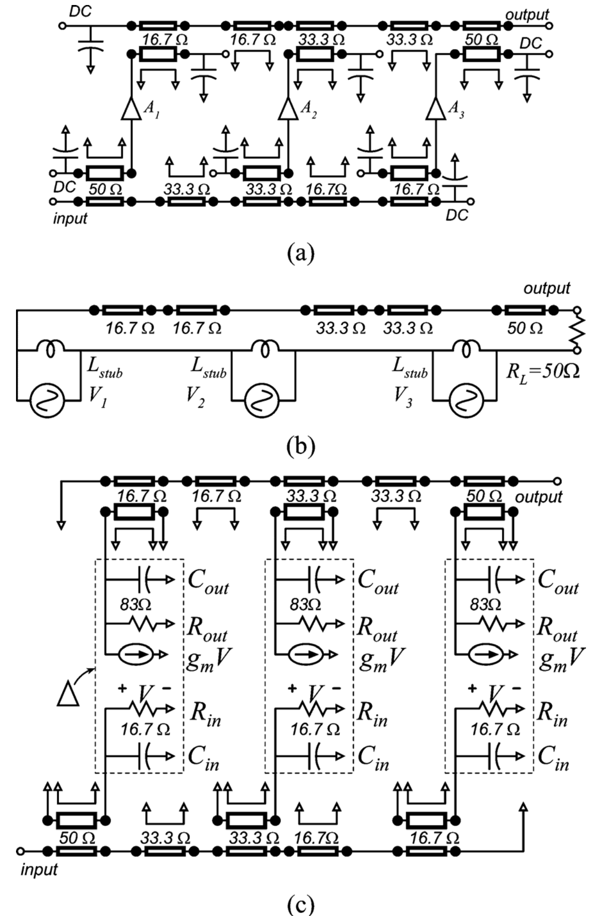

Fig. 18. Power amplifier with 3:1 series-combining using two-port voltage summation devices (a). Equivalent-circuit representation (b) of the output network. Each transistor cell is loaded by 16.7 Ω in parallel with an LC resonant network. The simulations of Fig. 19 assume a simplified transistor equivalent circuit model (c).

VII. BALUN AND TRANSMISSION-LINE TRANSFORMERS

In addition to either direct series connection or series connection using baluns, transistors in power amplifiers can also be connected in series using transformers with a segmented primary winding driven by multiple transistors [7]–[10]. Design of power amplifiers using such segmented transformers is closely related to that using baluns.

Fig. 20 examines the design of a segmented transformer with four inputs, similar to that of [10] but lacking the added windings which compensate port imbalances. The transformer has an upper winding m_3 above a segmented winding in m_2. The ground plane, in m_1, has an opening beneath the structure. We now describe the structure in terms of transmission-line modes on a three-conductor transmission-line, assuming for clarity and simplicity that the m_2 conductor is sufficiently wide to shield m_3 from m_1. With this simplifying assumption, we have two isolated transmission-line modes, i.e. with zero off-diagonal elements in the characteristic admittance matrix of (4); The first mode is between m_3 and m_2 and has characteristic impedance $Z_{0,2-3}$, while the second is between m_1 and m_2 and has characteristic impedance $Z_{0,1-2}$. Driven by the four signal sources V_1-V_4, each a voltage generator with some nonzero output impedance, with the indicated polarities, the upper and lower central points on the m_2 winding are at zero volts, and are virtual if not physical grounds.

The transformer is represented by the equivalent circuit of Fig. 20(b), where the sources V_1-V_4 are interconnected by four three-conductor transmission-lines. There are four

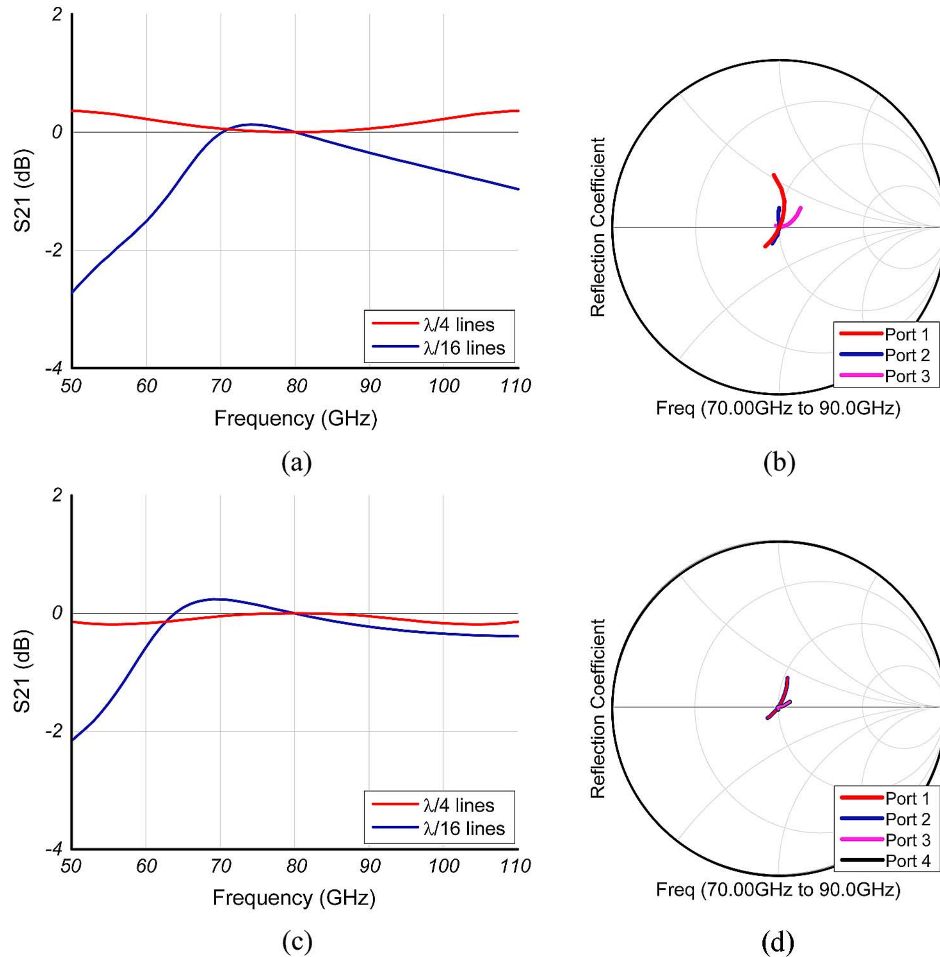

Fig. 19. Simulations, of the gain-frequency characteristics (a) and transistor load impedances (b), of a 3:1 series-connected design. Similarly (c) and (d) show the gain and transistor load impedances of a 4:1 series-connected design. The Smith charts of (b) and (d) are normalized to 16.7 Ω and 12.5 Ω.

short-circuited stubs in the m_1-m_2 transmission-line, these load (Fig. 20(c)) the sources V_1-V_4 with shunt inductive reactances $Z_{\mathrm{stub},a}$. As in the balun designs, these shunt inductances can tune in whole or in part the transistor output capacitances. There is a fifth short-circuited stub in the m_3-m_2 transmission-line; this appears as a series stub reactance $Z_{\mathrm{stub},b}$. The four sources V_1-V_4 are connected in series across the 50 Ω load, interspersed with three series transmission-line sections of characteristic impedance $Z_{0,2-3}$.

Unless appropriately designed, the transformer parasitic elements of Fig. 20(c) will introduce port-port imbalances and will cause the impedance presented to the generators to deviate from the 12.5 Ω which would arise in the absence of transformer reactances. The impedances $Z_{0,2-3}$ of lines B-D load the four sources with series inductance and shunt capacitance. There is a delay imbalance 2τ between the generators (V_3, V_4) and the generators (V_1, V_2) arising from transmission-lines B and C between these pairs of generators. Finally, the short-circuit stub impedance $Z_{\mathrm{stub},b}$ associated with the m_3-m_2 mode of line A is in series with the generators (V_3, V_4).

These high-frequency impairments can be eliminated by modifying the transformer design (Fig. 21(a)). There are four modifications. First, in line section A, the m_3-m_2 transmission-line is eliminated, with the end of the m_3 winding connected by a via to m_2 at the connection point to the generator V_4. The transformer secondary winding is consequently $3/4$ of a turn. Second, in line sections B and C the widths of m_3 are adjusted such that the m_3-m_2 transmission-line mode has characteristic impedance $Z_{0,2-3} = 25\ \Omega$. Third, in line section D the width of m_3 is adjusted such that $Z_{0,2-3} = 50\ \Omega$. With these modifications, in the transformer equivalent circuit (Fig. 21(b) and (c)) the parasitic series stub impedance $Z_{\mathrm{stub},b}$ is eliminated, the four m_2-m_1 shunt-stub inductive reactances $Z_{\mathrm{stub},a}$ again tune the transistor output capacitances C_{out}, and at the amplifier center frequency the m_3-m_2 characteristic impedances $Z_{0,2-3}$ of lines B, C, and D are all matched to the surrounding circuit and introduce neither series inductive nor shunt capacitive parasitic reactances. With these design decisions, the transformer equivalent circuit (Fig. 21(c)) is identical to that of the 4:1 series-connected balun power-combiner (Fig. 21(d)).

To add in phase, V_1 and V_2 must be delayed by 2τ, the transmission-line delay of line sections B and C, relative to V_3 and V_4. This is accomplished by using an identical transformer as

Fig. 20. Segmented power amplifier output transformer (a), equivalent-circuit representation using three-conductor transmission-lines (b), and reduced equivalent circuit (c) with the short-circuited stubs represented by inductive reactances.

an input power-splitter (Fig. 21(d)). Fig. 21(e) shows the resulting amplifier schematic; design is similar to the 4:1 series-connected amplifier of Fig. 9(c). Designs using these principles have been reported by Daneshgar [27].

VIII. Conclusion

Power amplifiers of 0.1–1 W output power will enable long-range and high-capacity millimeter-wave radar and imaging systems. High power-added efficiency results in low system DC power and heat-sinking costs, while high output power per unit die area reduces power amplifier cost and enables high output power in phased arrays. Given the low breakdown voltage of millimeter-wave transistors, series power-combining techniques permit increased output power per unit die area. Series power-combiners using sub-quarter-wave baluns complement direct series connection as a compact, area-efficient combining technique. Analysis of the propagating transmission-line modes on segmented transformer provides insights into the high-frequency parasitics associated with these series power-combiners. Given appropriate design, balun-based series combiners and segmented transformer are similar in their operation.

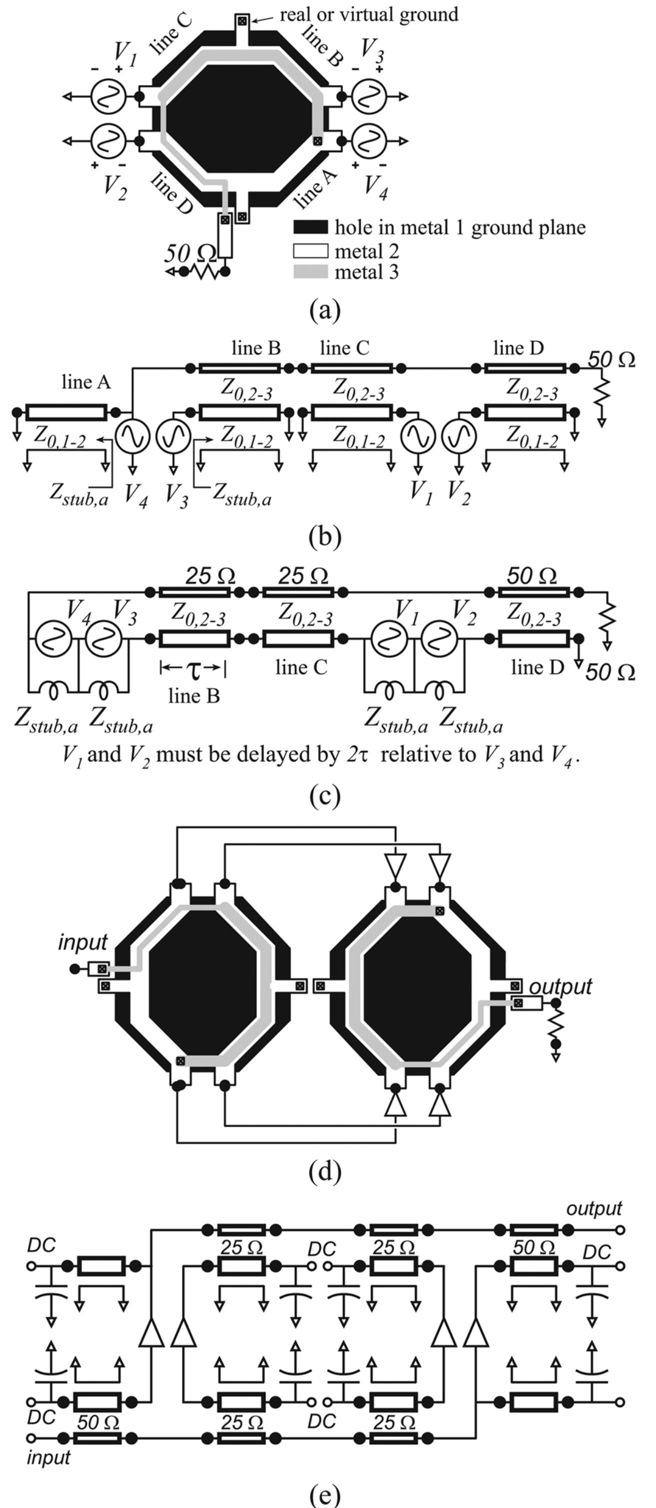

Fig. 21. Modified segmented transformer (a) with a controlled-impedance and stepped-impedance $3/4$-turn secondary winding, equivalent-circuit representation using three-conductor transmission-lines (b), reduced equivalent circuit (c) with the short-circuited stubs represented by inductive reactances, (d) power amplifier with a similar input transformer providing appropriate phase-matching, and its equivalent circuit (e). The output power-combiner is similar to that of Fig. 5(c), while the power amplifier equivalent circuit (e) is similar to that of Fig. 9(c).

Acknowledgment

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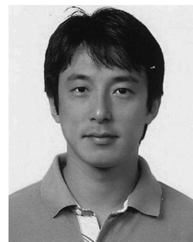

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