Design and Simulation of Two-Dimensional Superlattice Steep Transistors

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***Abstract*— We report design of double-gate metal–oxide–semiconductor field-effect-transistors having InGaAs/InAlAs superlattices between the N+ source and a planar InGaAs channel. As with nanowire superlattice transistors, the 2-D superlattice bandgap reduces injection into the channel of electrons having energy above the source Fermi energy. Simulated ballistic transport characteristics of FETs using a three-well superlattice show 29–37.5-mV/decade minimum subthreshold swing and 390-A/m ON-current given 0.1-A/m OFF-current and a 0.2 V power supply.**

***Index Terms*— MOSFETs, MOS devices.**

I. Introduction

VLSI power dissipation seriously constrains performance [1]. Low switching energy requires a low power supply voltage, yet decreased standby power requires either increased voltages or reduced transistor subthreshold swing ($S.S.$). In MOSFETs, thermal carrier injection limits $S.S.$ to 60mV/dec [1]. Efforts have been made [1]–[6] to obtain steeper characteristics. In tunneling MOSFETs, on-current (I_{on}) is significantly reduced [2]. In superlattice *nanowire* transistors [4]–[6] a superlattice energy filter between the N+ source and the channel suppresses the injection of high-thermal-energy electrons, reducing $S.S.$, in simulations [5], [6], to 13mV/dec.

Here we show that such superlattice energy filters can also be used in transistors having planar, two-dimensional channels. Such planar FETs may prove to be more easily fabricated. Further, with nanowire FETs, high I_{on} per unit die area demands small nanowire pitch. In the planar case, design is complicated by the dependence of the superlattice band structure on the wave vector, k_t, transverse to the transport direction.

II. Two-Dimensional Superlattice Transistors

In a planar FET, the drain current I_D is proportional to

$$I_D \propto \int_{-\pi/a}^{\pi/a} \int_{-\infty}^{+\infty} (2q/h) \cdot (W/\pi) \cdot T(E,k_t) f(E) dE dk_t, \quad (1)$$

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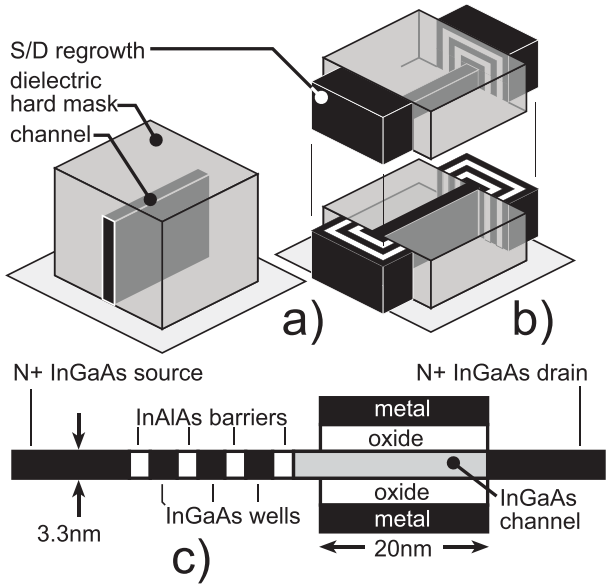

Fig. 1. Planar superlattice transistor: proposed fabrication by encapsulating a fin (a) in a dielectric and subsequently (b) forming the superlattice by MOCVD regrowth. Cross-section of structure assumed in simulations (c).

where W is the channel width, a the lattice constant, and $T(E,k_t)$ the energy-dependent total transmission, *i.e.* the transmission probability per mode summed over all modes having energy E and transverse wave vector k_t, and $f(E)$ the source Fermi distribution. For energies below E_{bc}, the channel barrier energy, $T(E,k_t) \approx 0$; above the barrier $T(E,k_t)$ approaches the number of above-barrier conducting modes present at each k_t. MOSFET 60mV/dec. subthreshold characteristics arise from the $e^{-K_B t}$ variation in $f(E)$ above the Fermi level; the superlattice introduces a sharp reduction in $T(E,k_t)$ at energies within the superlattice bandgap. If the source Fermi level is aligned with the energy maximum E_m of the 1st superlattice passband, $T(E,k_t)f(E)$ will decrease more rapidly with energy than $e^{-K_B t}$, and the subthreshold characteristics will be steeper than 60mV/dec.

Such transistors might be fabricated (fig. 1a,b) using processes similar to those used to fabricate nanowire- and finFETs [7], first forming an InGaAs fin and then forming the superlattice through MOCVD growth [8] of InGaAs and InAlAs layers. If (fig. 1b) the superlattice is present in the drain, reflections from this may distort the output characteristics [9], or drain resistance increased because electrons must thermalize before crossing the drain superlattice; if necessary, this can be eliminated by separately growing a conventional N+ drain. In fig. 1b, transport in the source superlattice is radial, whereas in fig. 1c, source transport

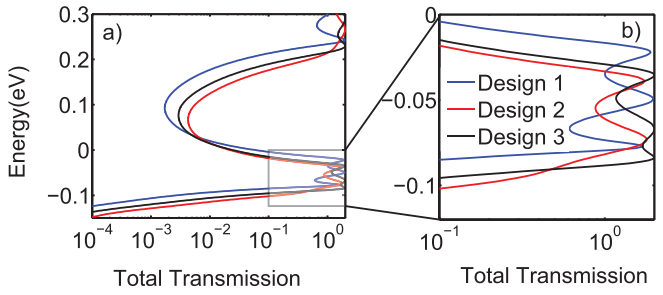

Fig. 2. Total transmission, versus energy, for the three superlattice designs, described in the text. On-state bias ($V_{GS} = V_{DS} = 0.2$ V).

is planar; with radial transport, the varying lateral confinement with distance from the channel will shift the superlattice energy levels relative to the case of a planar superlattice (fig 1c). These energy levels should be appropriately adjusted to maintain the desired transmission characteristics by adjusting the individual well and barrier layer thicknesses. Given available quantum transport simulators, we simulate the structure of fig. 1c; the structure of fig. 1b suggests how structures of similar characteristics might be fabricated.

III. Simulation and Design

We analyze double-gate MOSFETs (fig. 1c) with a 3.3nm thick undoped $In_{0.53}Ga_{0.47}As$ channel, 20nm gate length, and a 2.56nm thick gate dielectric having $\varepsilon_r = 20$. A superlattice with three $In_{0.53}Ga_{0.47}As$ wells and four undoped $In_{0.52}Al_{0.48}As$ barriers lies between the $N_D = 2.5 \cdot 10^{19}\text{cm}^{-3}$ doped InGaAs source and the channel. Doping the wells at $N_D = 10^{19}\text{cm}^{-3}$ aligns, at $V_{GS} \sim 0.2$ V, the source and superlattice well conduction bands, maintaining high transmission, hence high I_{on}; the well energies are then not aligned $V_{GS} = 0$V, as will be shown subsequently. Ballistic transport properties are simulated by the quantum transmitting boundary method [10], [11], with N+ regions in thermal equilibrium [11], band structure described by tight binding with an $sp^3d^5s^*$ basis [12], and with the Schrödinger and Poisson equations solved self-consistently, using the NEMO5 nanoelectronics modeling software [13]. The simulations include source-drain tunneling. Contact resistance and dielectric D_{it} are neglected; their effects can be small [14], [15]. At 0.2V drain bias, band-band tunneling in the InGaAs channel is negligible [15]. Surface roughness and bulk defect scattering are not included in the simulation, which primarily focuses on modeling the superlattice energy filtering.

By adjusting the barrier and well thicknesses [16], [17], the passband transmission can be increased, increasing I_{on}. Fig. 2 compares transmission of three designs; all have 12 monolayer (ml) length wells, but design 1 has 5ml barriers, design 2 has 3ml, 6ml, 6ml and 3ml barriers, and design 3 has 4ml, 6ml, 6ml and 4ml barriers. Design 3 has the largest and most uniform passband transmission. Except for fig. 7, subsequent figures will show simulations of design 3.

In a two-dimensional superlattice, the miniband energies vary with transverse momentum k_t (fig. 3), with $E_m(k_t)$ increasing as $\sim k_t^2$. If k_t is large, electrons with energy far above the source Fermi level may pass through the superlattice. Yet, steep subthreshold slope can still be maintained because the channel barrier $E_{bc}(k_t) \cong E_{bc}(0) + \hbar^2 k_t^2/2m^*$ also

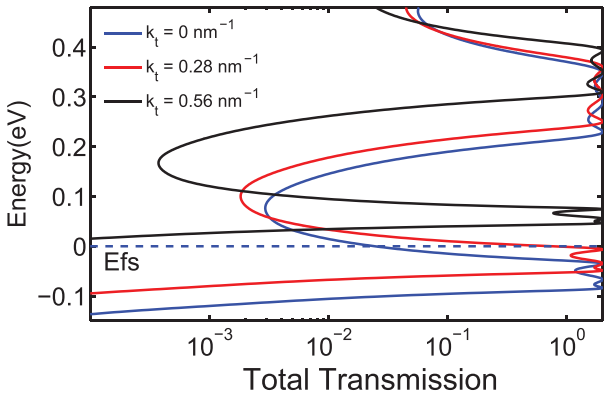

Fig. 3. Total mode transmission of design 3 as a function of transverse wave vector k_t, under on-state bias ($V_{gs} = 0.2$ V). E_{fs} is the source Fermi level.

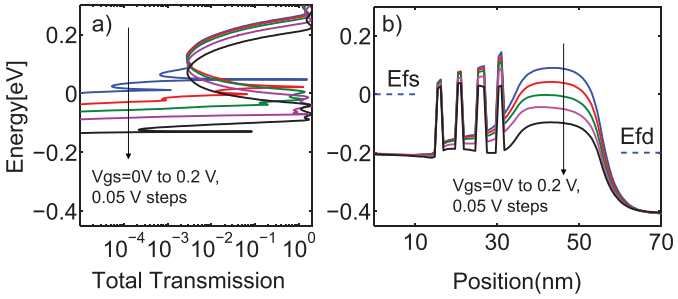

Fig. 4. (a) Transmission for the wave vector $k_t = 0$, and (b) conduction band profile across the device for gate voltages ranging from = 0 V to 0.20 V with a step of 0.05 V, at $k_t = 0$ at a 0.2 V source-drain voltage V_{DS}.

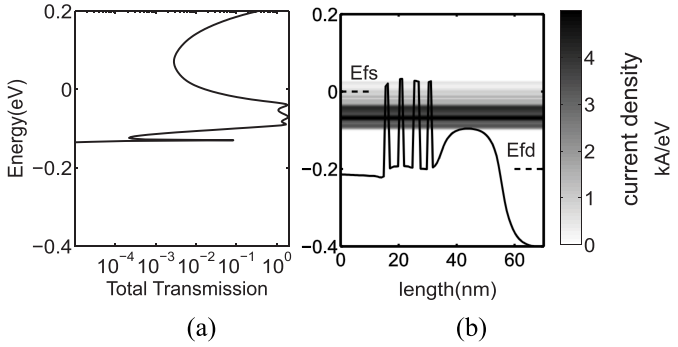

Fig. 5. Total transmission T at $k_t = 0$ (a) and energy-resolved current density, $W^{-1}dI_D/dE$ (b). In these plots, $V_{GS} = 0.2$ V and $V_{DS} = 0.2$ V.

increases with k_t. If $\partial^2 E_m/\partial k_t^2 < \partial^2 E_{bc}/\partial k_t^2$, then with the FET biased below threshold, i.e. with $E_{bc}(0)$ above the superlattice passband maximum $E_m(0)$ for zero transverse momentum, the barrier energy will remain above the passband with nonzero k_t. This suppresses transmission.

Fig. 4a shows the total energy-dependent mode transmission $T(E, k_t)$, and fig. 4b the band diagram, as function of gate-source voltage V_{gs}, with $k_t = 0$. As V_{gs} varies, the field within the superlattice changes, changing its transmission; at $V_{gs} = 0$V, there is a narrow range of energies, ~0.05eV, at which the superlattice fails to strongly suppress injection. Fig. 5a shows total transmission at $k_t = 0$, while fig. 5b shows the energy-resolved current density, $W^{-1} \cdot \partial I_D/\partial E$. Transport is strongly confined to within the 1st superlattice passband.

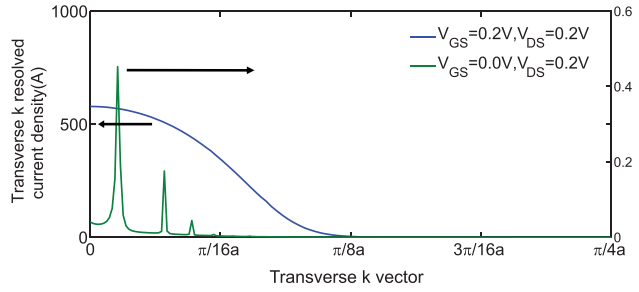

Fig. 6. Drain current density $W^{-1}dI_D/dk_t$ resolved as a function of transverse wave vector k_t, under both on-state ($V_{GS} = 0.2$ V , $V_{DS} = 0.2$ V) and off-state ($VGS = 0.2$ V , $V_{DS} = 0.2$ V) bias. The lattice constant is denoted by a.

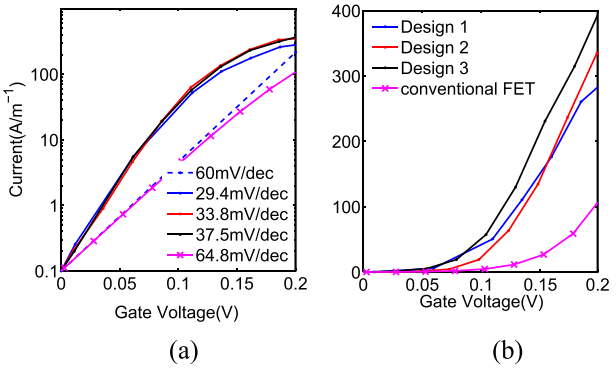

Fig. 7. Simulated transistor drain current I_D, in A/m, as a function of V_{GS}, with logarithmic (a) and linear (b) scales, at $V_{DS} = 0.2$ V for designs 1, 2, and 3. Threshold voltages were adjusted for $I_{off} = 0.1$ A/m at $V_{GS} = 0$ V and $V_{DS} = 0.2$ V.

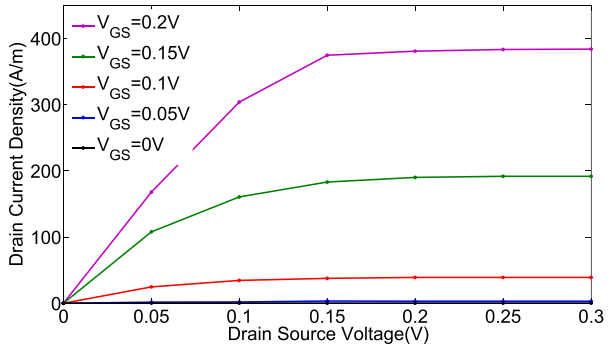

Fig. 8. Simulated common-source output characteristics with the threshold set such that $I_{off} = 100$ nA/μm.

Fig. 6 shows drain current density (I_D/W), resolved as a function of the transverse wave vector k_t, i.e. $W^{-1} \cdot \partial I_D/\partial k_t$. With the transistor off ($V_{GS} = 0$V, $V_{DS} = 0.2$V), leakage is dominated by resonant tunneling peaks which arise (fig. 4) as the applied V_{GS} misaligns the superlattice well energies, distorting the transmission characteristics. Because the channel barrier $E_{bc}(k_t)$ and the superlattice miniband energy $E_m(k_t)$ increase with increased k_t, I_{on} (at $V_{GS} = V_{DS} = 0.2$V) is carried primarily by modes with small k_t (fig. 6).

Fig. 7 compares transfer characteristics. Design 3, which shows the most uniform passband transmission (fig. 2), also exhibits the largest I_{on}, at 390 A/m, with $V_{GS} = V_{DS} = 0.2$V and $I_{\text{off}} = 0.1$ A/m. A conventional FET, otherwise identical, but lacking the superlattice, shows I_{on} =109 A/m, with $V_{GS} = V_{DS} = 0.2$V and $I_{\text{off}} = 0.1$ A/m. Minimum subthreshold swings are 29.4, 33.8, 37.5mV/dec. for designs 1, 2, and 3. Fig. 8 shows common-source characteristics of design 3. The barriers in design 3 differ from those of designs 1 and 2 by only 1 ml in thickness; adequate control of I_{on} requires that superlattice layer thicknesses be held to within 1 ml of the intended value. Atomic layer epitaxy [8] may enable such precision.

IV. Conclusion

Superlattice energy filters, earlier studied in 1-D nanowire transistors, also can provide subthreshold swings smaller than 60mV/dec. in planar and fin transistors. At 20nm gate length, with a 3.3nm thick channel and 0.5nm EOT gate dielectrics in a double-gate configuration, $I_{\text{on}} = 390$ A/m is simulated in the ballistic limit, with a low 0.2V supply and 0.1A/m I_{off}. These transistors are potentially attractive for low-power logic.

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