Challenges and Opportunities for High Frequency InP Integrated Circuits

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***Short-Abstract*—Recent advances in InP semiconductor device design and high-yield processing have led to the demonstration of transistors with power gain cut-off frequencies (f_{max}) greater than 1 THz. More importantly, the devices are supported by low-loss interconnects, accurate models and robust design kits. Employing a systematic design methodology that includes significant EM and thermal modeling, we have demonstrated circuit components for transceivers up to 670 GHz and power amplifiers with >100mW of output power operating at 230 GHz. Insertion of these high frequency chips requires additional breakthroughs in packaging, and thermal management. Other applications of the technology would allow the high gain-bandwidth to be traded for high dynamic range and efficiency at mmWave frequencies.**

I. Introduction

Recent advances in InP transistor technology has made inroads into the so-called THz-gap that exists between electronics and photonics. For the first time we now have transistors with gain well above 1 THz. The transistors are supported by interconnect and waveguide-to-chip transitions that have enabled the demonstration of gain stages up to 850GHz, oscillators, mixers, and dynamic dividers up to 670GHz, and power amplifiers and phase-locked-loops at 220GHz. If we take the natural length scale of the electronics circuit as roughly the wavelength, we are now faced with the challenge of integration and packaging.

II. Transistors

InP offers the combination of high electron velocity and breakdown field with lattice matched InGaAs/InAlAs heterostructures. The combination allows devices with unity current gain cut-off frequencies f_τ above 650GHz. Advances in epitaxial growth and process control have further reduced parasitic resistances and capacitances to push maximum power gain frequencies f_{max} above 1 THz [1-3]. InP based double heterostructure bipolar transistors (DHBTs) and high electron mobility transistor (HEMTs) are now the fastest three-terminal devices in the world. The HEMTs are suitable for low-noise amplifiers and low-loss switches. The DHBTs offer mV level threshold uniformity and higher breakdown voltage making them ideal for a wide range of high-speed digital, mixed-signal, and analog applications where dynamic range is important.

The primary challenge to device scaling for the InP HEMTs has been the development of a repeatable T-gate process down to 20nm gate lengths. Maintaining high yield on recess etching, minimizing fringe capacitances, keeping the contact resistances low and developing a backside process for wafers thinned to well below 1 mil are significant challenges as well. The challenges in the 130 nm InP DHBT have been the development of low contact-resistances and reduction of fringing capacitances. A low-loss wiring environment suitable for MMICs has been developed, but has not been sufficiently scaled for dense mixed-signal ICs.

Accurate device models have been developed and validated by comparing simulations and measurements. Typical intrinsic capacitances are ~fF/μm of device periphery, placing a premium on reduction of parasitic capacitances and accurate metrology during parameter extraction. Contact resistances are in the range of 100 Ohm- μm. Inductances intrinsic to the device have to be included to obtain high fidelity between measurement and model at sub-mmWave frequencies.

Both HEMTs and DHBTs have been demonstrated on the same wafer using selective area regrowth. Growth and process advances make HEMT/DHBT integration attractive for future chips, especially since there is a significant loss associated with chip-to-chip transitions. Low power logic remains a missing piece in the InP design kit.

III. Circuits

Circuits using the devices described in the previous section have been realized. Measurements match simulation closely as models and design kits have matured and a systematic design methodology has been developed. Electromagnetic simulations that take into account the layout and biasing are required. The HEMT technology uses a relatively conventional MMIC process with microstrip wiring and a ground plane on the backside of the wafer, typically thinned below 1mil. The DHBT technology employs up to four levels of metal interconnect embedded in a low-loss BCB dielectric. The DHBT circuits use inverted microstrip wiring and require through substrate vias for substrate mode suppression [4].

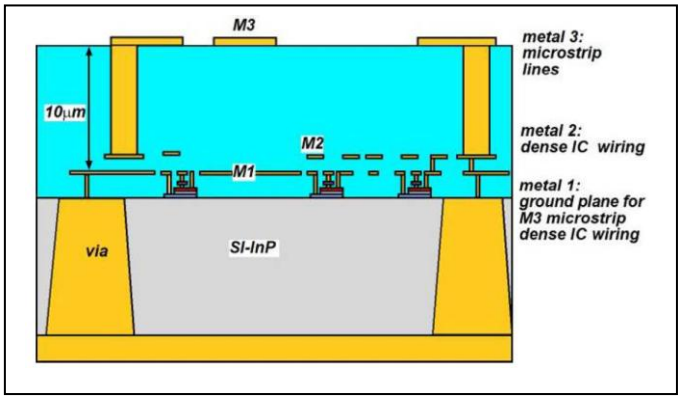

Figure 1: InP DHBT interconnect cross-section showing the ground-plane at M3, low-loss THz microstrip lines at M2 and inverted CPW-G transmission lines at M1. Vias are used to suppress substrate modes.

A. Low Noise Amplifiers

The lowest noise figure is obtained with InP HEMTs. Circuits with gain at 850 GHz have been fabricated and will be published later this year. The most recent published results for a HEMT LNA are at 670 GHz where a 30nm HEMT technology showed a 12.5 dB noise figure in a package [4]. Amplifiers built in the DHBT technology have shown noise figures of 10.4 dB at 265 GHz [5]. In comparison, LNAs built in 35nm HEMT technology have demonstrated a noise figure of 7.5dB at 270GHz [6].

B. Power Amplifiers

Amplifiers at 670 GHz have demonstrated 3mW output power with HEMTs [7, 8] and 0.9 mW in DHBTs [9]. A number of results have been published at 200GHz with sub-50nm gate-length HEMT power amplifiers delivering 75 mW at 210 GHz [10] and 250nm emitter-width DHBT chips cooled with -20C forced air delivering 180 mW at 214 GHz [11]. The HEMT amps produce about 78mW/μm of gate periphery while the DHBT devices produce 234mW/μm of emitter periphery or 0.94mW/μm^2 of emitter area. The DHBT measurements were conducted on full-thickness wafers and are almost certainly thermally limited. Preliminary thermal modeling of these structures indicates that the DHBT junction temperatures are above 200C. Measurements on smaller DHBT die showed 2.5x higher power density of 0.6W/mm at 250GHz, albeit at a lower total output power of 60mW [11]. The difference in the power density in the DHBT results could be attributed to power combining losses and device self-heating.

Recent amplifier results are summarized in Fig. 2 showing output power as a function of center frequency for a single MMIC [4-18]. The plot does not capture the importance of parameters such as bandwidth, efficiency, and gain. Such parameters explain the difference between the widely varying GaN results plotted at W-band. The lower power result represents a relatively wideband amplifier. The GaAs results are relatively dated, but included for comparison.

C. Transitions and Integration

The circuits described in the previous section were measured on-wafer and in waveguide blocks. On-wafer measurements are now increasingly straightforward with the expanded operating frequency of on-wafer probes. Wire bonding is considered an acceptable practice up to 300GHz [4], and often a separate transition element is used between the MMIC and the wave guide. At higher frequencies, in particular the 670 GHz results, the waveguide-to-chip transition is monolithically integrated onto the MMIC itself [3, 4]. Integrated transitions can be E-plane probes or dipoles that extend into the waveguide. The "transition loss" associated with getting on and off the chip could be greater than 3 dB, placing a premium on integrating greater functionality on chip.

Both HEMT and DHBT technologies have been employed to build monolithic receivers. The DHBT receiver and transmitters includes voltage controlled oscillators, dividers, mixers, buffers, and gain stages on chip. The DHBT technology lends itself to higher levels of integration, favored by mV threshold uniformity and larger critical dimensions for similar performance. Emitter dimensions for the DHBT technology are well within the capability of relatively inexpensive optical lithography tools, offering higher uniformity, and yield.

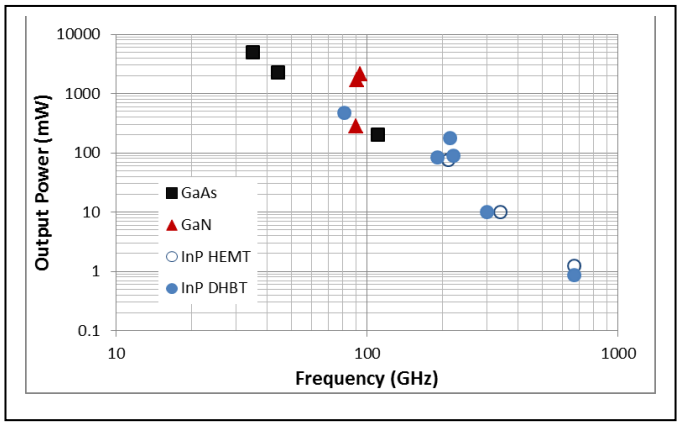

Figure 2: Maximum output power from a single MMIC as a function of frequency.

IV. Challenges and Opportunites

A. Thermal Management

Shrinking wavelengths necessitate circuit functionality to be packed into smaller size chips. Power amplifier die are a few mm on a side, but manage only a few percent in power added efficiency. Fast devices usually trade breakdown voltage for gain, leading to reduced voltage swings and less efficient circuits. Of course, gain is still a premium at these frequencies.

The 200GHz power amplifiers described above dissipate approximately 2W of heat in about 0.1x1 mm^2 section of the die. If the InP die is thinned to a few mils, that translates to a heat-flux of ~2 kW/cm^2 at the bottom of the die. The thinned InP substrate is not an efficient heat spreader. Compact or integrated heat spreading techniques are critical to the

development of components at these frequencies. Increasing the number of devices and/or reducing their power density will require efficient power combining.

B. Packaging

Typical die areas are small, modest levels of integration are possible (mm-periphery) and the DHBT technology uses high-yield, high-throughput, optical lithography to support relatively low cost chip fabrication. However, heat removal, transition losses, and size constraints combine to make packaging a key challenge at these frequencies.

Components at mmWave are expensive and have limited the development of systems. Above W-band we have been limited to bulky brass blocks with limited functionality for each component. Now that chips with useful power, performance and integration levels are being demonstrated we are ready to develop IC-based components for specific applications. At 200-300GHz we have demonstrated adequate gain to trade for reasonable efficiency, dynamic range and bandwidth. Output power can be increased by building arrays of Tx/Rx channels with phase control. Wide bandwidth communications, compact sensors, and mm-Wave imaging systems are obvious platforms enabled with the technology described.

Natural building blocks would be linear or 2-D arrays of integrated transmitters and receivers. Arrays offer increased power and steered beams. A common, enabling, building block would be a small linear array. Each channel would include gain control and/or phase control. The advantage of starting with a linear array is straightforward access to the chip for signal lines, DC biasing, and heat removal.

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