III-V MOS: Planar and Fin Technologies

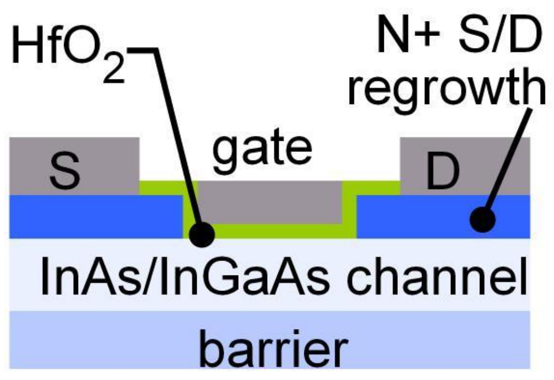
M.J.W. Rodwell, UCSB

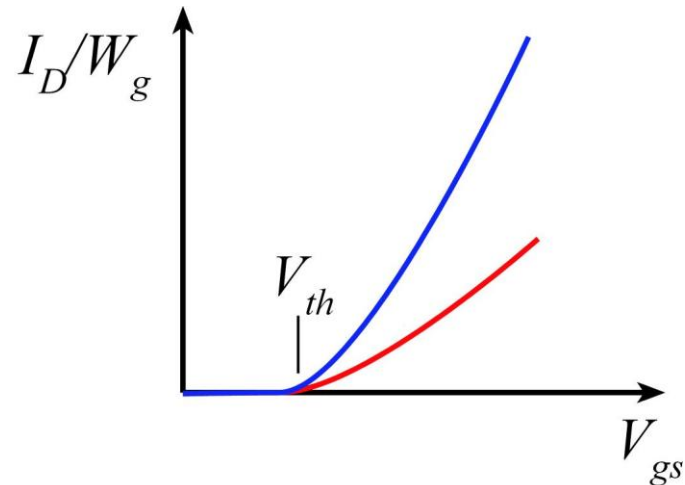
III-V MOS: *S. Lee, C.-Y. Huang, D. Elias, V. Chobpattanna, J. Law, A.C. Gossard, S. Stemmer, UCSB; T. Kent, A. Kummel, UCSD; P. McIntyre, Stanford.*

Transport Modeling: *P. Long, S. Mehrotra, M. Povolotskyi, G. Klimeck, Purdue*

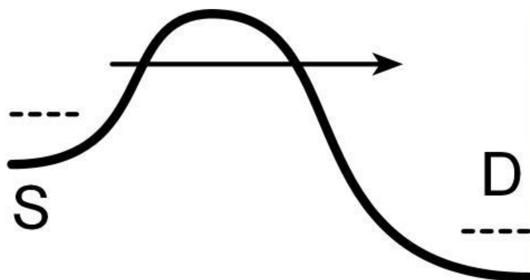
Why III-V MOS ?

III-V vs. Si: Low m*→ higher velocity. Fewer states→ less scattering → higher current. Can then trade for lower voltage or smaller FETs.



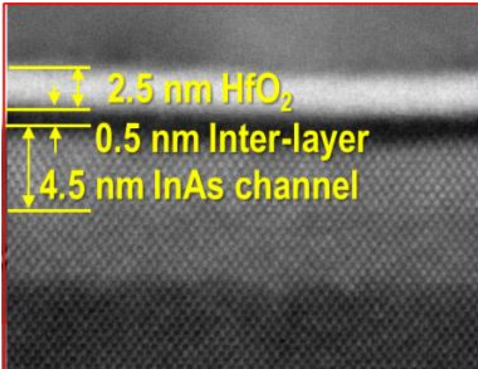


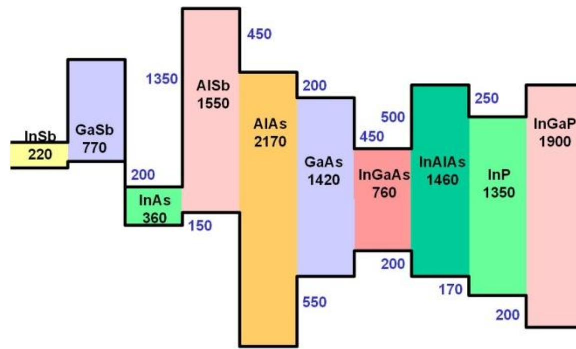
Problems: Low m*→ less charge. Low m* → more S/D tunneling.
Narrow bandgap→ more band-band tunneling, impact ionization.

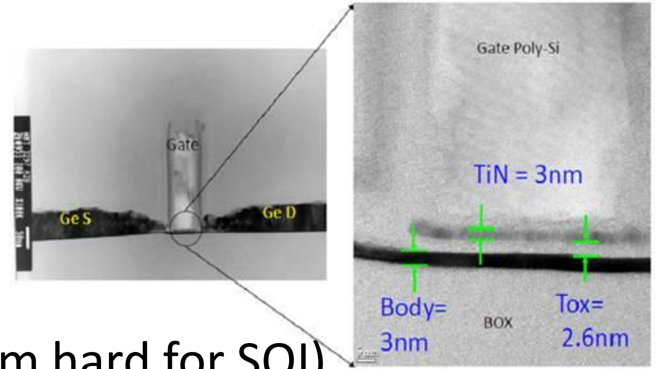


Why III-V MOS ? → important but less well-known reasons

nm-precise epitaxy, large heterojunction ΔE_C → 1nm thick channels



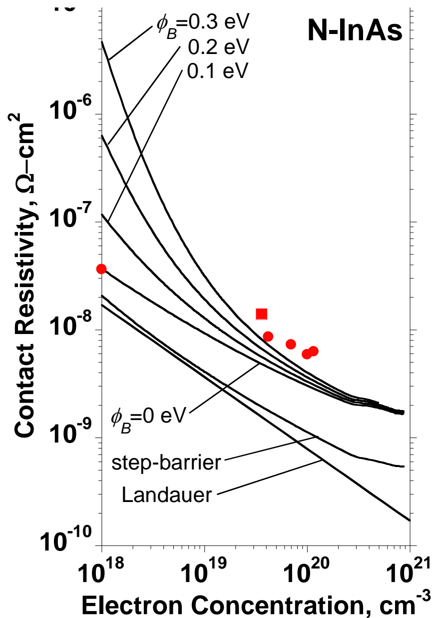




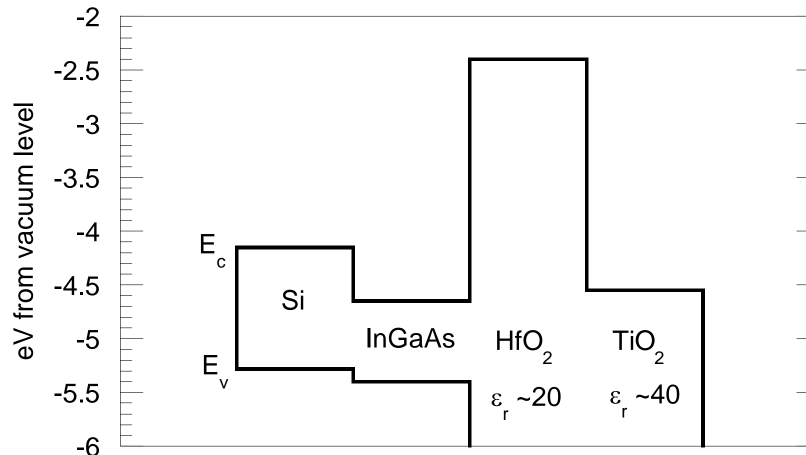
(1nm hard for SOI)

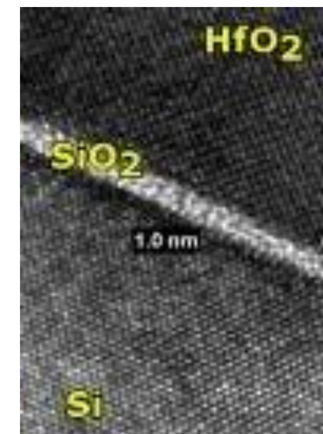
Y-K. Choi et al, VLSI Tech. Symp., 2001

Excellent contacts now.
Better contacts feasible.



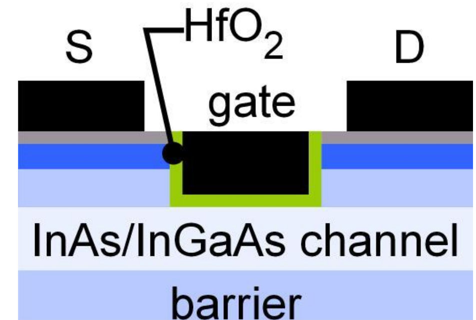
Dielectric-channel interface:
Large ΔE_C, no SiO_2 at interface → smaller EOT





http://nano.boisestate.edu/research-areas/gate-oxide-studies/

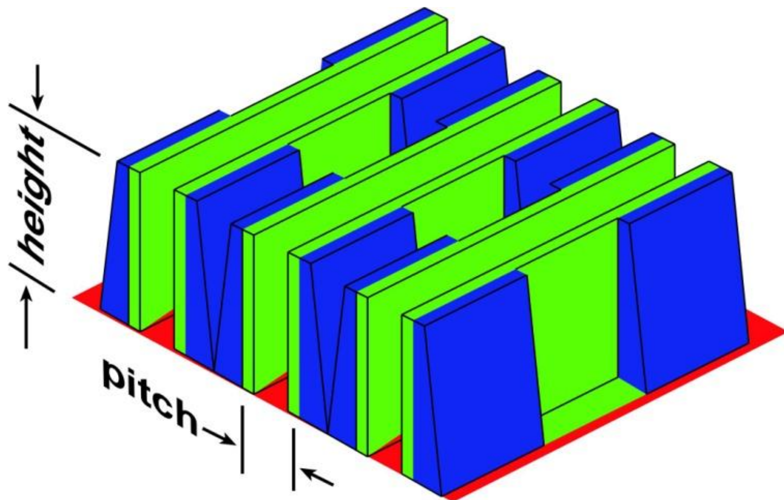
III-V MOS: how small can we make L_g ?

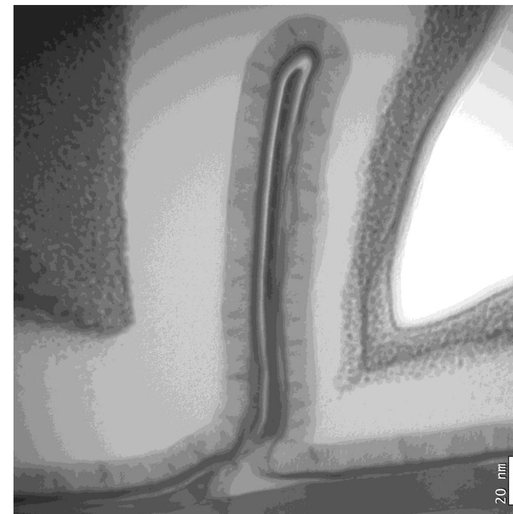


Planar UTB FETs might just scale to 10nm L_g:

- nm epitaxial control of channel thickness
- high-energy barriers (AlAsSb)
- possibly thinner high-K than in Si.
- vertical spacer greatly aids short-channel effects
- simulations suggest that, with spacers, even S/D tunneling is OK.

And with ALE techniques, few-nm-L_g III-V finFETs are also feasible.





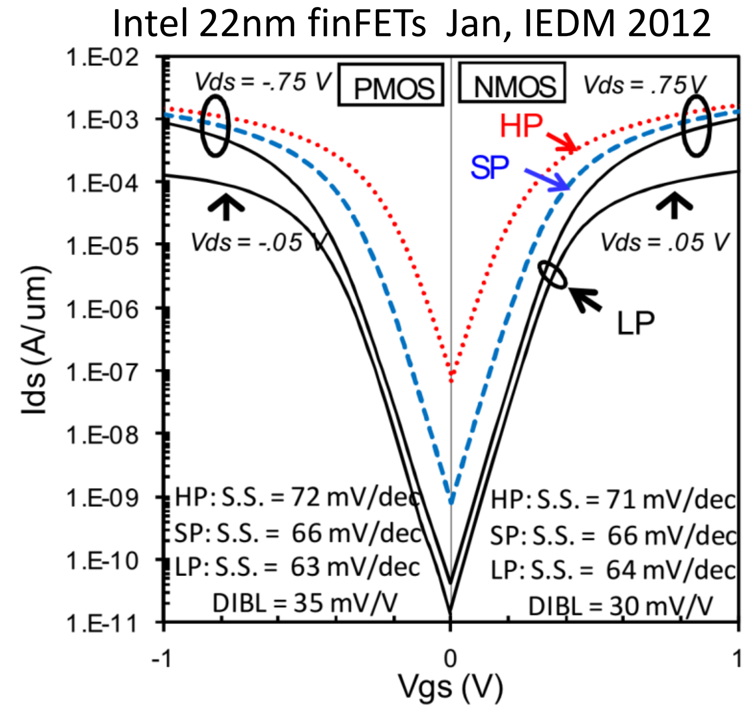
The Key question:

Compared to Silicon MOS,...

...can we get high I_{on} ,

..and low I_{off} , and low V_{DD} ,

...at a VLSI-relevant (8-10nm) technology node ?

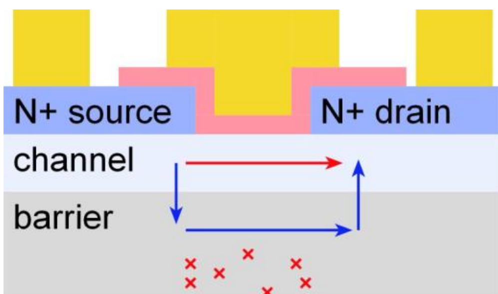


Performance @ e.g. 35nm is not important !

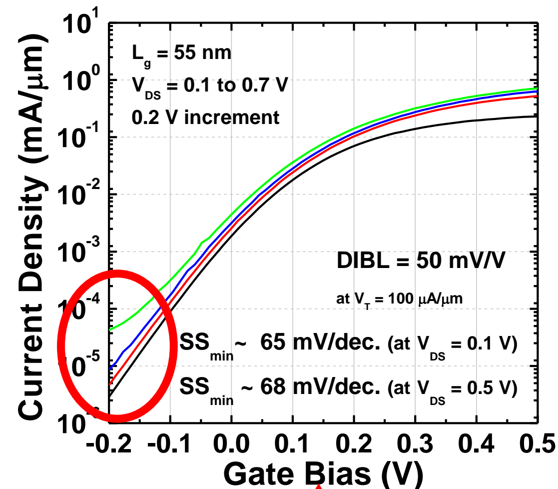
Small S/D pitch, not just small L_g, is essential !

Leakage, short-channel effects, performance comparisons

off-state leakage mechanisms:

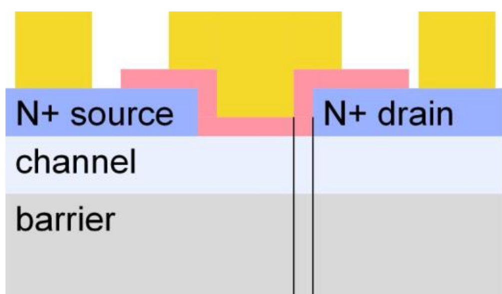


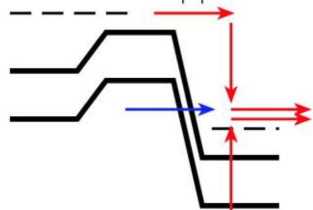
electrostatics / aspect ratio
bottom barrier injection
growth defects



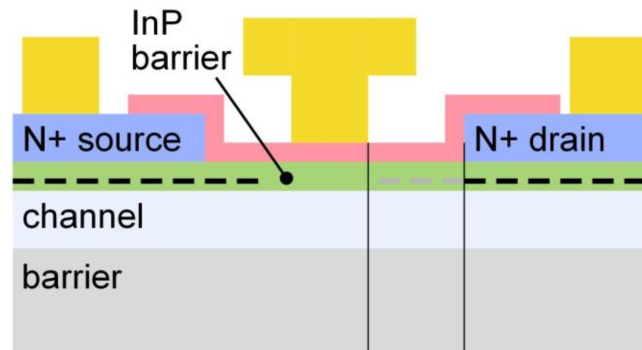
Band-band tunneling, S/D tunneling, impact ionization

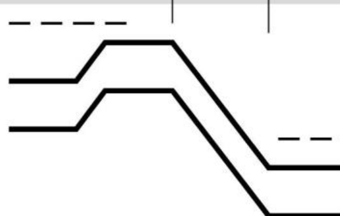
Small S/D contact pitch



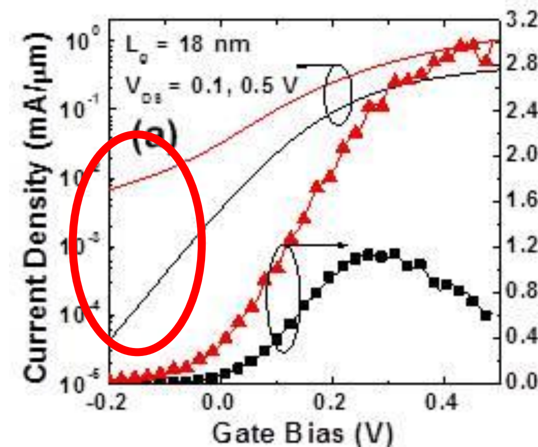


MOS-HEMT with large contact pitch





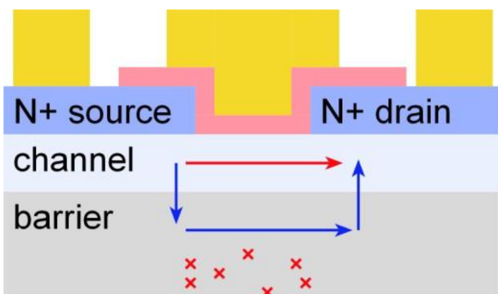
vs.



Lateral depletion region reduces severity of most short-channel effects (not VLSI-compatible)

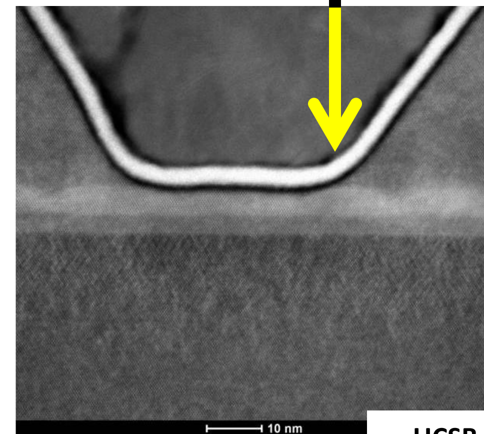
Leakage, short-channel effects, performance comparisons

off-state leakage mechanisms:



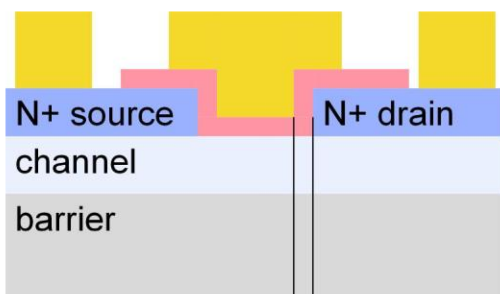
electrostatics / aspect ratio
bottom barrier injection
growth defects

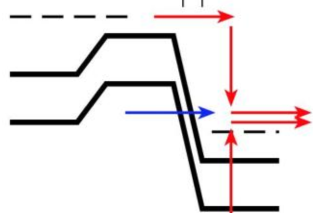
no lateral gate-drain space



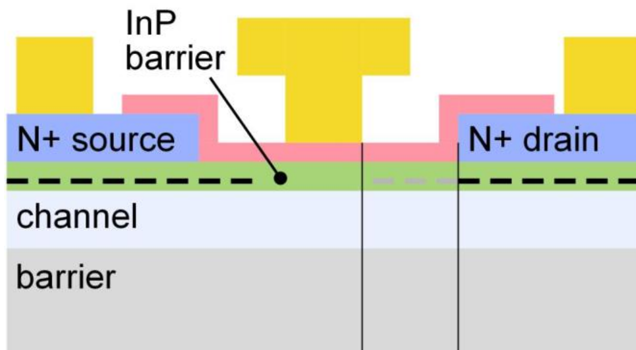
Band-band tunneling, S/D tunneling, impact ionization

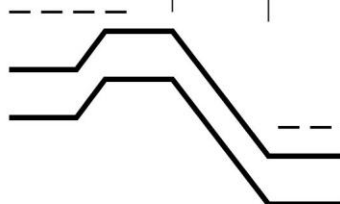
Small S/D contact pitch



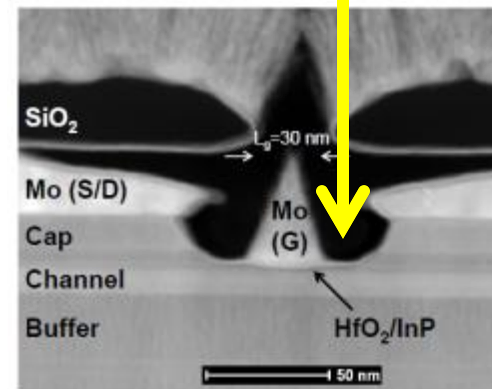


MOS-HEMT with large contact pitch





~20 nm gate-drain space

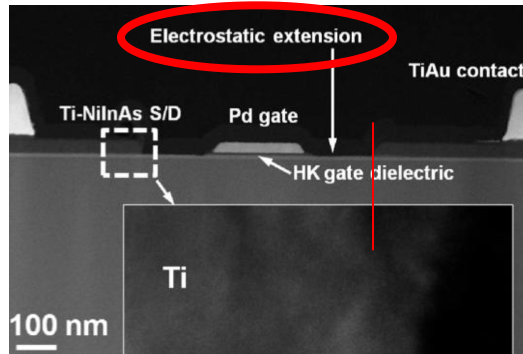


Lin, IEDM2012

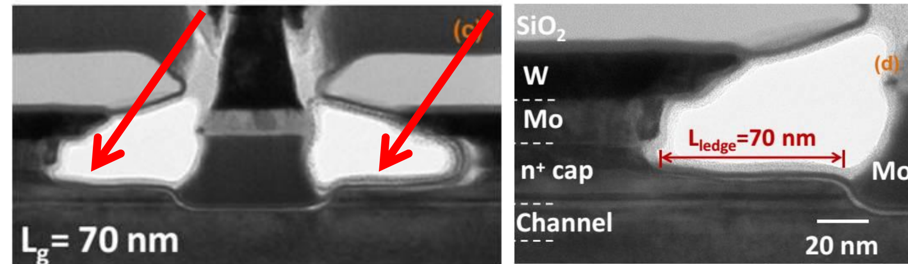
Lateral depletion region reduces severity of most short-channel effects (not VLSI-compatible)

Examples from literature: gate-drain lateral spacers

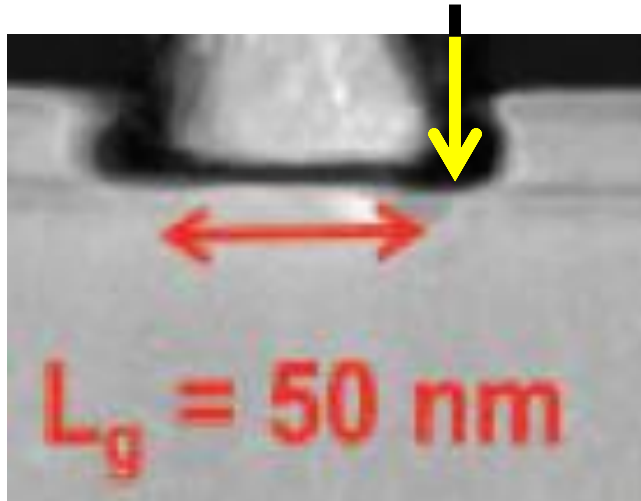
Chang *et al.*: IEDM 2013:
150nm gate-drain spacer



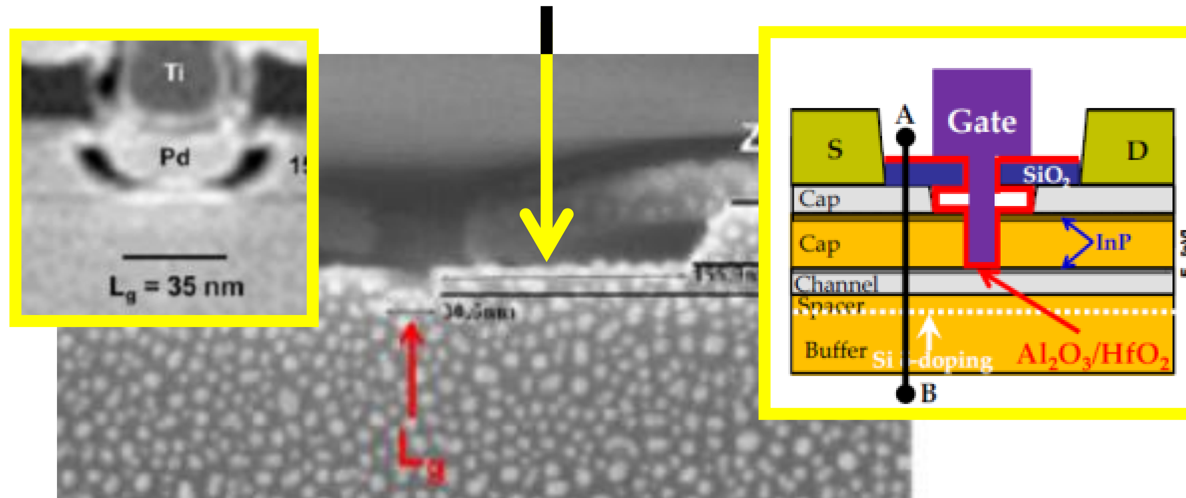
Lin *et al.* : IEDM 2013: 70nm S/G, G/D spacers



T. W. Kim *et al.*, IEDM2012
~16 nm S/G, G/D spacers

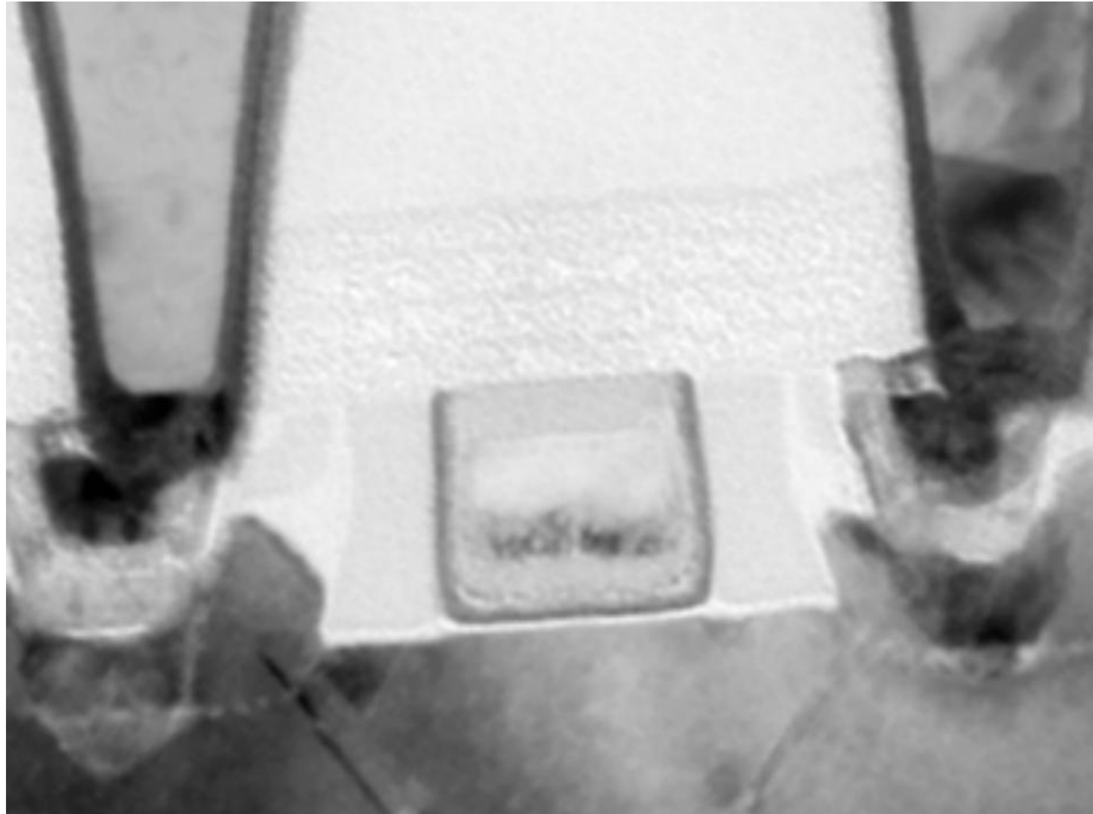


D. H. Kim *et al.*, IEDM2012
~100nm S/G, G/D spacers



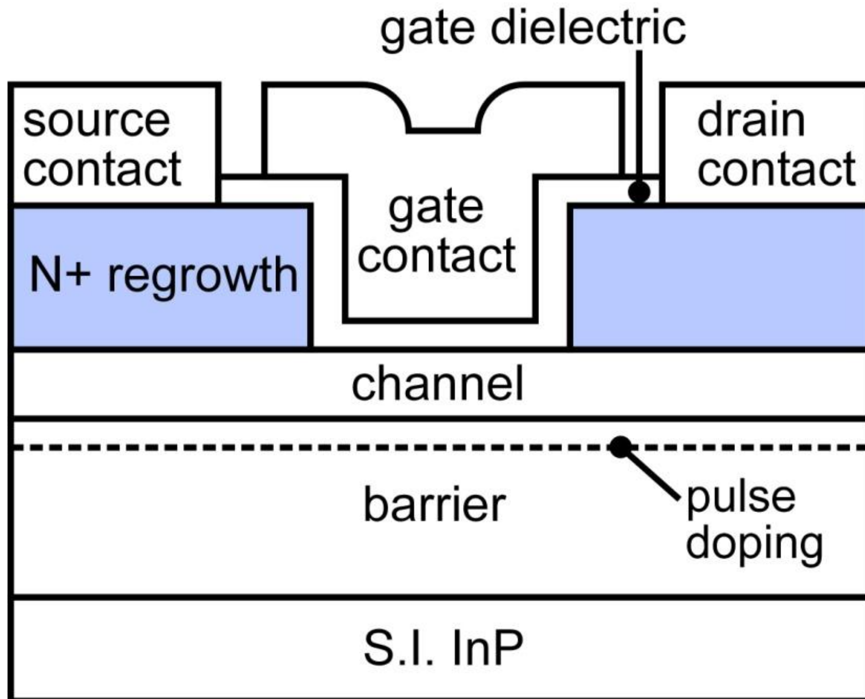
We must build devices with small S/D pitch.

contact pitch ~ 3 times lithographic half-pitch
(technology node dimension)

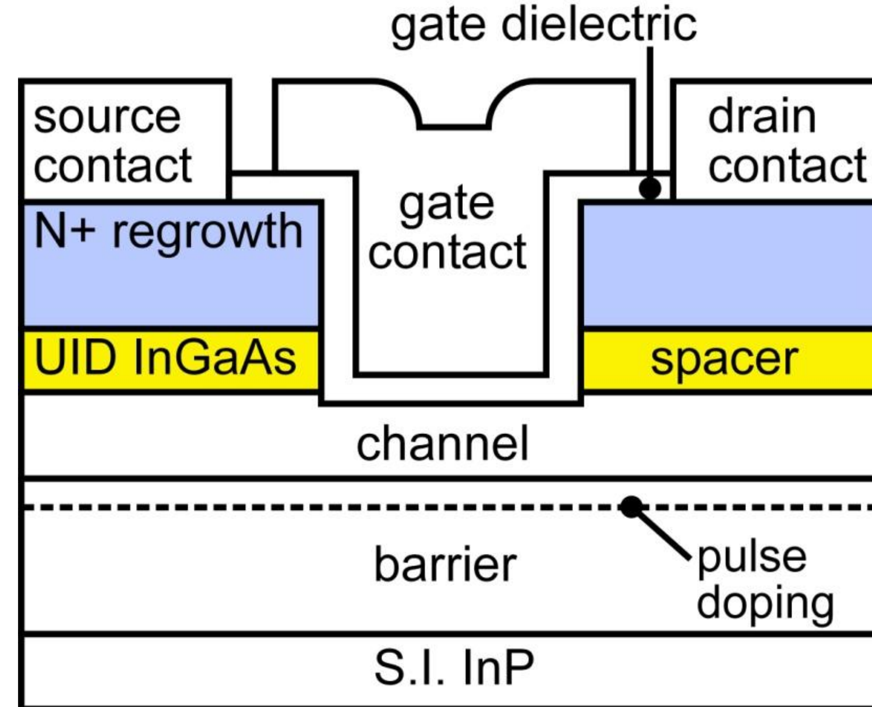


Small S/D pitch hard to realize if we require ~20-50nm lateral gate-drain spacers !

Vertical spacers: reduced leakage -- at small feasible S/D pitch

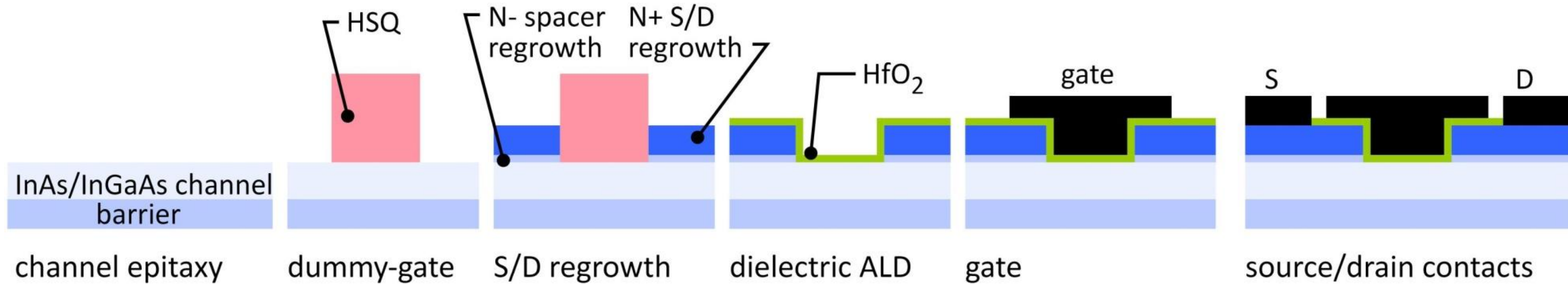


vs.

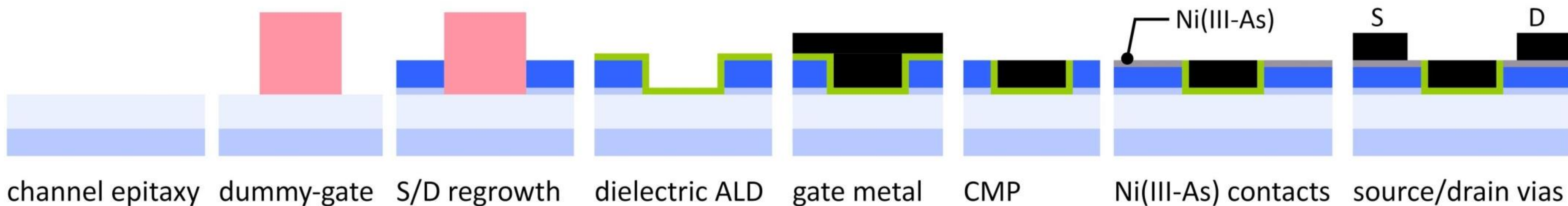


III-V MOSFET development process flow

Development process flow

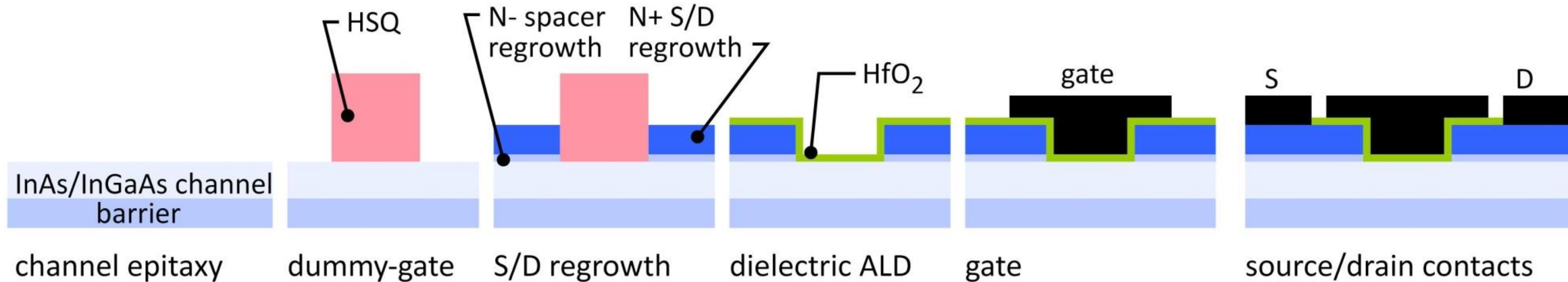


Manufacturing process flow



While our fast development process flow <u>does not provide</u> a small S/D contact pitch, in manufacturing, the vertical spacer <u>will provide</u> a small S/D contact pitch.

III-V MOSFET development process flow



Simple, 4-day, 16nm process→ learn quickly !

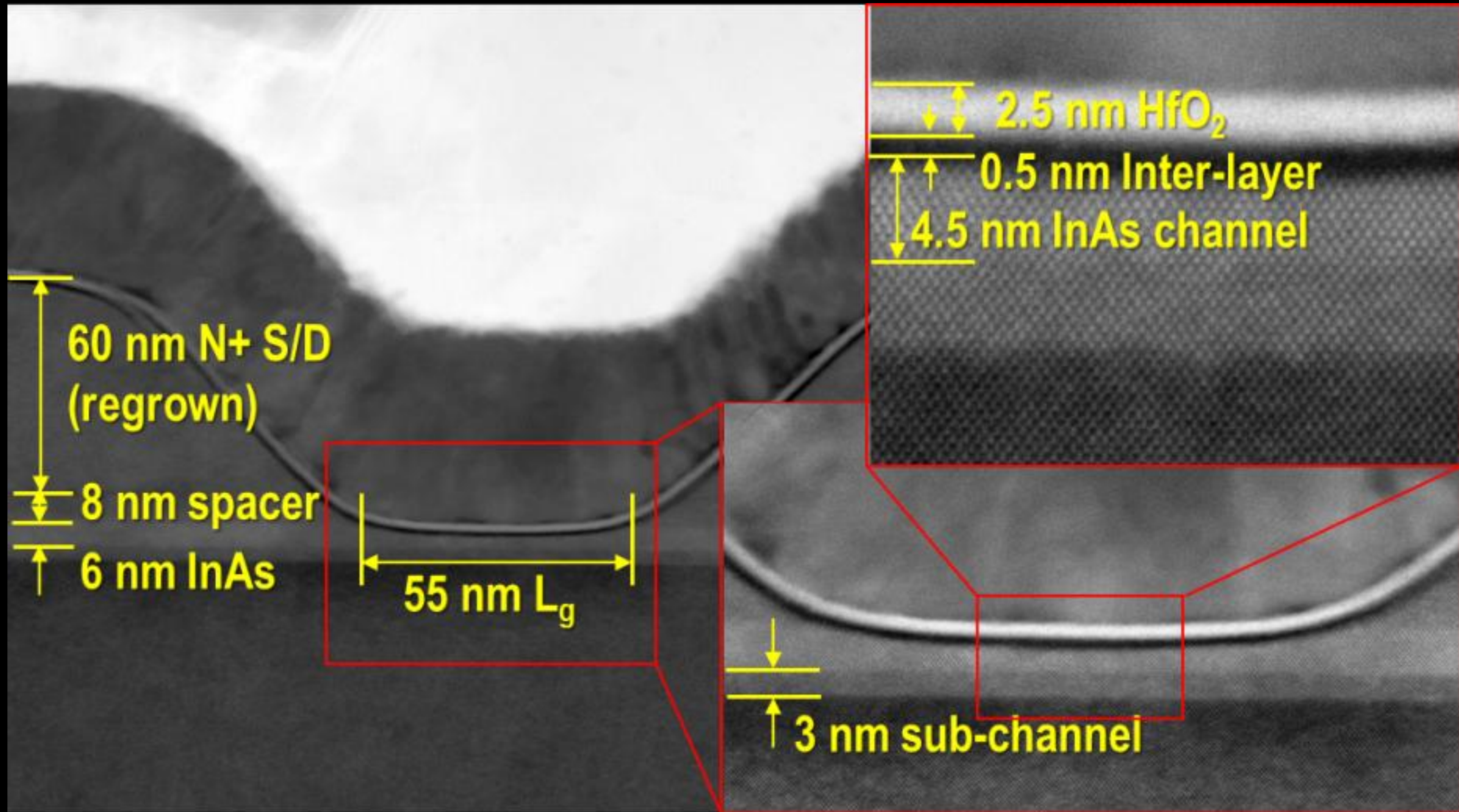
Low-damage: avoids confusing dielectric characterization.

Critical dimensions are scaled: L_g, channel thickness, (N+ S/D):G separations.

Process otherwise <u>not</u> scaled: large gate overlap, large S/D contact separations.
increases gate leakage, increases access resistance.

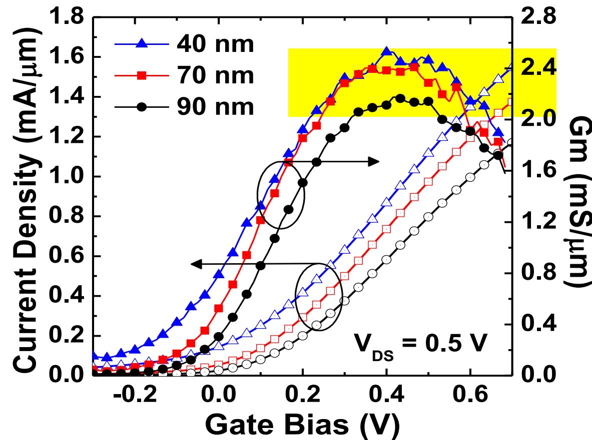
Process <u>is</u> <u>not</u> <u>now</u> self-aligned, but <u>could</u> <u>be</u> <u>made</u> self-aligned.

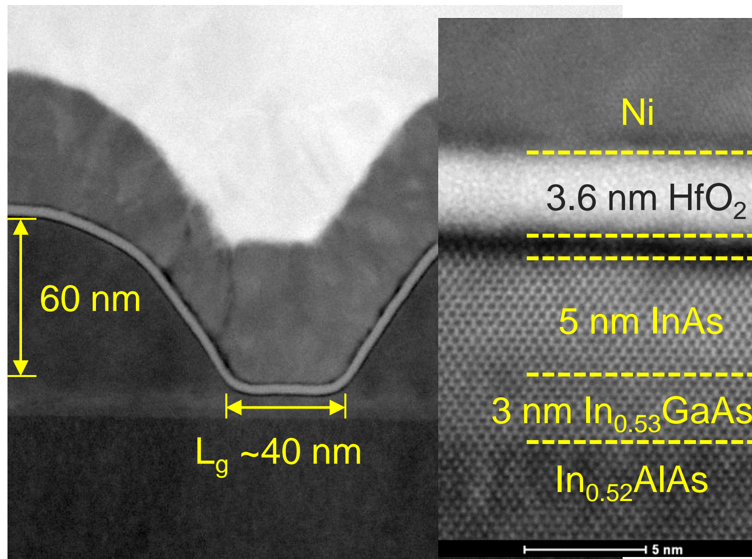
TEM Cross-Section, Summer 2013

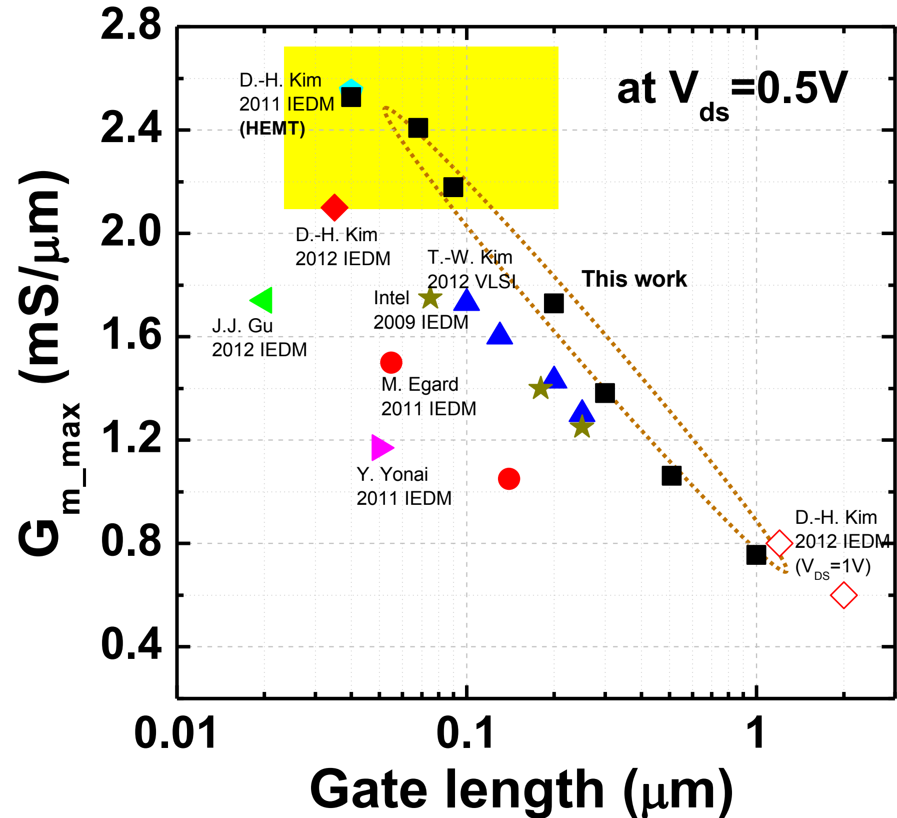


High Transconductance III-V MOSFETS: 2013 VLSI Meeting

Lee *et al*, 2013 VLSI Symposium, May





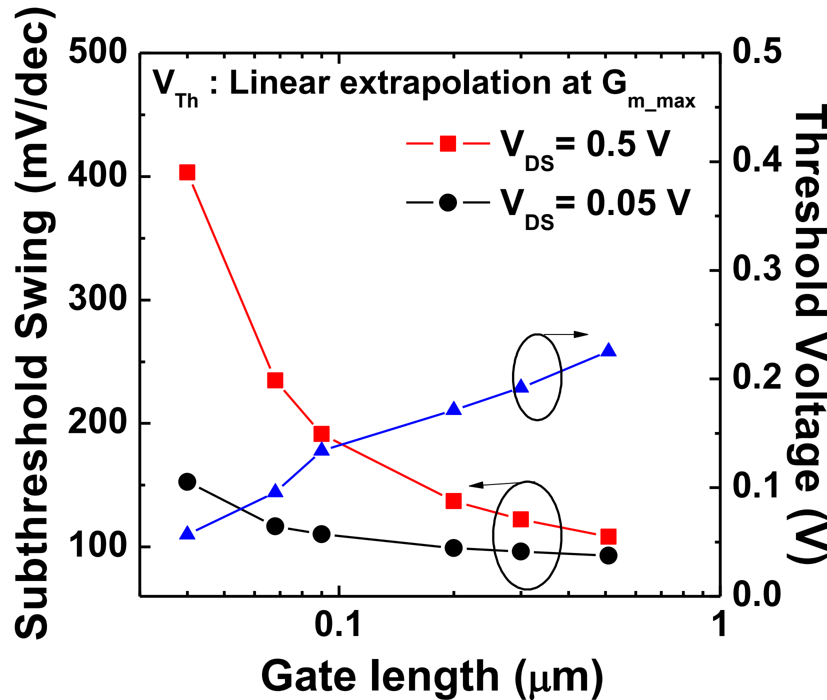


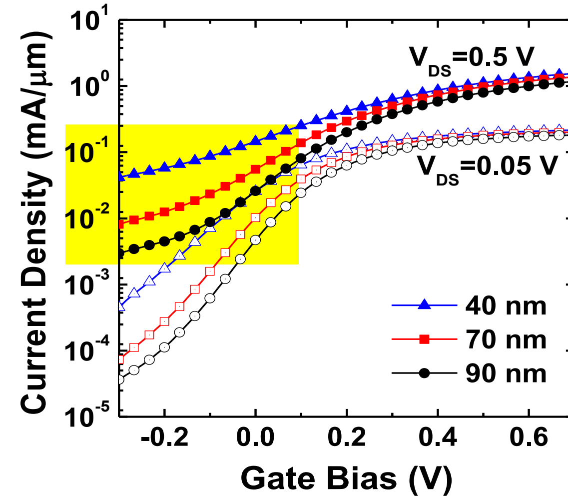
8 nm channel (5 nm/3 nm InAs/$In_{0.53}Ga_{0.47}As$) and ~4 nm HfO_2 high-k dielectric

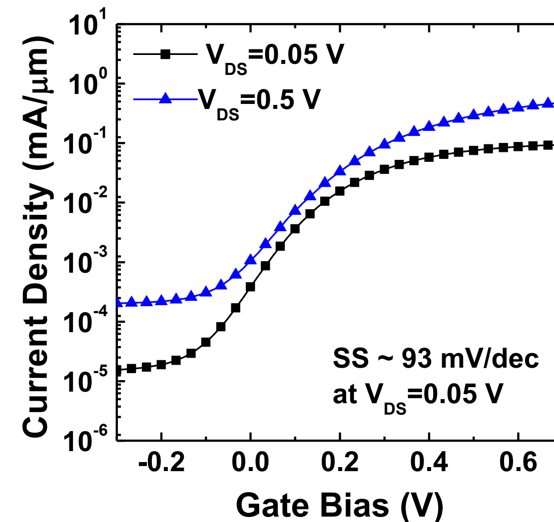
At time, record g_m over all gate lengths (i.e. 2.45 mS/μm at 0.5 V_{DS} for 40 nm-L_g)

High Transconductance III-V MOSFETS: 2013 VLSI Meeting

Lee *et al*, 2013 VLSI Symposium, May



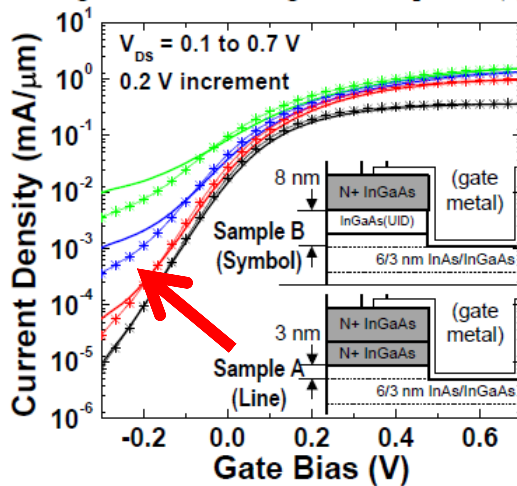


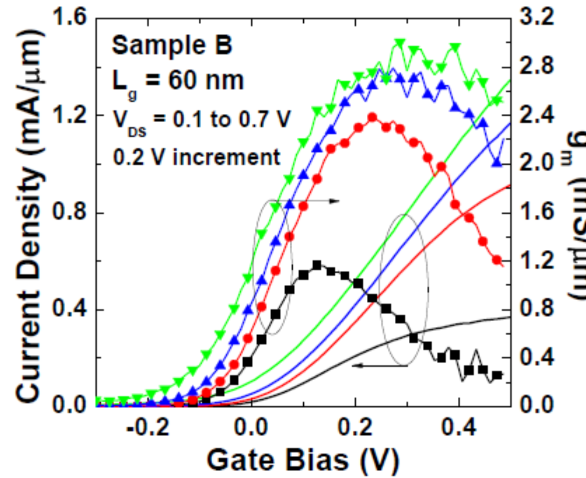


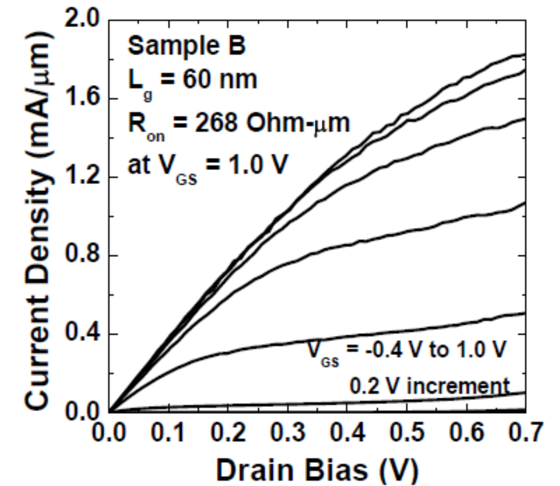
93 mV/dec @ 500 nm-L_g but > 400 mV/dec @ 40 nm-L_g.

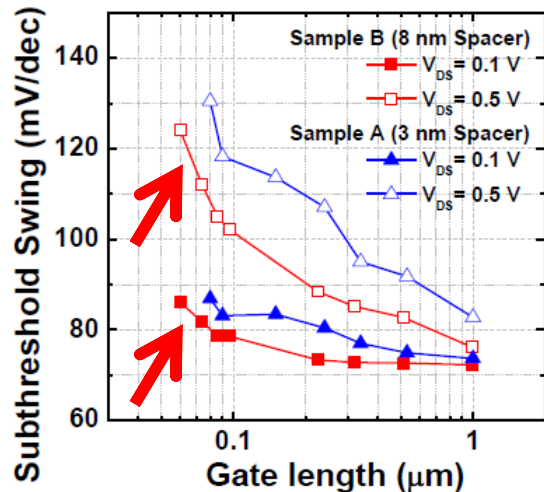
Extremely Poor Short-Channel Effects

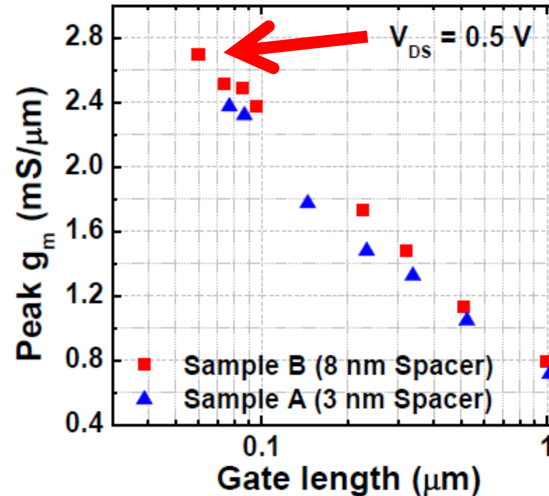
Reducing Leakage: 3nm vs. 8nm High-Field Spacer

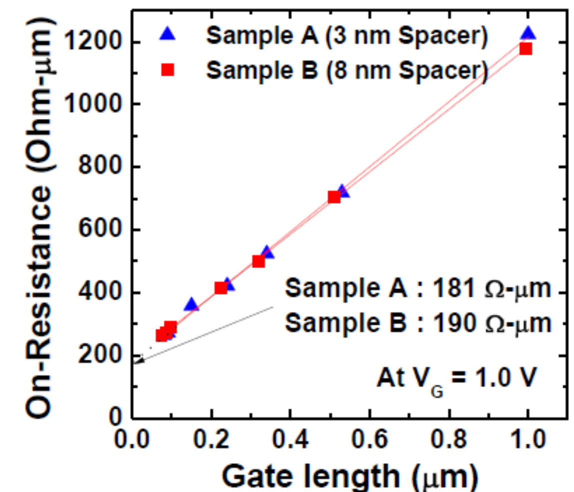








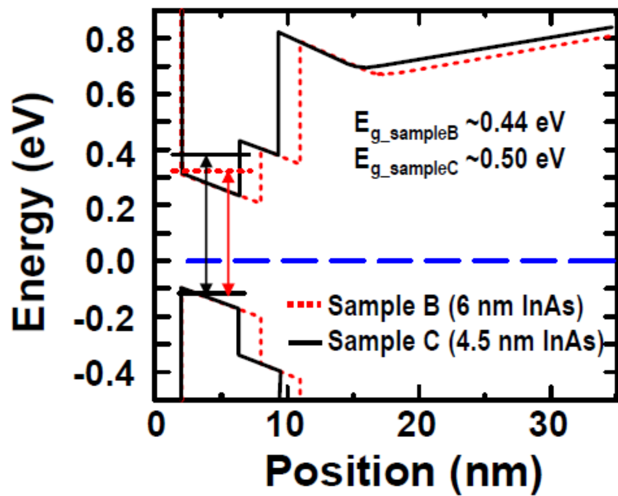


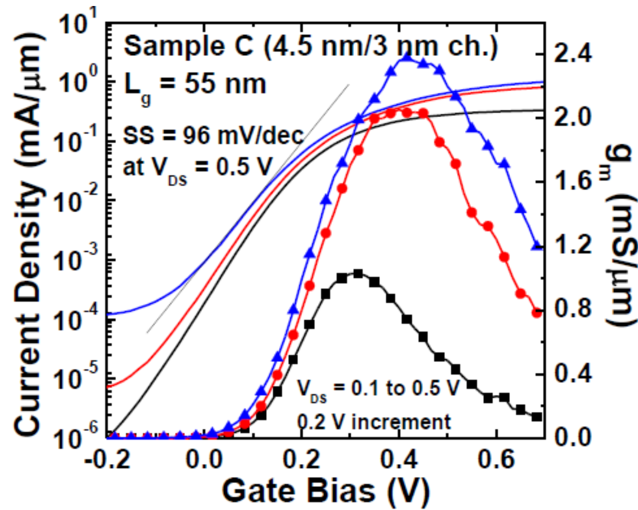


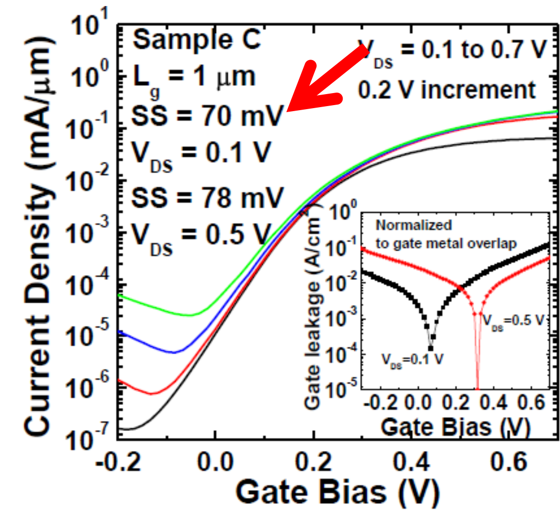
result

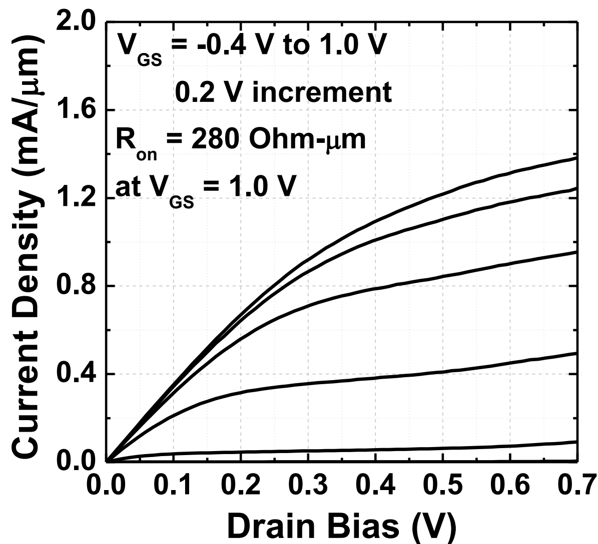
Reduced off-state leakage, improved short-channel effects, very high g_m & I_{on}.

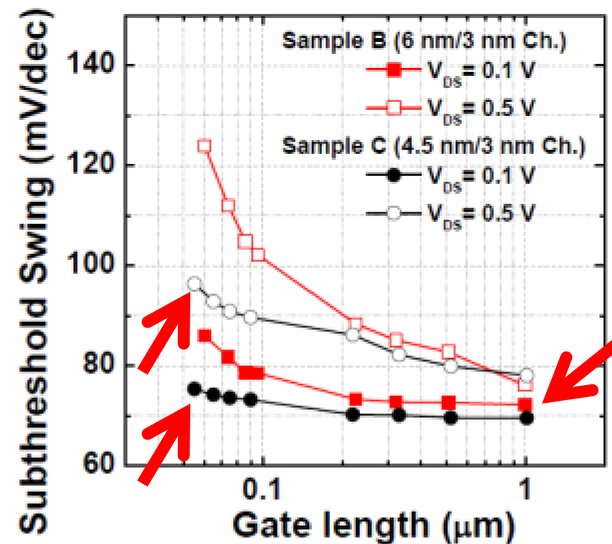
Reducing Leakage: 9nm vs. 7.5nm Channel Thickness

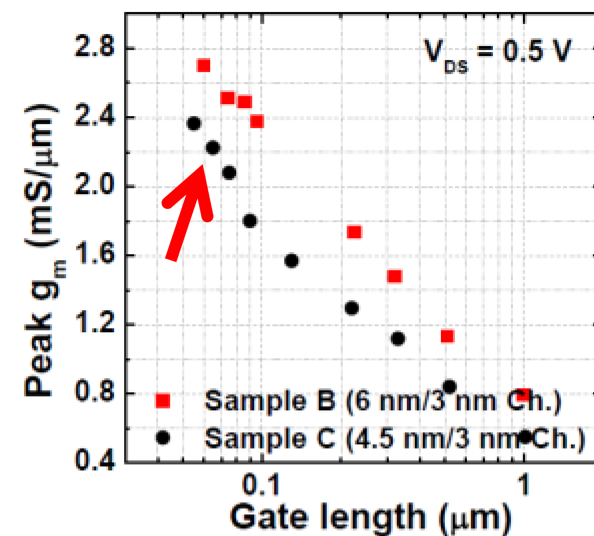








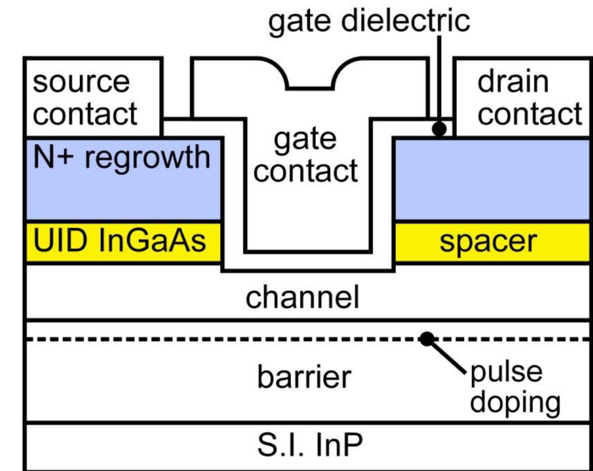




result

Better electrostatics, higher bandgap→ Reduced I_{off}, improved subthreshold swing, slightly less g_m & I_{on}.

Vertical spacers: some details



Minimum S/D contact pitch:
depends upon regrowth angle
we need to work on this.
[010] gate orientation should help

Spacer sidewalls are gated through the high-K.

Capacitance to UID sidewalls is negligible.
about 0.2 fF/μm
<< the ~1.0fF/μm interelectrode capacitances.

Capacitance to N+ contacts layers is large.
easy to eliminate: low-ε_r sidewall spacer.

Deliberate band offset between spacer & channel
compensates offset from strong quantization in channel.

Much Better Results to be Reported

To reduce off-state leakage:

thinner channels (quantization)→ less band-band tunneling

thinner channels & dielectrics → better electrostatics

To increase on-state current:

thinner channels & dielectrics

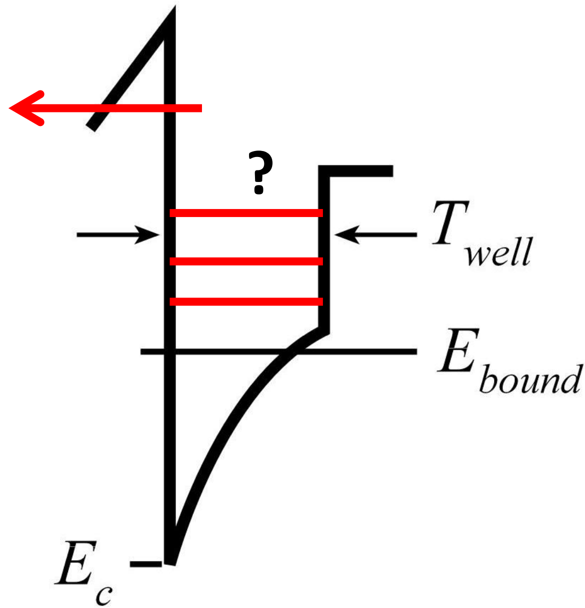
***Much* better results to be reported:**

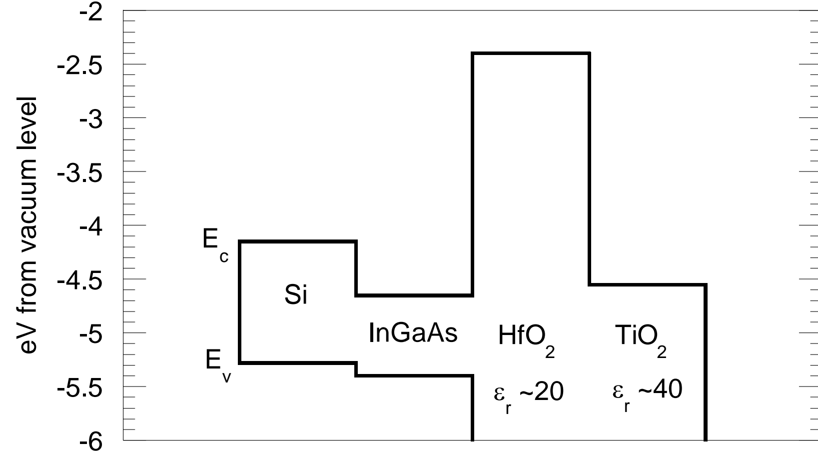
Lee et *al.*: EDL (in press)

Lee et *al.*: 2014 VLSI Symposium (June)

Thin Wells: Gate Leakage ?

In a thin InGaAs well, does the bound state energy rise to the point that dielectric leakage becomes high ?





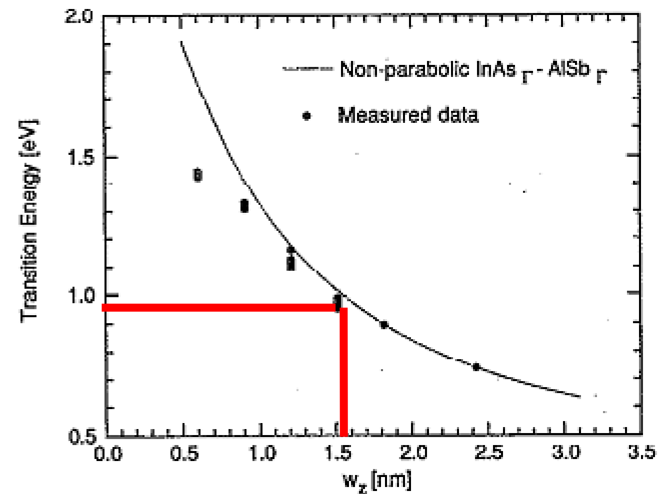


FIG. 3. Comparison between measured and calculated transition energies. The calculation assumes a spatially indirect transition.

1.5nm well: $(E_{bound}-E_c)$=0.5 eV

Brar data agrees well with:

1) Boykin, APL, 21 March 1994 (simulations)
2) Recent simulations by Povolotskyi (Purdue)
3) Recent unpublished UCSB FET data

Thermal Emission from Source over Back Barrier.

InGaAs-InAlAs barrier is 0.5 eV

Fermi level is 0.3~0.5 eV above conduction-band in the N+ source.

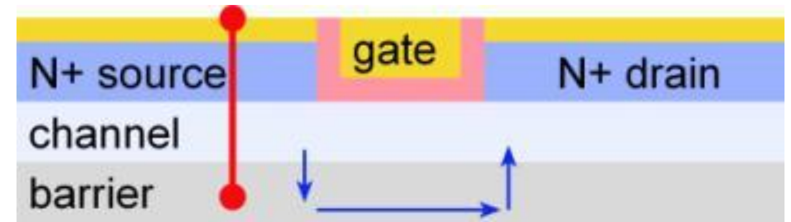
Barrier is only 0.1~0.25 eV above Fermi level.

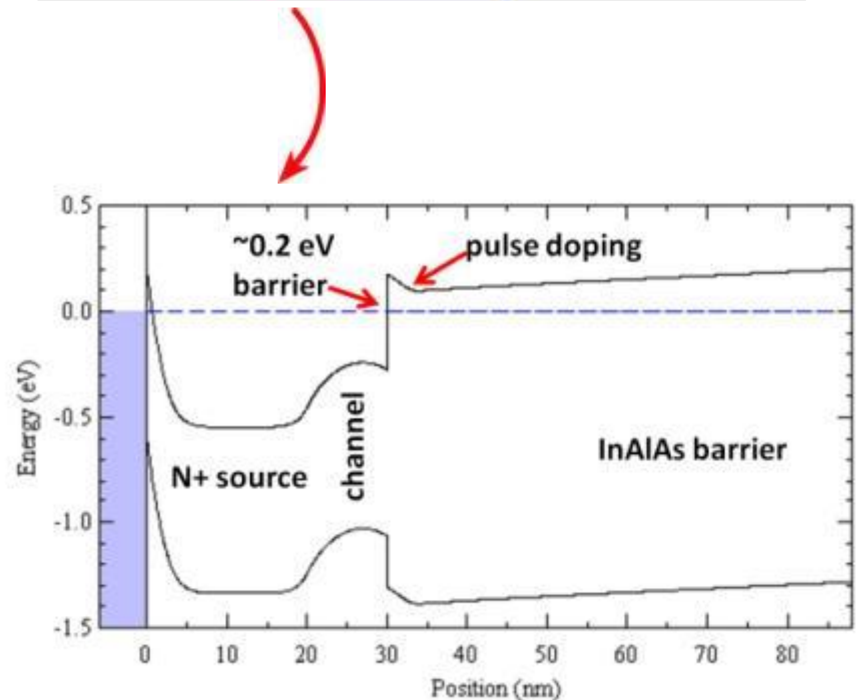
Thermionic emission flux:

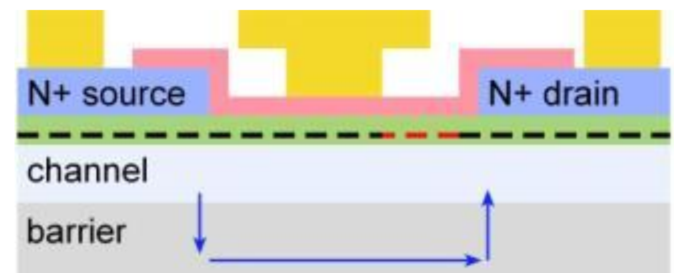
$$J_{thermionic} \approx q(kT/m^*)^{1/2} N_c \exp((E_f - E_c)/kT)$$
$$= 5\ \mu\text{A}/\mu\text{m}^2 \text{ for } 0.2\ \text{eV barrier.}$$

Need increased barrier energy.

Again, effect is less evident in MOS-HEMTs due to larger N+ S/D separation.



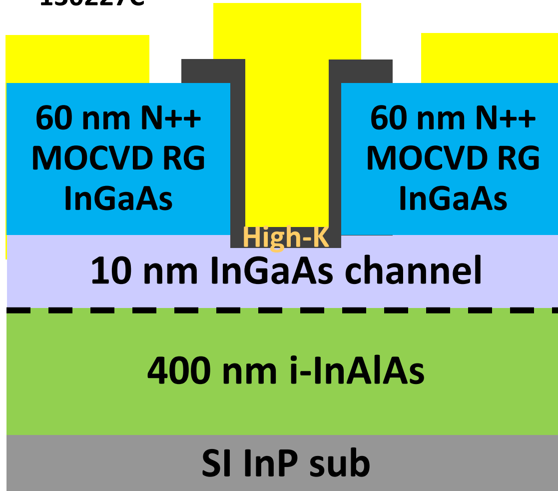




AlAsSb Back Barrier: Stops Barrier Thermal Leakage

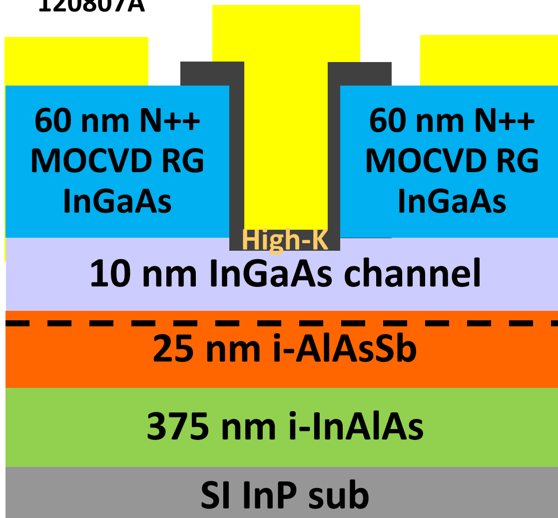
InAlAs back barrier

130227C



AlAsSb back barrier

120807A



AlAsSb layer:
0.5 eV increase in barrier.
Expect ~10^8:1 less thermal emission from source.

caution: as-draw gate length and gate widths stated. Data not yet corrected for either.

AlAsSb Back Barrier, P-doped layer, better isolation

InAlAs FET: 88 nm L_g, 25 micron drawn W_g, 8 nm InGaAs channel, 60 nm InGaAs Regrowth, 3.2 nm HfO_2, 0 deg

V_{DS} = 0.1 to 0.7 V
0.2 V increment
Current Density (mA/µm)
Gm (mS/µm)
Gate Bias (V)

V_{DS} = 0.1 to 0.7 V
0.2 V increment
SS ~ 135.9 mV at V_{DS}=0.5 V
SS ~ 99.9 mV at V_{DS}=0.1 V
Current Density (mA/µm)
Gate Bias (V)

V_{GS} = -0.2 V to 1.6 V
0.2 V increment
R_{on} = 344 Ohm-µm at V_{GS} = 1.6 V
Current Density (mA/µm)
Drain Bias (V)

AlAsSb FET: 90 nm L_g, 25 micron drawn W_g, 8 nm InGaAs channel, 60 nm InGaAs Regrowth, 3.2 nm HfO_2, 0 deg

V_{DS} = 0.1 to 0.7 V
0.2 V increment
Current Density (mA/µm)
Gm (mS/µm)
Gate Bias (V)

V_{DS} = 0.1 to 0.7 V
0.2 V increment
SS ~ 115.0 mV at V_{DS}=0.5 V
SS ~ 91.8 mV at V_{DS}=0.1 V
Current Density (mA/µm)
Gate Bias (V)

V_{GS} = -0.2 V to 1.6 V
0.2 V increment
R_{on} = 388 Ohm-µm at V_{GS} = 1.6 V
Current Density (mA/µm)
Drain Bias (V)

result

AlAsSb barrier shows lower off-state current and better SS as compared to P-InAlAs barrier.

III-V MOS: how small can we make Lg ?

Planar UTB FETs might just scale to 10nm L_g:

Unlike Si !

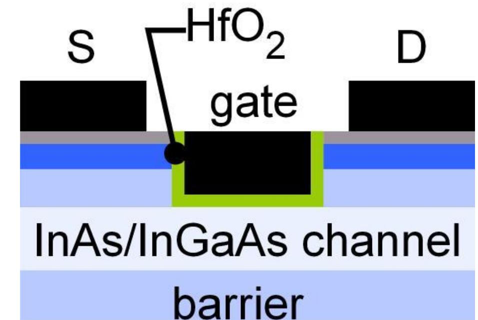
nm epitaxial control of channel thickness

high-energy barriers (AlAsSb)

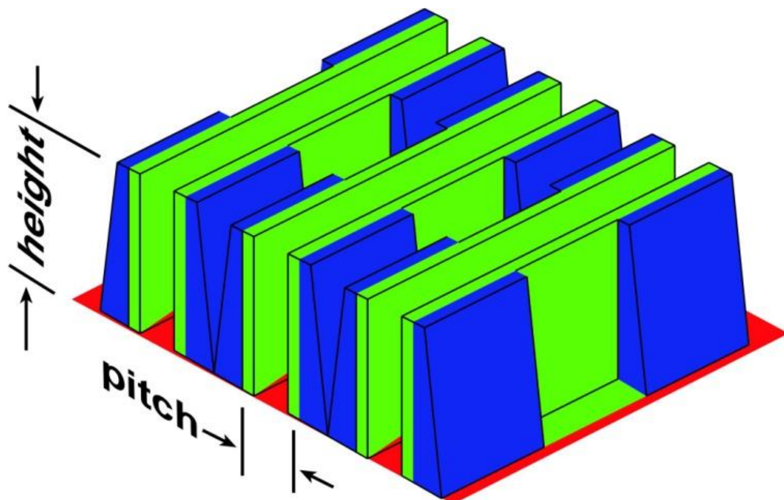
possibly thinner high-K than in Si.

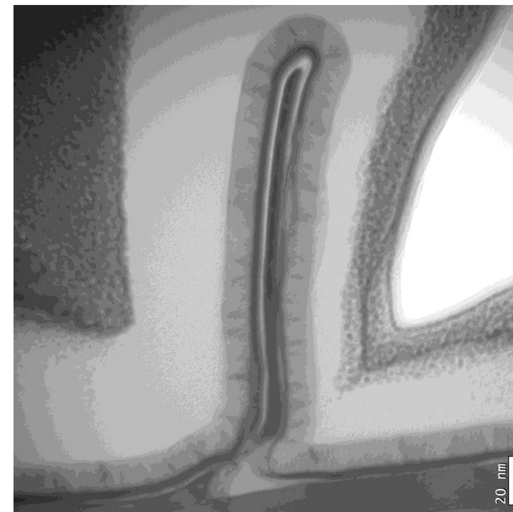
vertical spacer greatly aids short-channel effects

simulations suggest that, with spacers, even S/D tunneling is OK.



And with ALE techniques, few-nm L_g III-V **finFETs** are also feasible.





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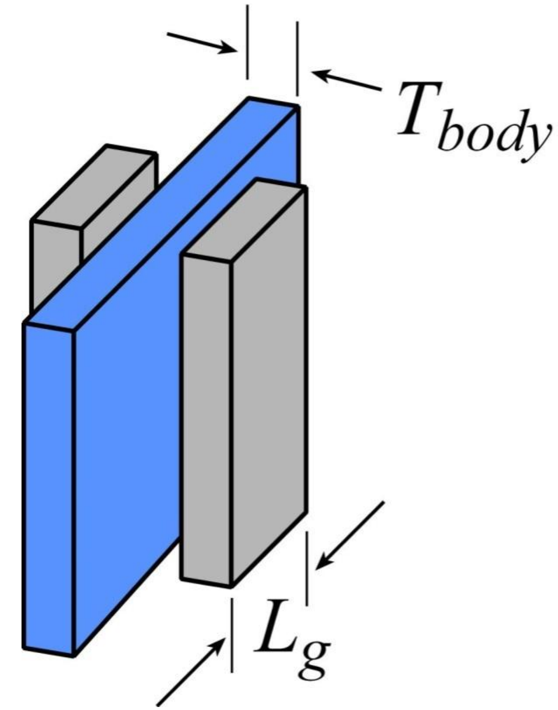
FinFETs by Atomic Layer Epitaxy: Why ?

***Electrostatics*:**
body must be thinner than ~L_g/2
→ less than 4 nm thick body for 8 nm L_g



***Problem*:**
threshold becomes sensitive to body thickness

$$\delta V_{th} \propto \delta T_{body} / T_{body}^3$$

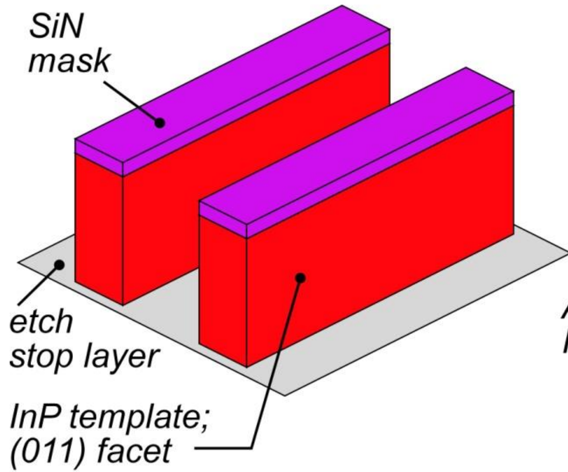
***Problem*:**
low mobility unless surfaces are very smooth

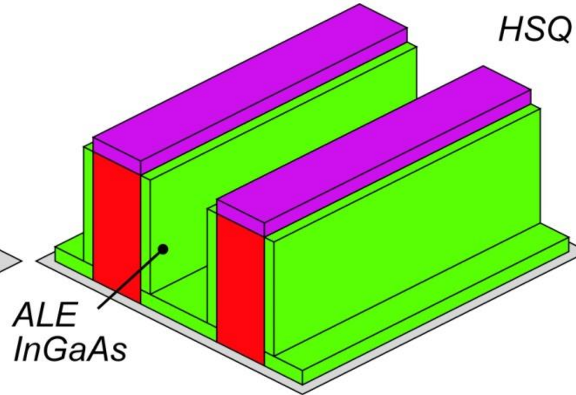
$$\mu \propto T_{body}^6 / \delta T_{body}^2$$

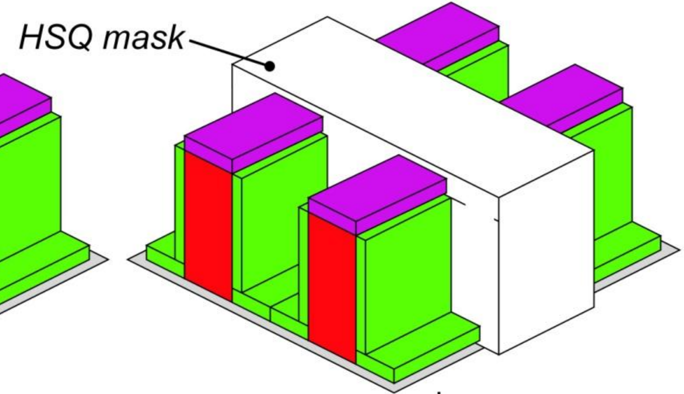
***Implication*: At sub-8-nm gate length, need :**
extremely smooth interfaces
extremely precise control of channel thickness

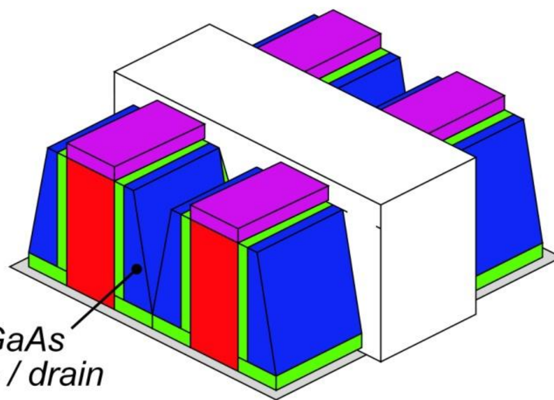
side benefit: high drive current→ low-voltage, low-power logic

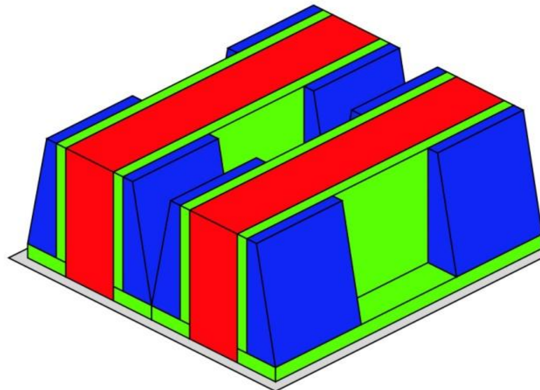
ALE-defined finFET

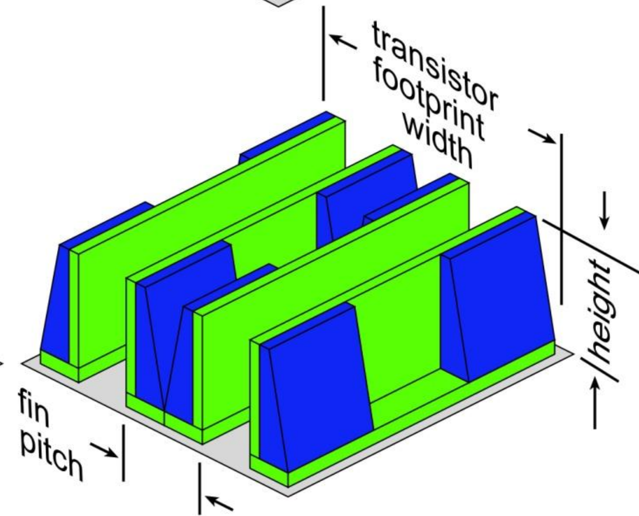










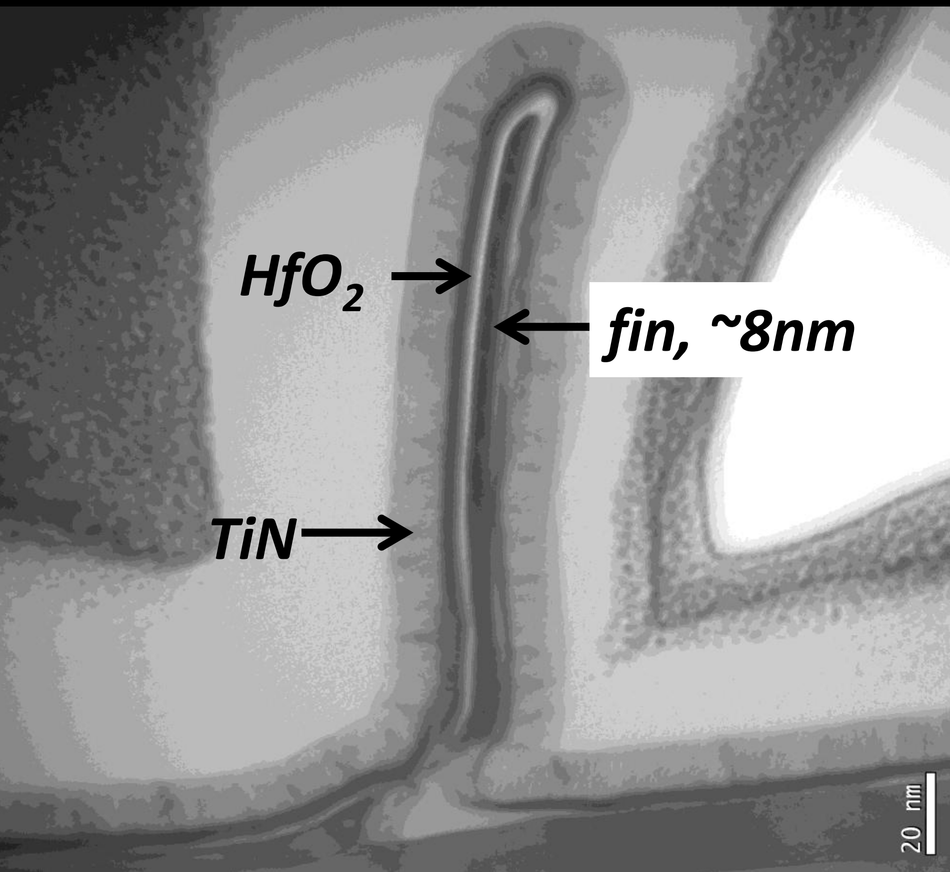


Fin template: formed by {110}-facet-selective etch→ atomically smooth

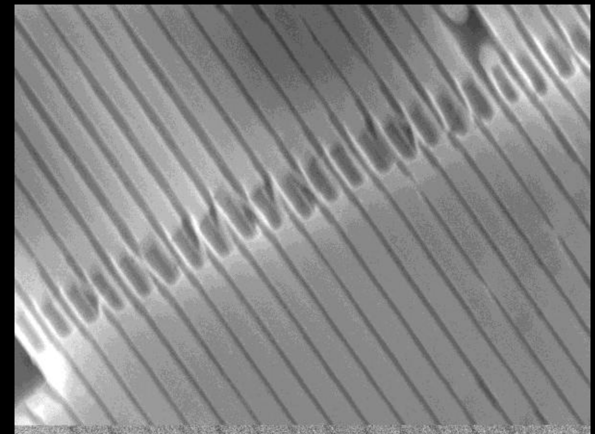
Channel thickness set by ALE growth→ atomically precise

Cohen-Elias *et al.*, DRC 2013

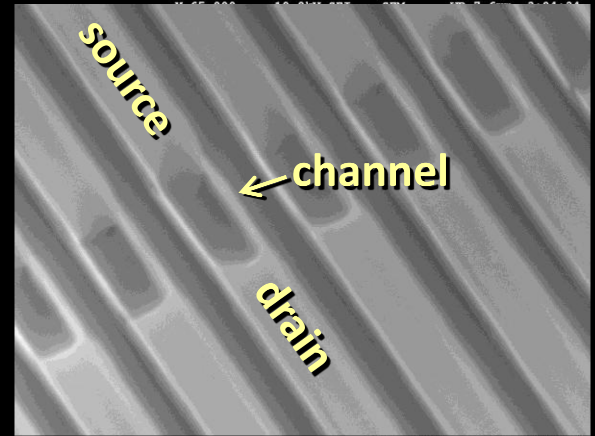
Images



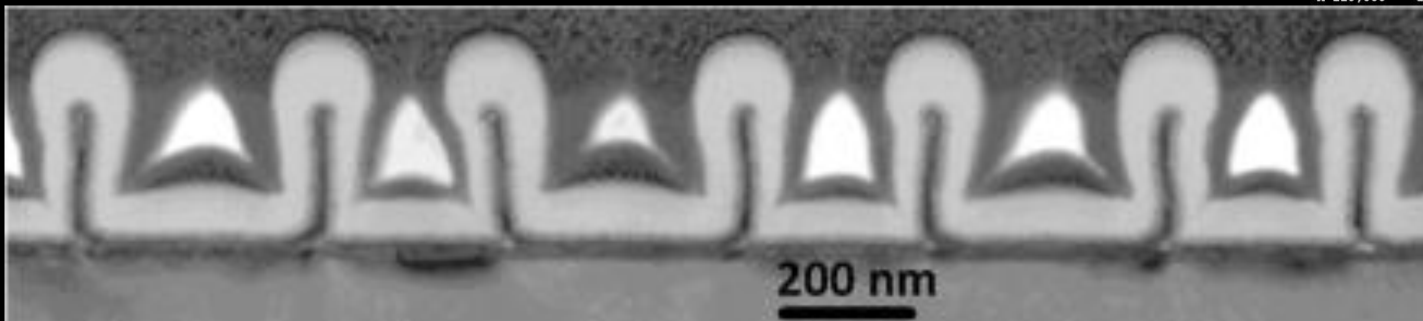
50 nm fin pitch



100 nm fin pitch



10 nm thick fins, 100 nm tall



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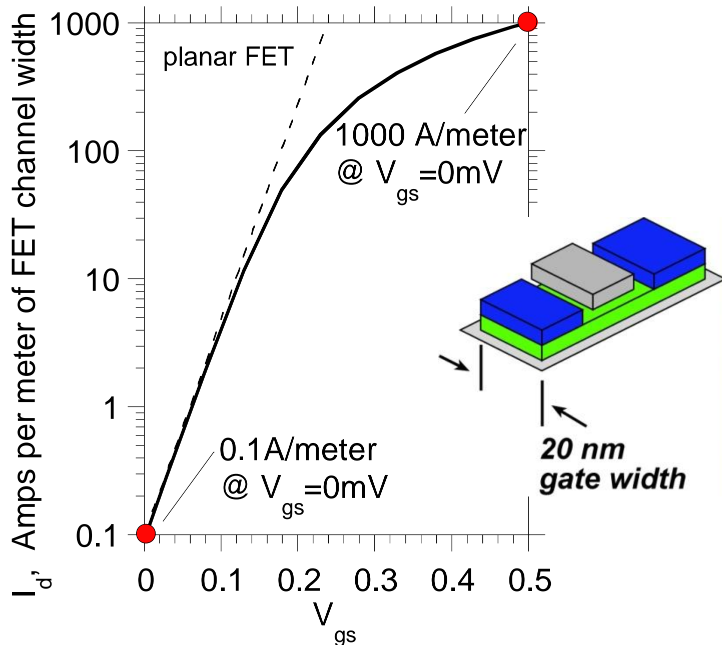
Tall Fins for Low-Power, Low-Voltage Logic

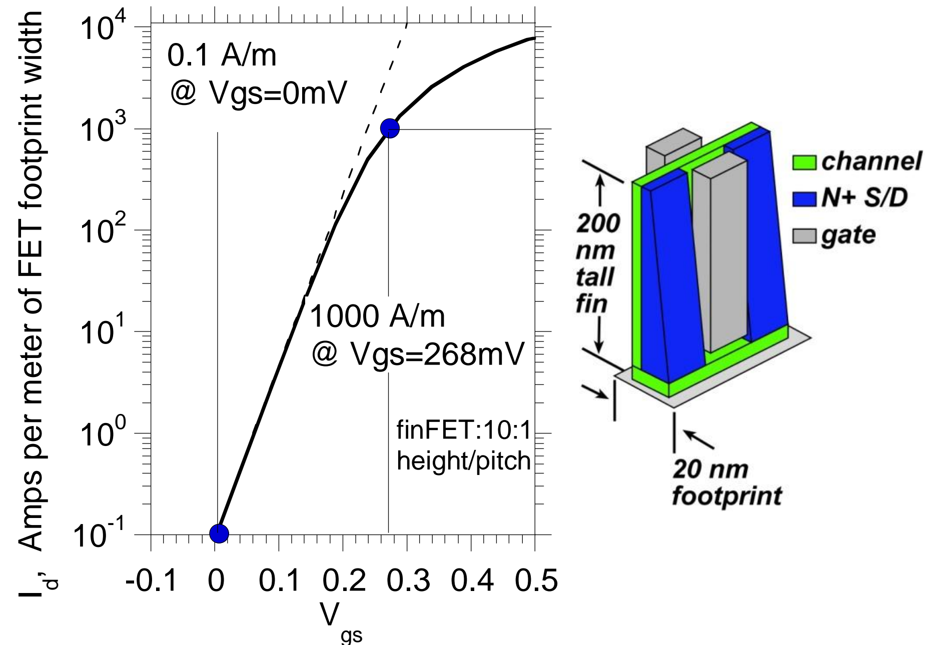
Low-voltage (near-V_T) operation:

low CV^2 dissipation, but low current→ long interconnect delays

Increased fin height→ increased current per unit die area

→ interconnect charging delays reduced





Supply reduced from 500mV to 268 mV while maintaining high speed.

3.5:1 power savings ? Circa 2.5:1 when FET capacitances considered.

What is next ?

In progress:

thinner dielectrics, better contacts, better alignment→ greater I_{on}

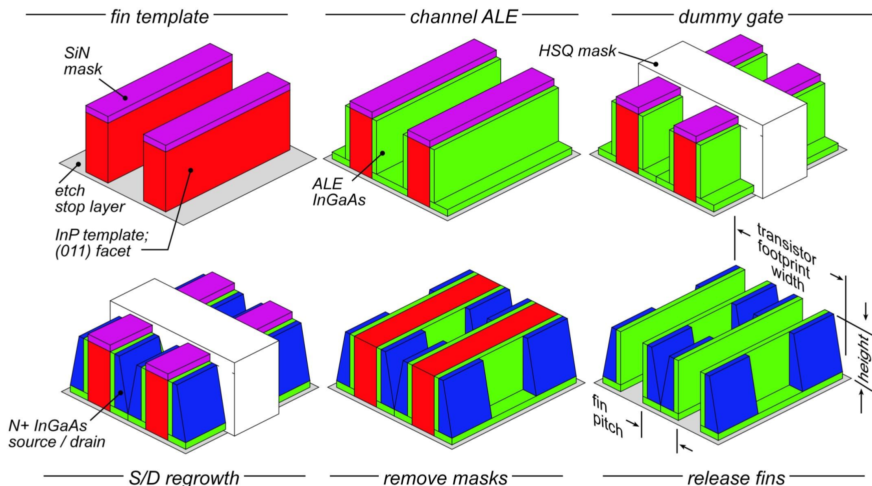
10nm L_g FETs: prove that spacer kills S/D tunneling leakage.

ultra-thin InGaAs & InAs channels low off-current

If we can:

InAs ALE-finFETs @ 10nm L_g→ high performance

110-oriented PMOS finFET→ performance approaching NMOS



(end)

Backup slides