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Record-Performance In(Ga)As Mosfets Targeting ITRS High-Performance and Low-Power Logic

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We review development of In(Ga)As-channel MOSFETs. InAs and InGaAs channels, combined with thin gate dielectrics, provide high transconductance, but off-state leakage can be high due to band-band tunneling currents. This leakage is reduced through thin 2.5-3nm channels, and through InGaAs or InP vertical field spacers in the raised source and drain. Devices with 2.7nm InAs channels and lightly-doped InGaAs source/drain spacers, at 25nm L_g, provide a record 0.5mA/µm I_{on} at 100nA/µm I_{off} and 500mV V_{DD}. 1 µm L_g FETs show 61mV/decade subthreshold swing at V_{DD}=0.1 V. Targeting the LP specification, we have developed InGaAs-channel MOSFETs with lightly-doped InP wide-bandgap source/drain spacer layers. At 30nm gate length, these show a minimum 60 pA/µm I_{off}, approximately 100:1 smaller than a similar device using InGaAs source/drain spacers. A FET using InP spacers, with 45 nm gate length, shows 0.15 mA/µm I_{on} at 1nA/µm I_{off} and 500mV V_{DD}.

InAs and InGaAs have been extensively studied for potential application in VLSI [1,2,3,4,5,6,7,8,9,10,11,12,13,14,15]. These materials have low electron effective mass, which provides a large carrier injection velocity. Together with the high carrier mobility, these devices provide the potential for increased on-current I_{on} relative to MOSFETs using Si channels. It should be noted as caveat that the advantage of III-V channels diminishes in the case of extremely thin gate dielectrics [16]. Yet, impact ionization, band-band tunneling, and source/drain (S/D) tunneling leakage currents can be high because of low bandgaps and low electron effective mass; until recently [14] I_{on} (at specified low I_{off} and V_{DD}), had not approached or surpassed Si.

If III-V MOSFETs are to supplant silicon MOSFETs in VLSI, their leakage currents will have to be greatly reduced, to levels varying from 100nA/µm for high-performance (HP) logic to 30pA/µm for low-power (LP) logic. Such low leakage currents must be obtained at device dimensions consistent with the next few scaling generations of VLSI; implying gate lengths approach 7-15nm and source/drain contact pitches approaching 20-

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40nm. Given such tight dimensions, reduction of this leakage through use of large lateral gate-drain spacers has little relevance to VLSI.

Here we describe device designs for low-leakage III-V MOSFETs. In addition to benefiting FET electrostatics, extreme thinning of the epitaxial In(Ga)As channel to 2-3nm increases the channel quantized bandgap, thereby also decreasing off-state leakage arising from BTBT. Inserting undoped vertical spacers within the raised regrown source/drain (S/D) reduces the otherwise extreme electric field in the gate-drain region, reducing band-to-band tunneling (BTBT) leakage currents. InP, with its wider bandgap, is less prone to BTBT, but, with its higher electron effective mass, its extensive use within the FET channel will decrease the transconductance and on-current; by judicious insertion of InP only in the regions of highest field, leakage can be greatly reduced while minimizing the sacrifice in on-current.

Figure 1 shows a schematic cross-section of a recent device, and Figure 2 a TEM cross-section of the channel. The FET has a 2.5-2.7nm thick InAs channel, a 1.0nm Al_2O_3 / 2.5nm ZrO_2 gate dielectric [9] and 12nm undoped InGaAs vertical spacers in the raised regrown S/D. Transconductance (Figure 3) is high because of low InAs effective mass and thin channel and dielectric; off-state leakage is moderately low (Figure 4) because of the vertical spacers and the strong quantization in the thin channel. Long-channel FETs show 61 mV/dec. subthreshold swing *S.S.* (Figure 6). For the 25nm L_g devices, on-current at 500mV V_{DD} and 100nA/µm I_{off} (Figure 7) is a record 0.5mA/µm, comparable to, or surpassing, leading Si fin- and nanowire FETs.

Because of residual BTBT at negative V_{gs}, off-current (Figure 4) in the FETs of Figure 1 meets the HP but not GP/LP/ULP ITRS requirements, with an off-state leakage floor of ~80nA/µm set by band-band tunneling. Replacing the narrow-bandgap InAs channel with InGaAs, and inserting (Figure 8) [15] raised-plus-recessed wide-bandgap InP S/D spacers, having a graded doping profile, the minimum off-current is reduced (Figure 9) to 300 pA/µm at V_{DS}=0.5V, this being limited by gate leakage. Increasing the ZrO_2 gate dielectric thickness from 3.0 to 3.8nm then reduces the minimum I_{off} to 60 pA/µm.

In these low-leakage devices, there is a moderate sacrifice in on-current, in part due to access resistance in the InP source spacer, and in part due to the due to the InGaAs channel. Present efforts seek to minimize the resistance associated with the source spacer, and to understand why the lower-leakage InGaAs channels provide smaller transconductance that InAs despite having similar transport effective mass.

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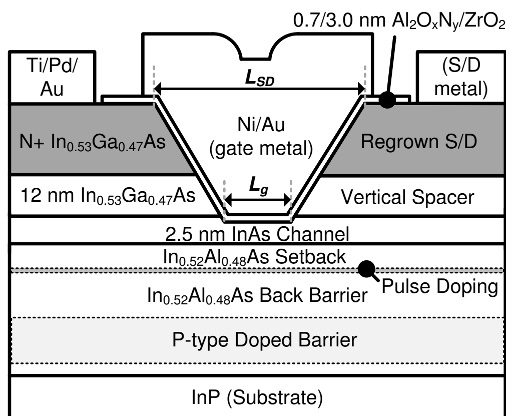

Figure 1: Schematic cross-section of III-V MOSFET with 2.5 nm InAs channel.

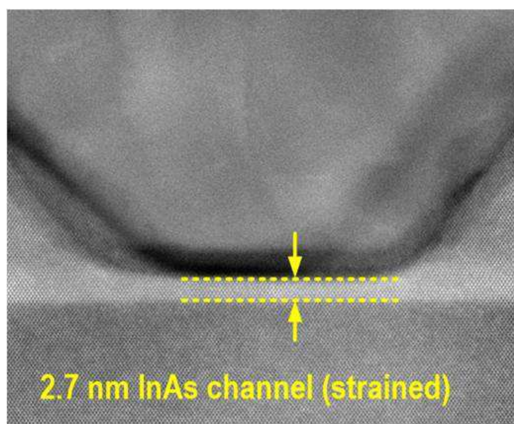

Figure 2: TEM cross-section of InAs MOSFET with 2.7nm InAs channel

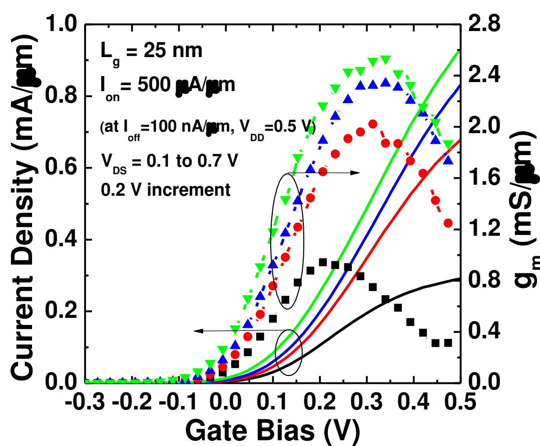

Figure 3: 2.7nm InAs channel FET: I_D and g_m, versus V_{GS}, at 25 nm L_g.

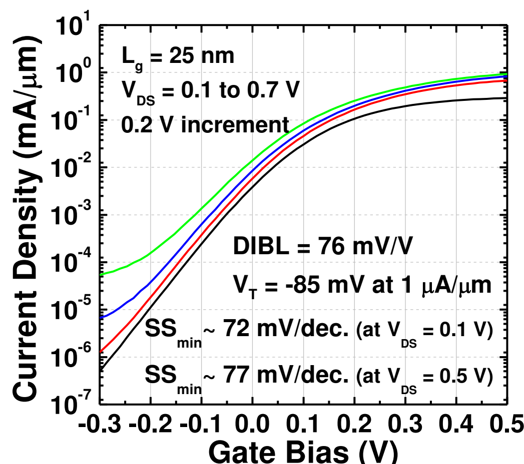

Figure 4: 2.7nm InAs channel FET: subthreshold characteristics at 25 nm L_g.

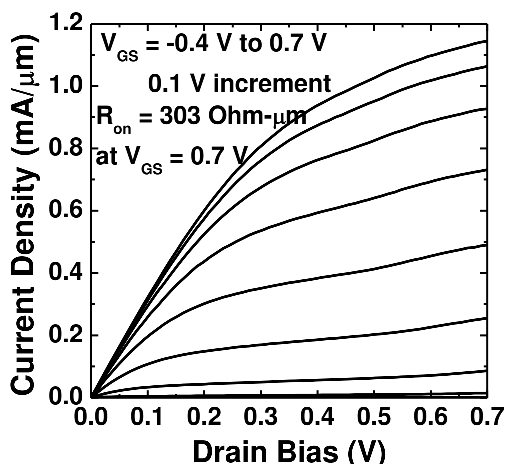

Figure 5: 2.7nm InAs channel FET: common-source DC characteristics at 25 nm L_g.

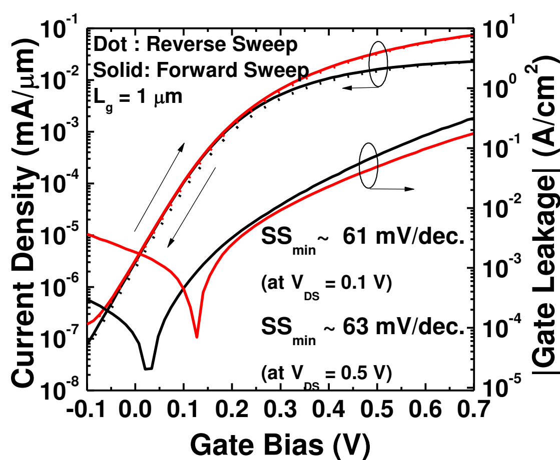

Figure 6: 2.7nm InAs channel FET: $\log(I_D)$ and $\log(I_G)$ versus V_{GS}, at 1μm L_g, at $V_{DS} = 0.1$ V and 0.5 V.

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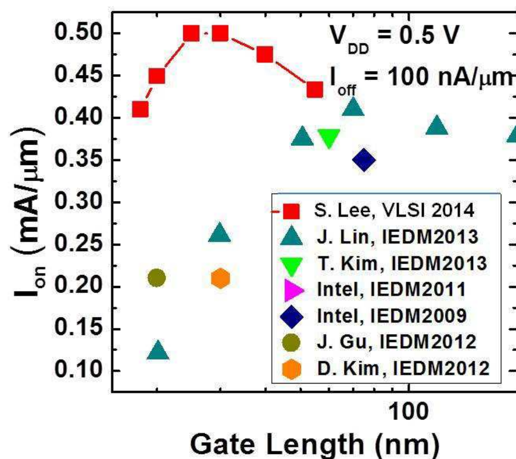


Figure 7: I_{on}, at 0.5V V_{DS} and 100nA/µm I_{off}, versus L_g, compared to the literature

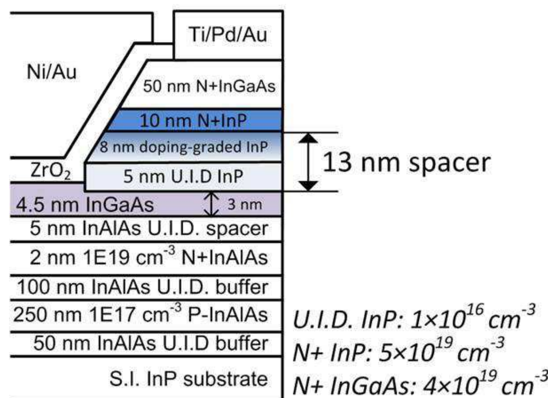
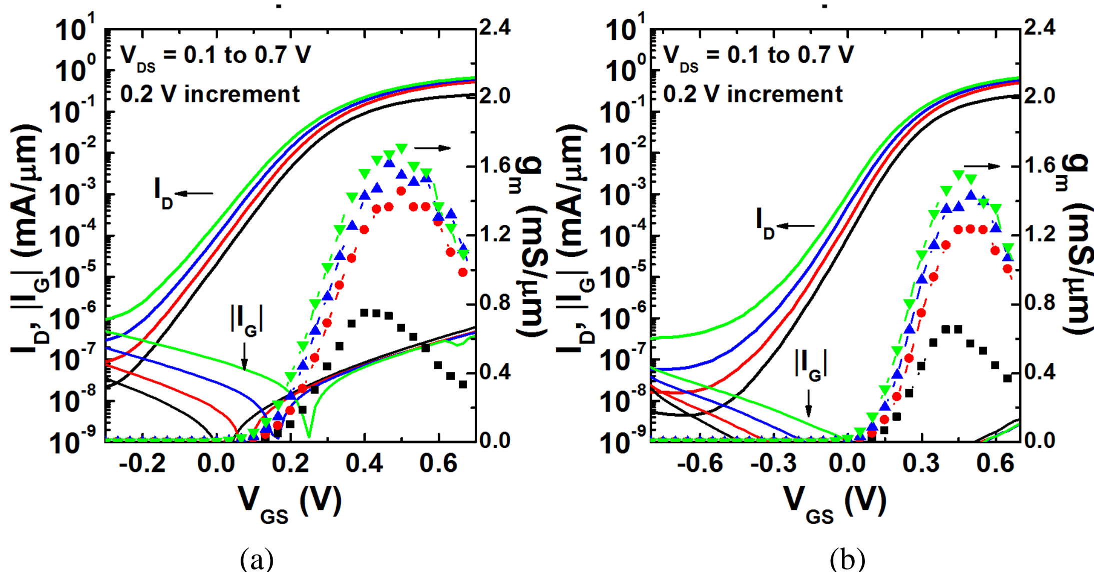


Figure 8: InGaAs MOSFET with recessed InP S/D field spacers, 13nm thick, in the raised source and drain.



(a) (b)

Figure 9: Subthreshold characteristics of the FET of Fig. 8 with (a) a 3.0nm thick ZrO_2 gate dielectric and (b) a 3.8nm thick ZrO_2 gate dielectric. The gate length of both devices is 30nm.

References

[1] J. Lin, X. Zhao, T. Yu, *et al.*, “A New self-aligned quantum-well MOSFET architecture fabricated by a scalable tight-pitch process” in Proc. IEEE IEDM, Dec. 2013, pp. 421-424.

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[2] S. W. Chang, R. Oxland, S.W Wang, et al., “InAs N-MOSFETs with record performance of I_{on} = 600 μA/μm at I_{off} = 100 nA/μm (V_d = 0.5 V),” in Proc. IEEE IEDM, Dec. 2013, pp. 417-420.
[3] D.-H. Kim, P. Hundal, A. Papavasiliou, et al., “E-mode planar L_g = 35 nm $In_{0.7}Ga_{0.3}As$ MOSFETs with $InP/Al_2O_3/HfO_2$ (EOT = 0.8 nm) composite insulator,” in Proc. IEEE IEDM, Dec. 2012, pp. 32-35.
[4] S. Lee, C.-Y. Huang, D. Elias, et al., “High performance raised source/drain InAs/ $In_{0.53}Ga_{0.47}As$ channel metal-oxide-semiconductor field-effect-transistors with reduced leakage using a vertical spacer,” Appl. Phys. Lett., vol. 103, no. 23, pp. 233503–233503, 2013.
[5] S. Kim, M. Yokoyama, R Nakane, et al., “High performance sub-20-nm-channel-length extremely-thin body InAs-on-insulator Tri-gate MOSFETs with high short channel effect immunity and V_t tunability,” in Proc. IEEE IEDM, Dec. 2013, pp. 429-432.
[6] M. Radosavljevic, et al., “Advanced high-K gate dielectric for high-performance short channel $In_{0.7}Ga_{0.3}As$ quantum well field effect transistors on silicon substrate for low power logic applications,” in Proc. IEEE IEDM, Dec. 2009, pp. 319–322.
[7] T.–W. Kim, D.-H. Kim, D. Koh, et al., “ETB-QW InAs MOSFET with scaled body for improved electrostatics,” in Proc. IEEE IEDM, Dec. 2012, pp. 776-779.
[8] D.-H. Kim, J.A. del Alamo, D.A. Antoniadis et al., "High-Performance III-V Devices for Future Logic Applications", 2014 IEDM, December, San Francisco.
[9] V. Chobpattana, J. Son, J. J. M. Law, et al., “Nitrogen-passivated dielectric/InGaAs interfaces with sub-nm equivalent oxide thickness and low interface trap densities,” Appl. Phys. Lett., vol. 102, 2013.
[10] T.-W. Kim, D.-H. Kim, D. H. Koh, et al., “Sub-100 nm InGaAs quantum-well (QW) tri-gate MOSFETs with Al_2O_3/HfO_2 (EOT < 1 nm) for low-power logic applications,” in Proc. IEEE IEDM, Dec. 2013, pp. 429-432.
[11] J. J. Gu, X. W. Wang, H. Wu, et al., “20-80nm channel Length InGaAs gate-all-around nanowire MOSFETs with EOT=1.2nm and lowest SS=63mV/dec,” in Proc. IEEE IEDM, Dec. 2012, pp. 636-639.
[12] M. Radosavljevic, G. Dewey, D. Basu, et al., “Electrostatics improvement in 3-D tri-gate over ultra-thin body planar InGaAs quantum well field effect transistors with High-K gate dielectric and scaled gate-to-drain/gate-to-source separation”, in Proc. IEEE IEDM, Dec. 2011, pp. 765–768.
[13] M. Egard, L. Ohlsson, M.B.M. Borg, et al., "High transconductance self-aligned gate-last surface channel $In_{0.53}Ga_{0.47}As$ MOSFET," in Proc. IEEE IEDM, Dec. 2011, pp. 304-307.
[14] S. Lee, V. Chobpattana, C.-Y. Huang, B.J. Thibeault, W. Mitchell, S. Stemmer, A.C. Gossard, M.J.W. Rodwell , "Record I_{on} (0.50 mA/μm at V_{DD}= 0.5 V and I_{off}= 100 nA/μm) 25 nm-gate-length ZrO_2/InAs/InAlAs MOSFETs", 2014 Symposium on VLSI Technology, June, Honolulu.
[15] C. Huang, S. Lee, V. Chobpattana, S. Stemmer, A. Gossard, B. Thibeault, W. Mitchell and M. Rodwell, "Low Power III-V InGaAs MOSFETs Featuring InP Recessed Source/Drain Spacers with I_{on}=120 μA/μm at I_{off}=1 nA/μm and VDS=0.5V", 2014 IEDM, December, San Francisco.

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[16] S. R. Mehrotra, M. Povolotskyi, D. Cohen Elias, T. Kubis, J.J.M. Law, M.J.W. Rodwell, G. Klimeck, "Simulation study of thin-body ballistic n-MOSFETs involving transport in mixed-L valleys", IEEE Electron Device Letters, Vol. 34, No. 9, pp. 1196-1198.

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