Nanometer InP Electron Devices for VLSI and THz Applications

M. J. W. Rodwell[1], S. Lee[1], C.-Y. Huang[1], D. Elias[1], V. Chobpattanna[2], J. Rode[1], H.-W. Chiang[1], P. Choudhary[1], R. Maurer[1], M. Urteaga[3], B. Brar[3], A.C. Gossard[2], S. Stemmer[2]

[1]ECE and [2]Materials Departments, University of California, Santa Barbara, USA, rodwell@ece.ucsb.edu

[3]Teledyne Scientific and Imaging, 1049 Camino Dos Rios, Thousand Oaks, CA, 91360, USA

While the growth of III-As and III-P semiconductors is well-established, and their transport properties well-understood, the performance of high-frequency and VLSI electron devices can still be substantially improved. Here we review design principles, experimental efforts, and intermediate results, in the development of nm and THz electron devices, including nm InAs/InGaAs planar MOSFETs and finFETs for VLSI, InGaAs/InP DHBTs for 0.1-1 THz wireless communications and imaging, and ~5nm InAs/InGaAs Schottky diodes for mid-IR mixing.

Electron device bandwidths are determined by depletion-layer transit times and by *RC* charging times arising from depletion-layer and interelectrode fringing capacitances, and bulk semiconductor, contact, and charge-control transport barrier resistances. References [1,2,3] give detailed MOSFET, HBT, and THz diode scaling laws; bandwidths are increased by reducing lithographic and epitaxial dimensions, by increasing access region doping, by increasing current densities over control barriers, by reducing the Ohmic contact resistivities, and (with FETs) by increasing gate dielectric capacitance densities. Beyond difficulties in the growth and fabrication of small structures, key challenges include extremely low-resistivity Ohmic contacts [4], and the operation of these at 0.01-0.1 A/μm^2, forcing use of refractory contact metals [4]. For FETs, gate dielectrics must be thin yet low-leakage [5], channels must be ~1-3nm thick, channel interfaces must be smooth, and channel thicknesses well-controlled. At high currents, transport is degenerate, *i.e*. is limited by available electron states, with 3-D contact resistivities ultimately varying as $\sim \hbar q^{-2} n^{-2/3}$ [4,6], FET currents varying as $J \sim q^{5/2}\hbar^{-2}(m^*)^{1/2}V^{3/2}$ [1,7], and diode and HBT current varying as $J \sim q^3\hbar^{-3}(m^*)^1V^2$ in 3-D [2,8], and as $I \sim q^2\hbar^{-1}(m^*)^0V^1$ in the limit of a few-nm-wide, 1-D quantum-confined junction.

We are investigating InAs/InGaAs MOSFETs for VLSI application. Here, low transport mass provides large transconductance, but low effective mass and low bandgap can cause high off-state leakage currents through impact ionization, band-band tunneling, and source/drain (S/D) tunneling. We have reduced such leakage using vertical InGaAs spacers in the raised regrown S/D [9,10] (fig. 1) and using thin InAs or InGaAs channels for increased channel bandgap. Very thin gate dielectrics [11], together with the thin channels, improve electrostatics and increase transconductance. Very recently submitted results [10], still under review, from devices having extreme scaling of the channel and dielectric thicknesses, show DC performance comparable to, and possibly exceeding, that of production 22nm Si *finFETs* [12]. We have not yet determined whether the vertical spacers can adequately suppress S/D tunneling at 8-10nm L_g. At short gate lengths, finFETs suppress short-channel effects even with ~2:1 thicker channels and dielectrics than in a planar FET. Using sidewall ALE growth [13] few-nm-thick InGaAs finFETs (fig. 4,5) can be formed; the high aspect ratio may allow reduced-voltage operation [14].

THz InP HBTs [2] are being developed for 0.1-1THz wireless communications and radar [15]. HBT f_{max} exceeds 1.1 THz [16] at the 130nm node, and 600GHz ICs [17] have been demonstrated. At the 32nm (~2.2THz target f_{max}) node, high-current-density, low penetration depth, <1 Ω–μm^2 resistivity emitter and base contacts are the key challenges. Fig. 6 shows an HBT with a ~1nm Pt/5nm Ru controlled-penetration-depth 0.8 Ω–μm^2 resistivity base contact. Targeting the 64nm and 32nm nodes, we are developing (fig. 7) refractory TiN and TiW emitter via/contacts using ALD. Using similar processes, we are developing ~5nm diameter Ru/TiN Schottky contacts to InAs/InGaAs. We calculate that these diodes will operate in the 1-D quantum transport limit, will have ~50THz transit and RC cutoff frequencies, perhaps sufficient for even 30THz operation.

Work done in the UCSB Nanofabrication Facility, part of the NSF-funded NNIN network, and in the MRL Central Facilities supported by the MRSEC Program of the NSF under Award MR05-20415.

References: [1] M. Rodwell *et. al.*,. IEEE DRC, 2010 [2] M. Rodwell *et. al.*, Proc. IEEE, Feb. 2008, [3] M. Rodwell *et. al.*, IEEE Trans. MTT, July 1991, [4] A. Baraskar *et. al.*, J. Appl. Phys., 114, (2013), [5] V. Chobpattana *et al.*, J. Appl. Phys., 114, (2013), [6] A. Baraskar *et. al.*, IEEE IPRM., 2012 [7] K. Natori, J. Appl. Phys., vol. 76, no. 8, (1994), [8] V. Jain, M. J. W. Rodwell, IEEE EDL, Aug. 2011, [9] S. Lee *et al.,* APL, vol.103, p.233503 (2013) [10] S. Lee *et al.,* VLSI symposium, submitted (2014), [11] V. Chobpattana *et al.*, APL submitted (2014), [12] C.H. Jan *et al.*, IEDM 2012, [13] D. Elias *et al*., 2013 IEEE DRC [14] M. Rodwell, D. Elias, 3rd Berkeley Symp. Energy Efficient Electronic Systems, 2013, [15] M. Rodwell, 2013 IEEE APMC, [16] M. Urteaga *et. al.*,. IEEE DRC, 2011 [17] M. Seo *et. al.*,. IEEE IMS, 2013.

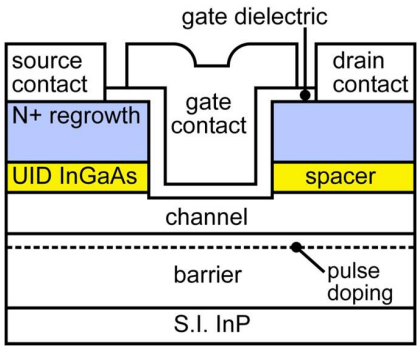

Fig. 1: III-V MOSFET showing a thin In(Ga)As channel and dielectric, and InGaAs vertical spacers for reduced I_{off}.

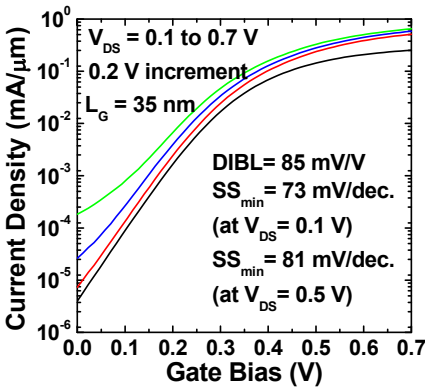

Fig.2: MOSFET log(I_D) versus V_{GS}, at 35 nm L_g, of a device with a 5nm thick InGaAs-channel and 3nm HfO_2 dielectric.

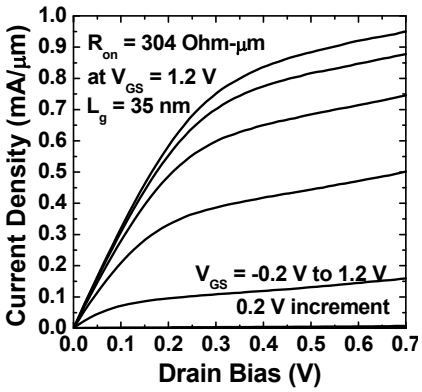

Fig. 3: MOS common-source DC curves at 35 nm L_g, of a device with a 5nm thick InGaAs-channel and 3nm HfO_2 dielectric.

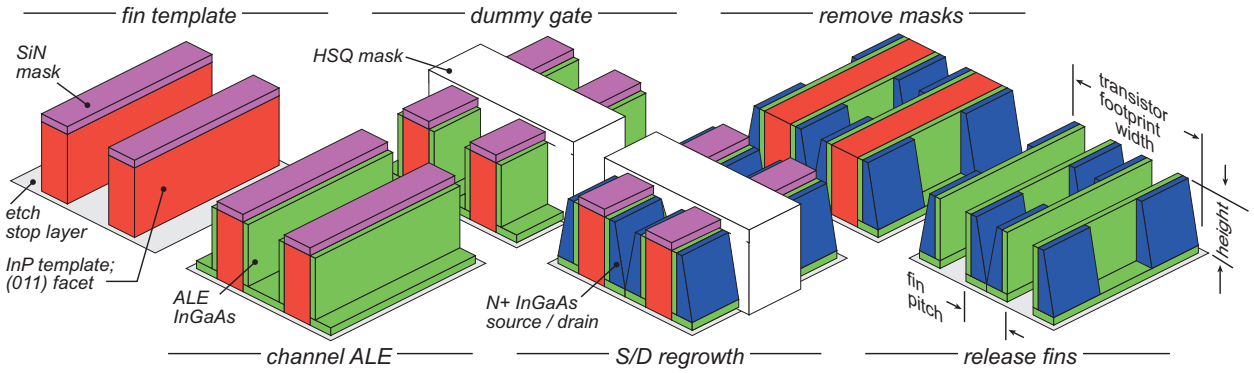

Fig. 4: Process flow for high aspect ratio finFETs. The InP template is defined by an wet etch selective to the vertical (011) facet. ALE growth can provide ~1nm control of the channel thickness. Not shown: ALD gate dielectric, gate & S/D metals.

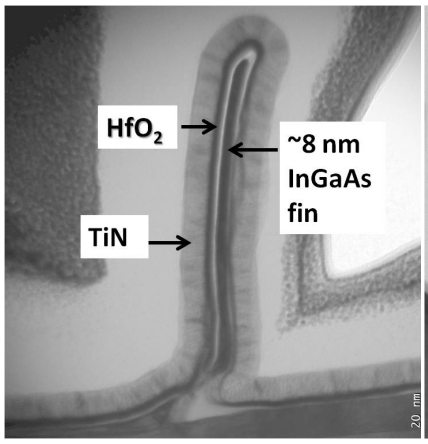

Fig. 5: High aspect ratio InGaAs finFET channel, formed by atomic layer epitaxy, with ALD HfO_2 gate dielectric and ALD TiN gate metal. The fin has 8nm width and ~180nm height.

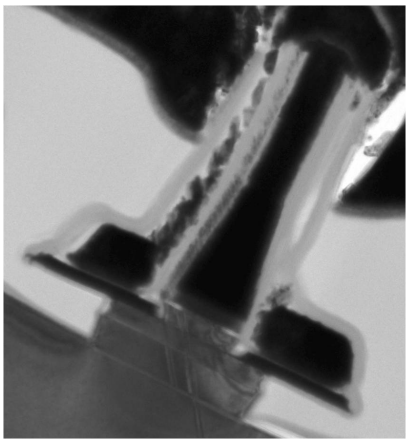

Fig. 6: 130nm InP DHBT with 1nm Ti/5nm Ru base and Mo emitter contacts. Process complications limited this device to only 800-GHz f_{max}; the design target is ~1.2 THz.

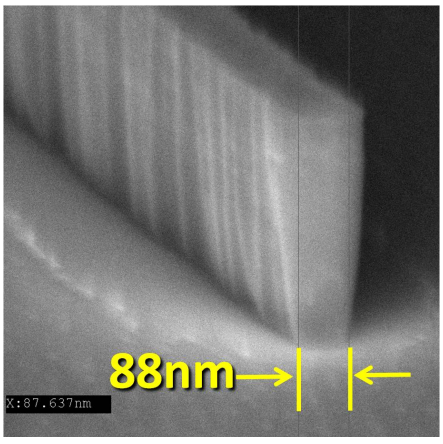

Fig. 7: Refractory TiN HBT emitter contact via/post formed by ALD deposition into a dry-etched Si mask. Such high-current refractory contacts can be scaled to < 64nm, serving future THz HBT scaling nodes.