35 nm-L_g Raised S/D $In_{0.53}Ga_{0.47}As$ Quantum-well MOSFETs with 81 mV/decade Subthreshold Swing at V_{DS}=0.5 V

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Recently, InAs or In-rich InGaAs (In>53%) has been widely studied as the channel material for III-V FETs due to its superior electron transport properties over $In_{0.53}Ga_{0.47}As$. These materials provide excellent on-state characteristics, e.g. >2.5 mS/μm peak transconductanc (g_m) at V_{DS}=0.5 V [1-3]. The narrow bandgap in these materials, however, causes band-to-band tunneling (BTBT) in the high drain-field region even at relatively low supply voltage of 0.5 V, thus resulting in high leakage at the off-state [1][3]. In our previous work, in order to address this issue, we incorporated a vertical spacer between the channel and N+ source/drain (S/D) to accommodate the depletion region near the channel-drain junction. The spacer significantly improved off-state characteristics such as off-state leakage, drain-induced barrier lowering (DIBL), and subthreshold swing (SS) without increasing the device footprint [3], [4]. In this work, by adopting a ~4 nm-thick $In_{0.53}Ga_{0.47}As$ channel instead of a thick InAs channel, we have further improved the off-state characteristics at high V_{DS} and achieved 81 mV/dec. minimum subthreshold swing (SS_{min}) for a 35 nm-L_g device at V_{DS}=0.5 V and 385 μA/μm on-current (I_{on}) at 100 nA/μm off-current (I_{off}) and V_{DD}=0.5 V, which are the best SS_{min} and I_{on} from all reported $In_{0.53}Ga_{0.47}As$ channel FETs.

The epitaxial layers, grown on semi-insulating InP by solid source MBE, consist of a 7 nm unintentionally doped (U.I.D) $In_{0.53}Ga_{0.47}As$ channel on an $In_{0.52}Al_{0.48}As$ back-barrier, the details of which are described in [3]. ~50 nm of HSQ was spun and patterned by e-beam lithography for dummy gate formation. To form the vertical spacer and N+ S/D, a 10 nm unintentionally doped and a 60 nm Si-doped ($4 \cdot 10^{19}$ cm^{-3}) $In_{0.53}Ga_{0.47}As$ layer were selectively regrown at 600°C using a MOCVD. Device mesas were isolated by a wet-etch. Dummy gates were removed in buffered oxide etch. To remove the surface which reacted with the dummy gates during the regrowth, ~3 nm of InGaAs surface was isotropically wet-etched using a digital etch [5]. The sample was then immediately loaded into an ALD. After *in-situ* N_2/TMA treatment during which ~0.5 nm of Al_2ON_x was formed, ~3 nm HfO_2 was deposited [6]. The sample was then annealed in forming gas at 400°C. Ni/Au gate metals and Ti/Pd/Au S/D metal contacts were lifted-off using a thermal and an e-beam evaporator, respectively. The summary of the process flow and the cross-sectional schematic of the device structure are described in Fig. 1 (a) and (b). Fig. 1(c) shows a top-down SEM image for a device with a 35 nm of gate length (L_g). Here, the L_g is defined as the spacing between the edges of the regrown layer. Because the vertical spacer is also gated as shown in Fig. 1(b), the effective gate length is ~34 nm larger than the lateral, lithographic gate length L_g.

Fig. 2 shows the transfer characteristics of a device with a 35 nm-L_g. The device shows 1.7 mS/μm peak g_m at V_{DS}=0.5 V and 385 μA/μm on-current (I_{on}) at a fixed I_{off}=100 nA/μm and V_{DD}=0.5 V. Fig. 3 shows the subthreshold characteristics for the 35 nm-L_g device. Its SS_{min} at V_{DS}= 0.1 and 0.5 V are 73 mV/dec. and 81 mV/dec., respectively. Its threshold voltage (V_T) defined at I_D=1 μA/μm is 0.15 V, and DIBL is 85 mV/V. Fig. 4 shows the output characteristics of the 35 nm-L_g device. The device exhibits excellent I_D saturation even at the short gate length. Its on-resistance (R_{on}) is 304 Ω·μm at V_{GS}=1.2 V. Fig. 5 shows subthreshold characteristics of a device with a 1 μm-L_g. Its SS_{min} at low V_{DS} of 0.1 V is 64 mV/dec., from which an interfacial trap density (D_{it}) of $2.8 \cdot 10^{12}$ $cm^{-2} \cdot eV^{-1}$ is calculated. The gate leakage is negligible at all measured bias (not shown). Fig. 6 shows the peak g_m at V_{DS}=0.5 V as a function of the gate length. The peak g_m does not saturated at 35 nm gate length, indicating that further gate length scaling may continue to improve on-state performance. Fig. 7 shows R_{on} as a function of gate length. The R_{on} extrapolated at the zero gate length is 233 Ω·μm, which includes ~90 Ω·μm S/D access resistance, as determined by TLM measurement (not shown). Fig. 8 shows DIBL as a function of the gate length, comparing with recently reported III-V MOSFETs. The devices in this work show significantly lower DIBL at similar gate lengths than other planar III-V MOSFETs. We believe that this is mostly because the vertical spacer and the thin 4nm channel improve electrostatic integrity especially at short L_g. In addition, the smaller off-state leakage at V_{DS}= 0.5V of the $In_{0.53}Ga_{0.47}As$-channel MOSFETs, compared to that of InAs [3], is likely due to reduced BTBT in the high drain-field region. Fig. 9 shows SS_{min} at V_{DS}=0.5 V as a function of the gate length. These devices have the lowest SS_{min} compared to any other III-V MOSFETs regardless of the device architecture, which is attributed to both the high-k dielectric with sub-1 nm EOT and low D_{it} and the design features mentioned above. Fig. 10 compares I_{on} at I_{off}=100 nA/μm and V_{DD}=0.5 V with recently reported III-V MOSFETs result. Due to the outstanding subthreshold characteristics, the devices have higher I_{on} at sub-50 nm-L_g than other reported III-V MOSFETs.

[1] J. Lin, *et al.*, IEDM (2013), [2] S. W. Chang, *et al.*, IEDM (2013), [3] S. Lee, *et al.*, APL, vol. 103, no. 23 (2013), [4] S. Lee, *et al.*, EDL submitted, [5] S. Lee, *et al.* IPRM (2013), [6] V. Chobpattana, *et al.*, APL, vol. 113, (2013)

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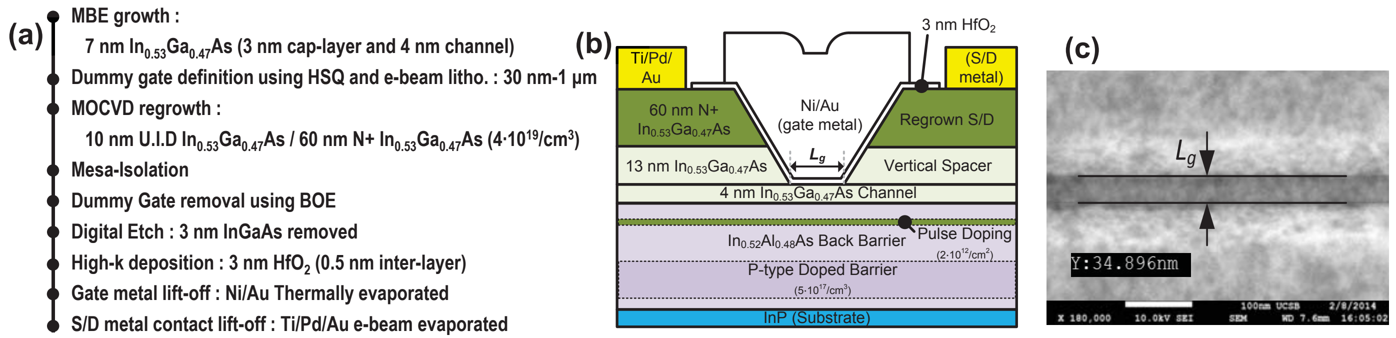

Fig. 1. (a) Summary of fabrication process flow, (b) schematic cross-section for raised S/D InGaAs QW MOSFETs, and (c) top-down SEM image for a gate trench (without gate metal) of a 35 nm-L_g device.

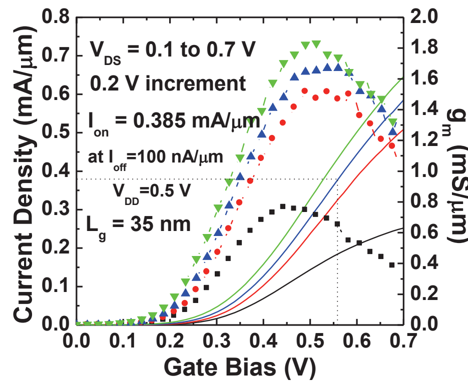

Fig. 2. I_D-V_{GS} and g_m for a 35 nm-L_g device.

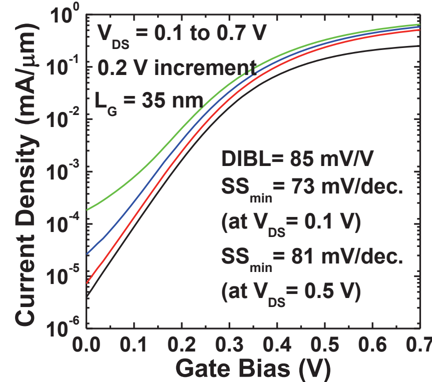

Fig. 3. log(I_D)-V_{GS} for a 35 nm-L_g device.

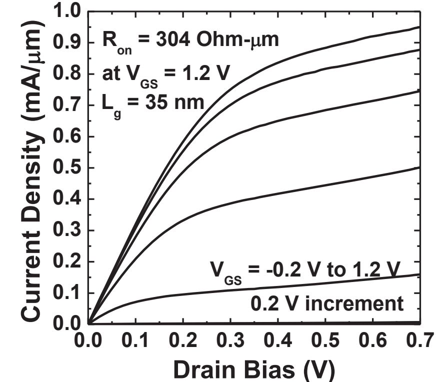

Fig. 4. I_D-V_{DS} for a 35 nm-L_g device.

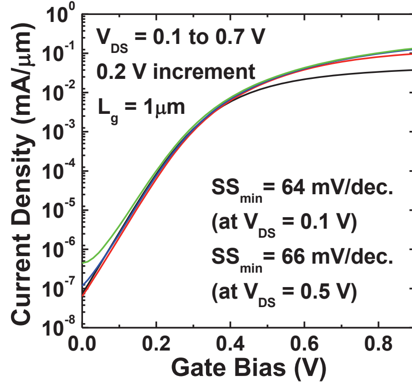

Fig. 5. log(I_D)-V_{GS} for a 1 μm-L_g device.

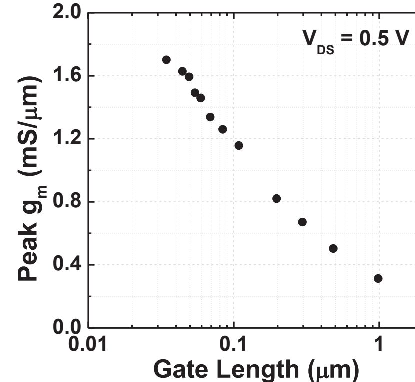

Fig. 6. Peak g_m vs. L_g.

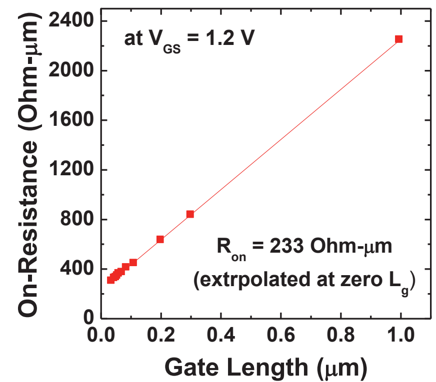

Fig. 7. R_{on} at V_{GS}=1.2 V vs. L_g.

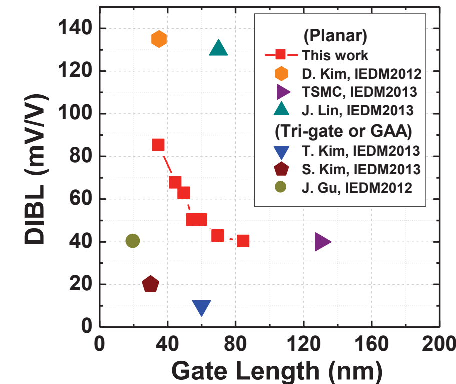

Fig. 8. DIBL vs. L_g, comparing with recently reported III-V MOSFETs

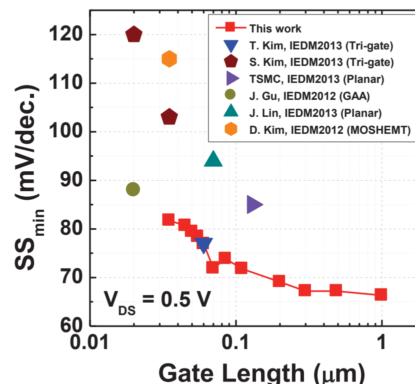

Fig. 9. SS_{min} at V_{DS}=0.5 V vs. L_g , comparing with recently reported III-V MOSFETs

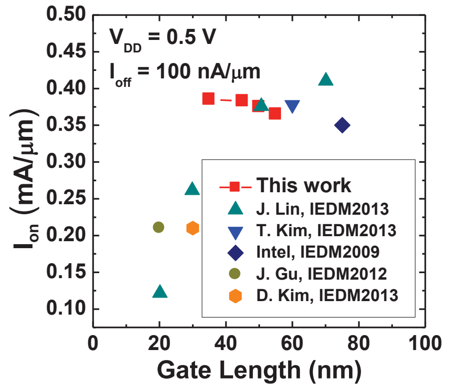

Fig. 10. I_{on} at I_{off}=100 nA/μm and V_{DD}=0.5 V vs. L_g, comparing with recently reported III-V MOSFETs