An 81 GHz, 470 mW, 1.1 mm^2 InP HBT Power Amplifier with 4:1 Series Power Combining using Sub-quarter-wavelength Baluns

[1]Hyun-chul Park, [1]Saeid Daneshgar, [1]Johann C. Rode, [2]Zach Griffith, [2]Miguel Urteaga, [3]Byung-sung Kim, and [1]Mark Rodwell

[1]ECE Department, University of California at Santa Barbara, Santa Barbara, CA, 93106, USA,
[2]Teledyne Scientific and Imaging, 1049 Camino Dos Rios, Thousand Oaks, CA, 91360, USA,
[3]ECE Department, Sungkyunkwan University, Suwon, 440-746, South Korea,
Email: hcpark@ece.ucsb.edu

Abstract — We report a two-stage W-band power amplifier (PA) using novel 4:1 series power-combining with sub-quarter-wavelength baluns. The power amplifier, fabricated in a 0.25 µm InP HBT technology, produces 470 mW (26.7 dBm) output power at 81 GHz, 23.4 % peak PAE, and >11.5 GHz 3-dB bandwidth. The compact series power-combining networks permit a small 1.06 mm^2 die area and a high 443 mW/mm^2 output power per unit die area.

Index Terms — Power amplifier, sub-quarter-wavelength balun, series power combining, W-band, InP.

I. Introduction

The mm-wave bands will enable future high speed wireless communications links and high resolution radar [1]-[6]. Propagation losses are high, particularly in foul weather, hence high power amplifiers (PAs) are needed for long transmission range. High PA efficiency reduces power-supply and heat-sink costs, while high power per unit die area reduces IC costs and enables integration into monolithic arrays.

Compact, efficient power-combining is necessary for high power-added efficiency (PAE) and small die area. Classical thru-substrate transmission-line power-combiners suffer from appreciable radiative substrate losses and occupy large die area [1]-[2]. With transformer combiners, the challenges are low inductor Q, low coupling factor, and port imbalances [3]-[4]. Direct transistor series-connection with local feedback [5]-[6] enables low-loss power-combining in a small die; here the challenges are maintaining a uniform voltage distribution and unity current gain, so that all transistors compress at once. A new compact 2:1 series-connected design using sub-quarter wavelength (λ/4) baluns was proposed in [7]; this showed >30 % PAE and >20 dBm output power (P_{out}) at 86 GHz with a 2.5 V supply.

Here we extend the technique of [7] to 4:1 series combining for low supply voltage devices (i.e. InP and Silicon). The two-stage design (Fig. 1) operates at 81 GHz and uses InP HBTs. Compact sub-λ/4 series baluns connect the output transistors in series. With a 4:1 series connection, the PA output power is increased 16:1 over a design in which the HBTs directly drive 50 Ω. The two-stage amplifier is small (1.1 mm^2 including pads), and produces 470 mW P_{out} at 23.4 % PAE.

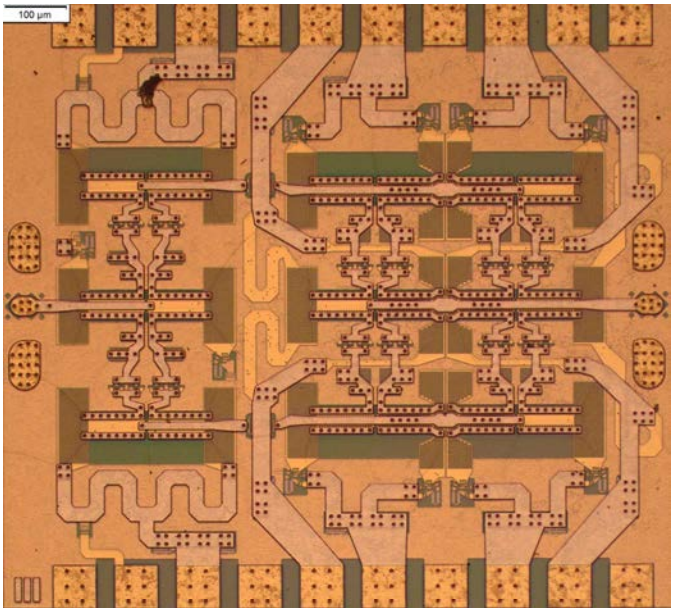

Fig. 1. Die photograph of the two-stage PA using 4:1 series power combining (Die area: 1.08 × 0.98 mm^2).

II. Series Combining Using Sub -λ/4-Baluns

Using two baluns, the output power-combiner connects in series the outputs of four HBT cells. The amplifier output voltage is the sum of the voltages at the four HBT cells; each cell sees a 12.5 Ω load, and must have 4:1 larger junction area, and 4:1 larger output current, than a cell sized to directly drive 50 Ω. Neglecting losses, the output power is therefore increased 16:1. The baluns are much shorter than $\lambda_g/4$ (~$\lambda_g/16$ in this design), a quarter of a guide wavelength, minimizing combining losses and reducing die area. The sub-quarter-wave baluns load the transistor with an inductive shunt stub, loading which tunes the transistor output capacitance.

First consider [7] a 2:1 series power-combiner, Fig. 2 (a), using tri-plate transmission lines with M_1 ground plane, M_2 intermediate conductor, and M_3 upper conductor. The M_2 conductor is much wider than the M_3 conductor, shielding the M_3 line from M_1 to assure P_2 to P_3 balance. There are

978·1-4799-3869-8/14/$31.00 ®2014 IEEE

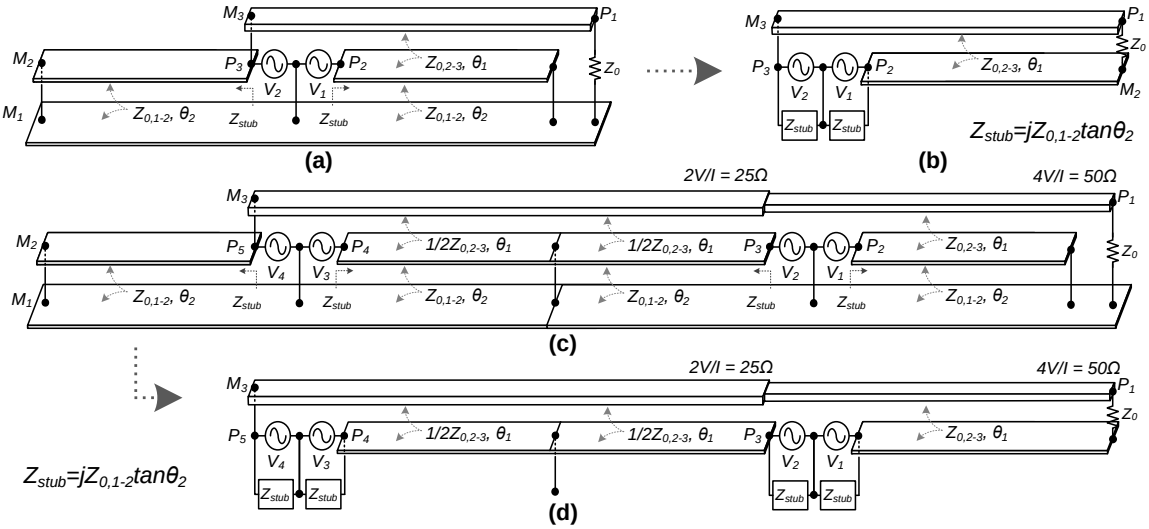

Fig. 2. Sub-quarter-wavelength balun concepts: (a) 2:1 balun structure, (b) 2:1 simplified balun model illustrated in [7], (c) new proposed 4:1 balun structure, and (d) 4:1 simplified balun model.

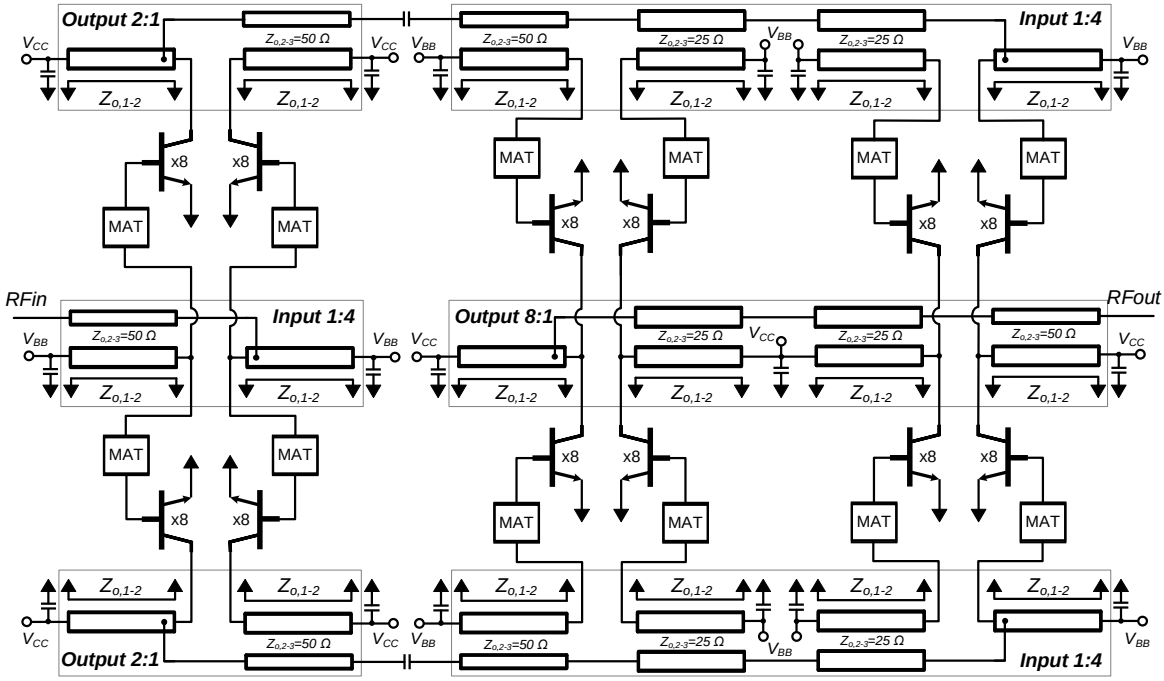

Fig. 3. A two-stage PA schematic using the series power combining baluns (2:1 baluns in the first stage and 4:1 baluns in the second stage).

microstrip lines of impedance $Z_{0,1\text{-}2}$ between M_1 and M_2 and of impedance $Z_{0,2\text{-}3}$ between M_2 and M_3.

The 2:1 power-combiner, Fig. 2 (a), is understood using the equivalent circuit of Fig. 2 (b). Voltage sources V_1 and V_2 are connected in series between conductors M_2 and M_3, a 50 Ω transmission-line connected to the 50 Ω load. V_1 and V_2 each see a 25 Ω load. V_1 and V_2 are also loaded in parallel by the shunt-stub impedance $Z_{stub}=jZ_{0,1\text{-}2}\tan\theta_2$ from the short-circuited transmission-line stubs between M_1 and M_2.

In class-A power amplifiers, highest output power and highest collector/drain efficiency are obtained if the transistor is loaded by an *LR* parallel network where $R_{L,\text{opt}}=(V_{\max}-V_{\min})/I_{\max}$, is the ratio of maximum transistor voltage swing to maximum transistor current, and where $j\omega L=-1/j\omega C_{\text{out}}$, where C_{out} is the transistor output capacitance. The HBT junction area, hence $I_{\max}$, are adjusted until $R_{L,\text{opt}}=25$ Ω, , and the balun length θ_2 is adjusted to set $Z_{stub}=-1/j\omega C_{\text{out}}$. Each HBT power cells has 2:1 larger junction area, and 2:1 larger $I_{\max}$, than a device sized to directly drive 50 Ω with appropriate shunt inductive tuning. The output power is therefore increased 4:1.

The 4:1 series-connected design, Fig. 2 (c), has the equivalent circuit of Fig. 2 (d). The four sources V_1 V_4 are connected in series across the 50 Ω amplifier load. Each source sees a 12.5 Ω load, again loaded in parallel with Z_{stub}. Design therefore consists of adjusting the HBT junction area, and hence $I_{\max}$, until $R_{L,\text{opt}}=12.5$ Ω, and then adjusting the

978·1-4799-3869-8/14/$31.00 ®2014 IEEE

TABLE I – SUMMARY OF RECENT W-BAND POWER AMPLIFIERS

Ref.	Technology	Freq. (GHz)	f_{max} / f_τ (GHz)	$BW_{3\text{-}dB}$ (GHz)	Max. S_{21}(dB)	P_{out} (dBm)	Peak PAE (%)	V_{DD} or V_{CC} (V)	Area (mm^2)	mW /mm^2	Topology
[1]	0.14 µm GaN HEMT	93.5	230 / 97	~10	~18	31.5	22.0	12	-	-	-
[2]	0.14 µm GaN HEMT	91	-	~7	~16	30.8	>20	17.5	2.25	530	Classic corporate combiner
[4]	0.13 µm BiCMOS	62	-	>10	20.6	20.1	18.0	1.8	0.72	142	4-way transformer
[7]	0.25 µm InP HBT	86	590 / 350	23	9.4	20.4	30.4	2.5	0.37	294 (723)	2:1 sub-λ/4 series power combiner
[7]	0.25 µm InP HBT	86	590 / 350	-	17.5	23.1	30.2	3.0	0.67	307 (497)	2-stage 2:1 sub-λ/4 series power combiner
This work	0.25 µm InP HBT	81	590 / 350	>11.5	17.5	26.7	23.4	2.75	1.06	443 (633)	2-stage 4:1 sub-λ/4 series power combiner

balun length θ_2 until Z_{stub}=-1/$j\omega C_{out}$. The HBT power cells now have 4:1 larger junction area, and 4:1 larger I_{max}, than a device sized to directly drive 50 Ω, hence the total output power is increased 16:1. The line connecting V_2 and V_3 must have 25 Ω impedance realized by periodically capacitive loaded transmission lines [8]. The phases of (V_1, V_2) must differ those of (V_3, V_4) by the delay of the line connecting V_2 and V_3, the latter requirement satisfied by using an identical input power-splitter. A separate test structure measurement shows the insertion loss of the 4:1 combiner to be 0.92 dB, where the 0.5 dB roll-off bandwidth is between 73 GHz and 103 GHz.

III. PA IC DESIGNS AND MEASURED RESULTS

The PAs were designed into a 0.25 µm InP HBT process, which exhibits BV_{CEO}=4.5 V, f_{max}=590 GHz, and f_τ=350 GHz [9]. There are three Au interconnect planes, M_1, M_2, and M_3 (top) of 1 µm, 1 µm, and 3 µm thicknesses. A 5 µm thick BCB (ε_r=2.7) dielectric separates M_3 and M_2, while 1 µm of BCB separates M_2 and M_1. The process provides 0.3 fF/µm^2 MIM capacitors and 50 Ω/square thin-film-resistors (TFR).

Fig. 3 shows the schematic. The basic HBT power cell (48 µm periphery, 2 x (4 x 6 µm)) has $R_{L,opt}$=25 Ω. Details of the HBT PA unit cell have been reported in [10]. The input driver stage uses 2:1 series splitters and combiners, and has two separate RF outputs driving the two inputs of the main PA stage. In the main power amplifier stage, each RF input is split by a 4:1 series-connected balun network, dividing the total input power among eight HBT cells. The HBT cells are then connected into four pairs, four above and four below the output power-combiner of Fig. 3 with each pair driving one port of the output combiner. Each pair of cells requires $R_{L,opt}$=12.5 Ω, the impedance presented to the pair by each port of the combiner.

Transistor inputs are matched by two-section *LC* networks, and emitter-buffered active bias circuits increase the DC collector current as output power increases [11], this enhancing thermal stability. Bias is slightly below class-A.

Fig. 4 shows measured IC performance. The zero-signal bias currents are 60 mA and 400 mA for the 1st and 2nd stages.

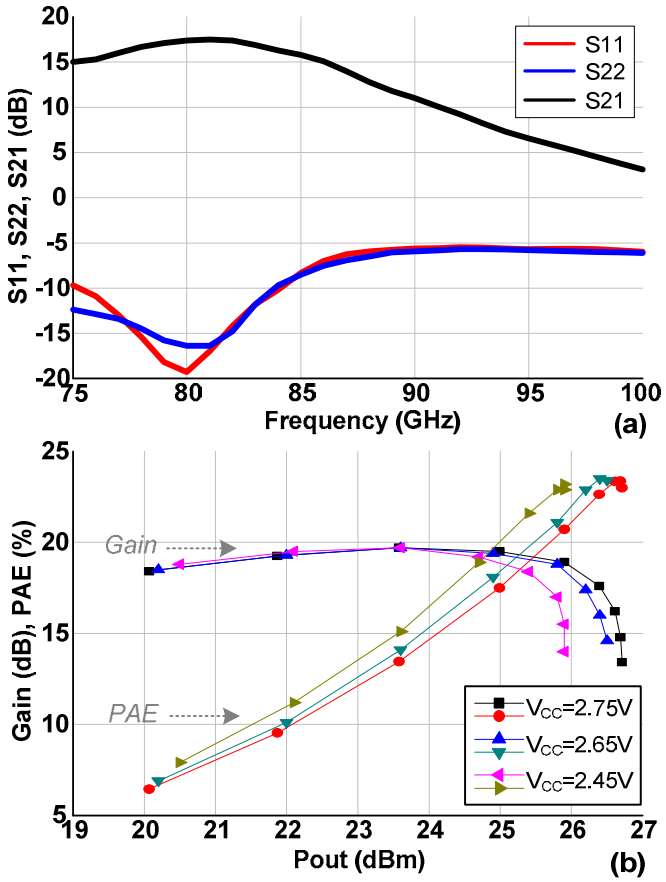

Fig. 4. Measured PA IC results: (a) small signal s-parameters, and (b) large signal gain and PAE vs. output powers.

The PA exhibits (Fig. 4 (a)) 17.5 dB gain S_{21} at 81 GHz, >11.5 GHz 3-dB bandwidth, and (S_{11}, S_{22}) <-10 dB over a 10 GHz bandwidth. In 81 GHz large signal measurements at V_{CC}=2.75 V (Fig. 4 (b)), the PA IC exhibits 26.7 dBm (470 mW) maximum output power, 23.4 % peak PAE, and 443 (633) mW/mm^2 power density including (excluding) pads.

IV. CONCLUSION

We demonstrated a compact high performance W-band InP power amplifier (PA) using a new 4:1 sub-λ/4 balun series

978·1-4799-3869-8/14/$31.00 ®2014 IEEE

power combining technique. The PA showed output power of 470 mW and peak PAE of 23.4 % with IC size of 1.06 mm^2. With improved thermal stability and high supply voltage of 3.0 V, >28 dBm output power can be expected.

ACKNOWLEDGEMENT

This work is supported by DARPA Mobile HotSpots program. The author would like to thank to Teledyne Science Company for the PA IC fabrications.

REFERENCES

[1] M. Micovic, A. Kurdoghlian, A. Margomenos, D.F. Brown, K. Shinohara, S. Burnham, I. Milosavljevic, R. Bowen, A.J. Williams, P. Hashimoto, R. Grabar, C. Butler, A. Schmitz, P.J. Willadsen, and D.H. Chow, "92–96 GHz GaN power amplifiers," *2012 IEEE IMS*, pp.1,3, 17-22 June 2012.

[2] A. Brown, K. Brown, J. Chen, K.C. Hwang, N. Kolias, and R. Scott, "W-band GaN power amplifier MMICs," *2011 IEEE IMS*, pp.1,4, 5-10 June 2011.

[3] T.S.D. Cheung, J.R. Long, T.V. Tretiakov, and D.L. Harame, "A 21-27GHz self-shielded 4-way power-combining PA balun," *2004 IEEE CICC*, pp. 617-620, 3-6 Oct. 2004.

[4] Z. Yi, and J.R. Long, "A Wideband, Dual-Path, Millimeter-Wave Power Amplifier With 20 dBm Output Power and PAE Above 15% in 130 nm SiGe-BiCMOS," *IEEE JSSC*, vol.47, no.9, pp.1981-1997, Sept. 2012.

[5] M. Rodwell, S. Jaganathan, S. T. Allen, "Series-connected Microwave Power Amplifiers with Voltage Feedback and Method of Operation for the Same," *U.S. Patent* 5,945,879, Aug. 31, 1999.

[6] A. Agah, J. Jayamon, P. Asbeck, J. Buckwalter, and L. Larson, "A 11% PAE, 15.8-dBm Two-Stage 90-GHz Stacked-FET Power Amplifier in 45-nm SOI CMOS," *2013 IEEE IMS*, 2-7, June 2013.

[7] H. Park, S. Daneshgar, J.C. Rode, Z. Griffith, M. Urteaga, B. Kim, and M. Rodwell, "30% PAE W-Band InP Power Amplifiers Using Sub-Quarter-Wavelength Baluns for Series-Connected Power-Combining,." *2013 IEEE CSICS*, pp. 1-4, 13-16, Oct. 2013.

[8] B. Agarwal, A. Schmitz, J. Brown, M. Matloubian, M. Case, M. Le, M. Lui, and M. Rodwell, "112-GHz, 157-GHz, and 180-GHz InP HEMT traveling-wave amplifiers," *IEEE Tran. MTT*, vol. 46, no. 12, pp. 2553-2559, Dec 1998.

[9] M. Seo, M. Urteaga, J. Hacker, A. Young, Z. Griffith, V. Jain, R. Pierson, P. Rowell, A. Skalare, A. Peralta, R. Lin, D. Pukala, and M. Rodwell, "InP HBT IC Technology for Terahertz Frequencies: Fundamental Oscillators Up to 0.57 THz," *IEEE JSSC*, vol. 46, no. 10, pp. 2203-2214, Oct. 2011.

[10] Z. Griffith, M. Urteaga, P. Rowell, R. Pierson, and M. Field, "Multi-finger 250nm InP HBTs for 220GHz mm-Wave Power", *2012 IEEE IPRM*, Aug. 26-30, 2012.

[11] Y. Youngoo, K. Choi, and K.P. Weller, "DC boosting effect of active bias circuits and its optimization for class-AB InGaP-GaAs HBT power amplifiers," *IEEE Tran. MTT*, vol. 52, no. 5, pp. 1455-1463, May 2004.

978·1-4799-3869-8/14/$31.00 ®2014 IEEE