



TU3B-1

An 81 GHz, 470 mW, 1.1 mm² InP HBT Power Amplifier with 4:1 Series Power Combining using Sub-quarter-wavelength Baluns

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Outline

- Motivation, Challenge
- Power-combining Techniques in mm-Wave
- Proposed Baluns (2:1 and 4:1 Series Combiners)
- Power Amplifier Designs (2:1 and 4:1)
- Measurement Results and Comparisons
- Conclusion

mm-Wave Power Amplifier: Challenges

mm-Wave PAs:

Applications: High speed communications, high resolution images

Needed: High power / High efficiency / Small die area (low cost)

Extensive power combining

Compact power-combining

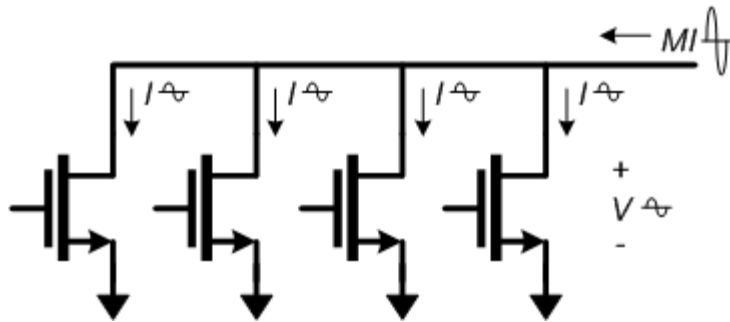
$$\text{PAE} = \eta_{\text{drain/collector}} \left(1 - \frac{1}{\text{Gain}} \right) \cdot \eta_{\text{power-combiner}}$$

Class E/D/F are poor @ mm-wave
insufficient gain $\sim f_{max}$
high losses in harmonic terminations

Efficient power-combining

Goal: efficient, compact mm-wave power-combiners

Parallel Power-Combining

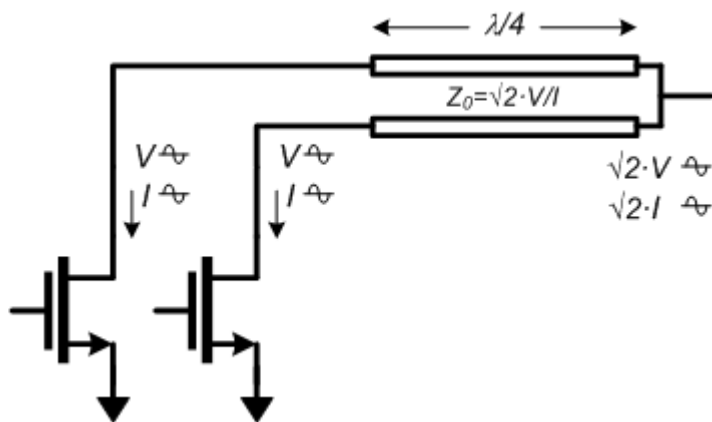


Output power: $P_{OUT} = V \times (M \times I)$

Parallel connection **increases** P_{OUT}

Load Impedance: $R_{OPT} = V / (M \times I)$

Parallel connection **decreases** R_{OPT}



High P_{OUT} using low $V_{DD} \rightarrow$ Low R_{OPT}

Needs impedance transformation:

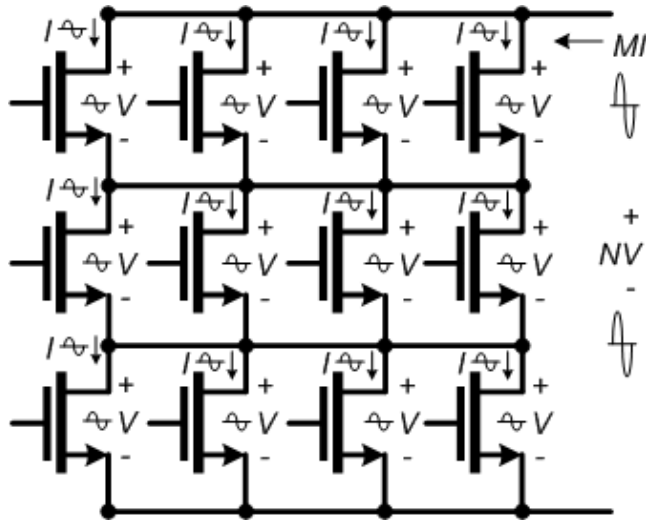
Wilkinson or lumped lines ...

\rightarrow **High insertion loss**

\rightarrow **Small bandwidth**

\rightarrow **Large die area**

Series Power-Combining & Stacks



Parallel connections: $I_{OUT} = \mathbf{M} \times I$

Series connections: $V_{OUT} = \mathbf{N} \times V$

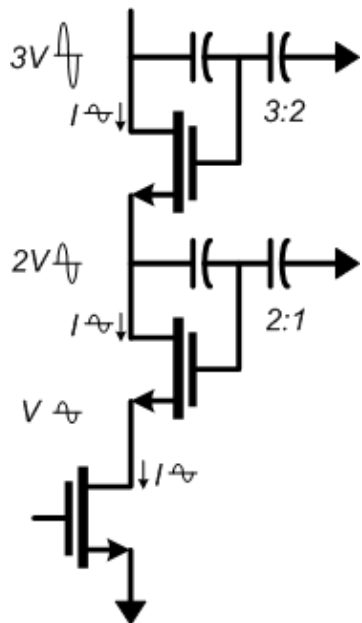
Output power: $P_{OUT} = (\mathbf{N} \cdot \mathbf{M}) \times V \times I$

Load impedance: $R_{OPT} = (\mathbf{N}/\mathbf{M}) \times V/I$

Small or zero power-combining losses

Small die area

BUT, how do we drive the gates ?



Local voltage feedback:

drives gates, sets voltage distribution

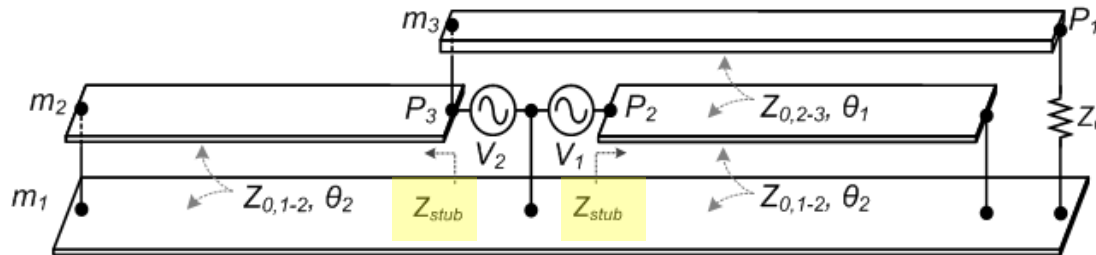
Design challenge:

need uniform RF voltage distribution

need \sim unity RF current gain per element

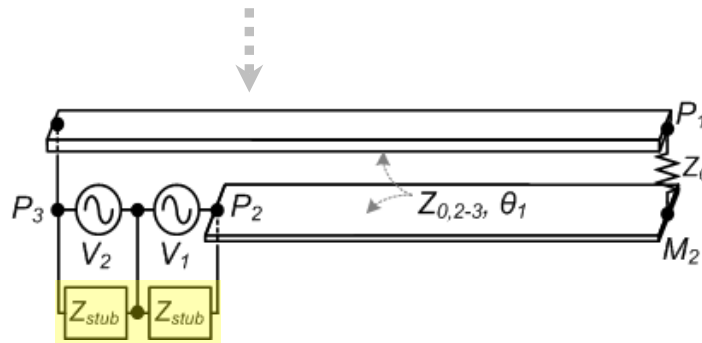
...needed for simultaneous compression of all FETs.

Proposed $\lambda/4$ Baluns



Balun structure

Simplified model



$$Z_{stub} = jZ_{0,1-2} \tan \theta_2$$

$$\text{if } \theta_2 = \lambda / 4, Z_{stub} = \infty$$

Our proposed balun with $\lambda/4$ lines

Three-conductor transmission-lines

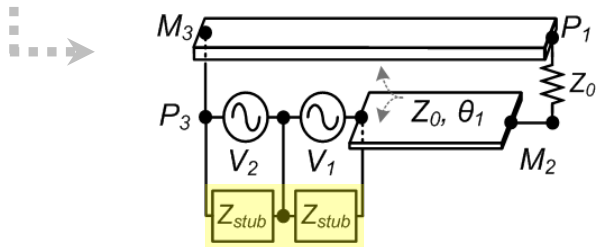
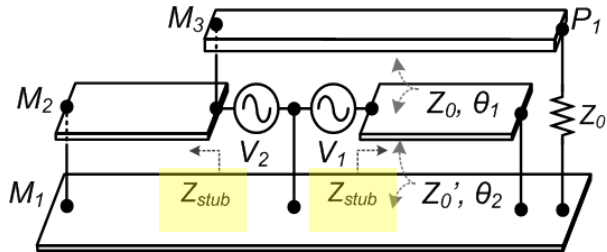
→ Two separate transmission lines (m_3 - m_2 , m_2 - m_1)

Fields between m_3 and m_1 isolated!

$\lambda/4$ line stub → $Z_{stub} = \text{open}$

BUT, still long line → high loss and large die area ☹

Proposed **Sub- $\lambda/4$** Baluns



What if balun length is $\ll \lambda/4$?
 \rightarrow Stub line becomes **inductive!**

Sub- $\lambda/4$ balun:

Inductive stub line

Tunes transistor C_{OUT} !!

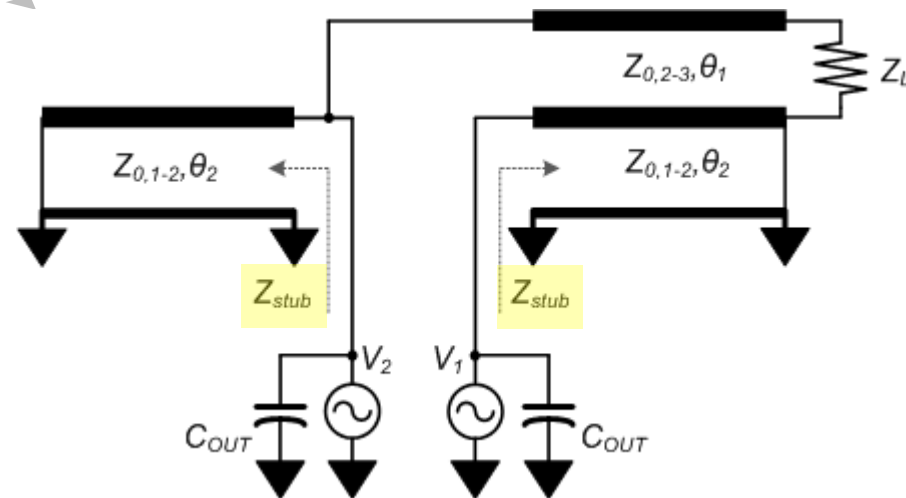
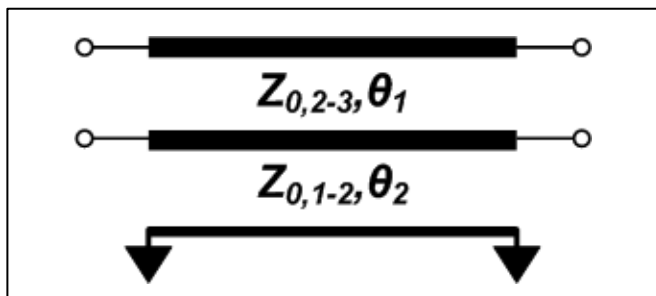
Short line \rightarrow **Low losses** 😊

\rightarrow **Small die area** 😊

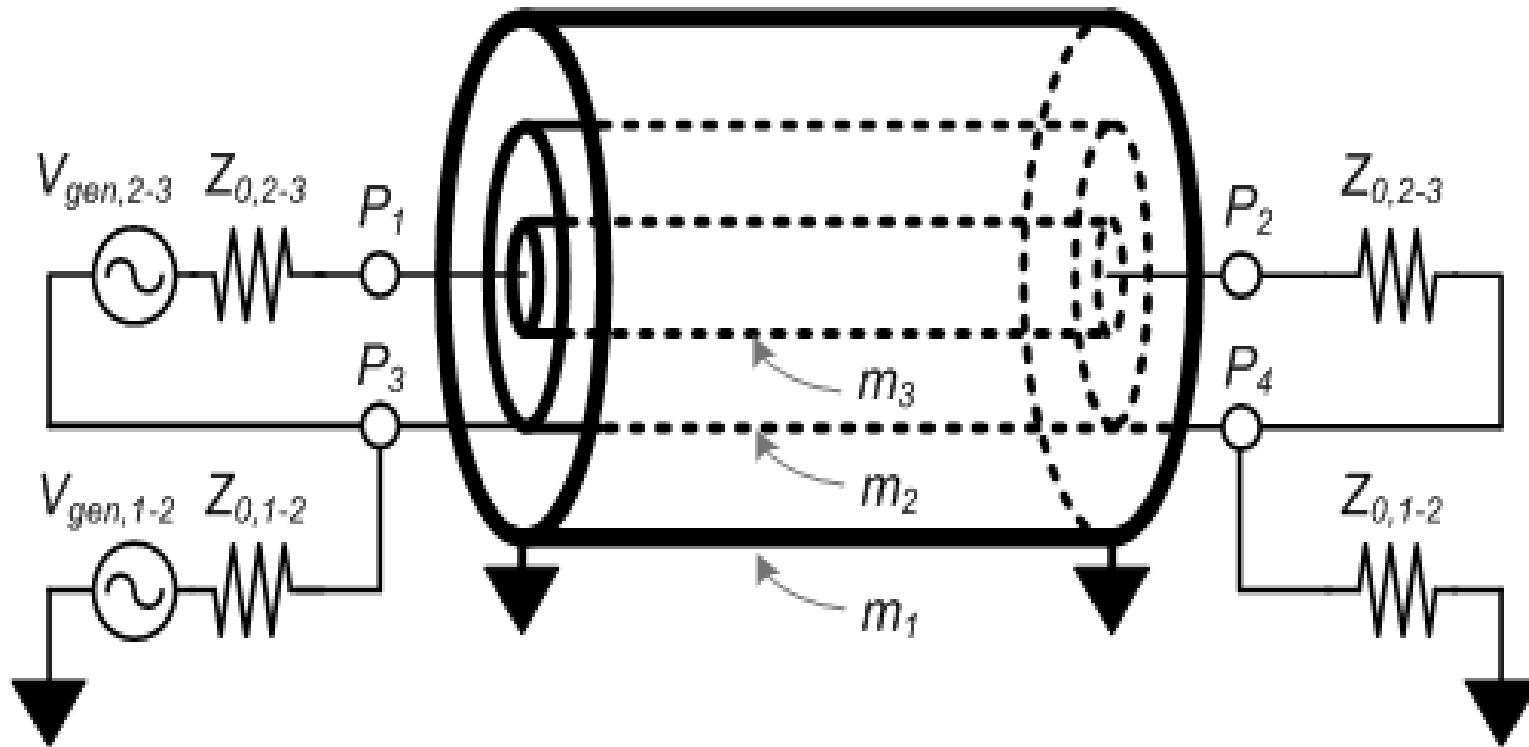
if $\theta_2 \ll \lambda/4$, $Z_{stub} \rightarrow$ inductive

*Symbol:

Three-conductor transmission line

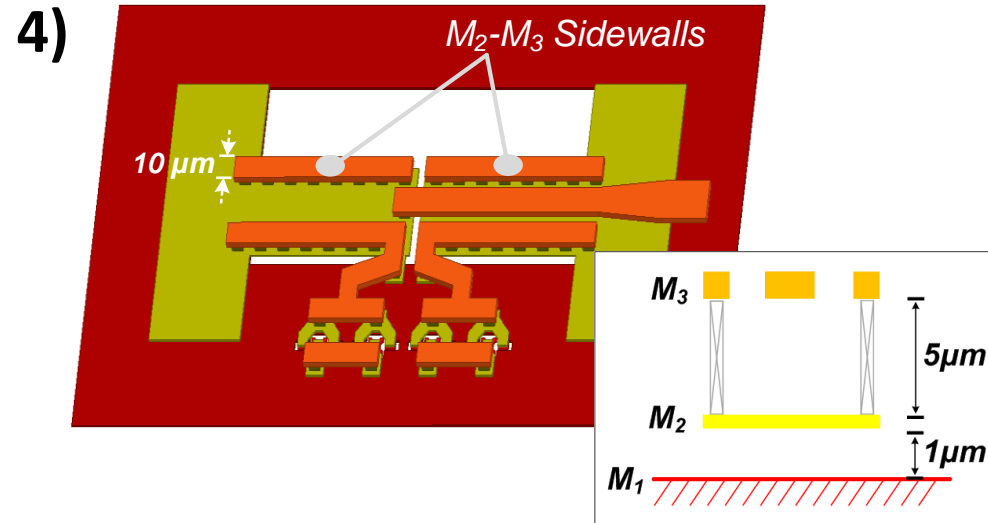
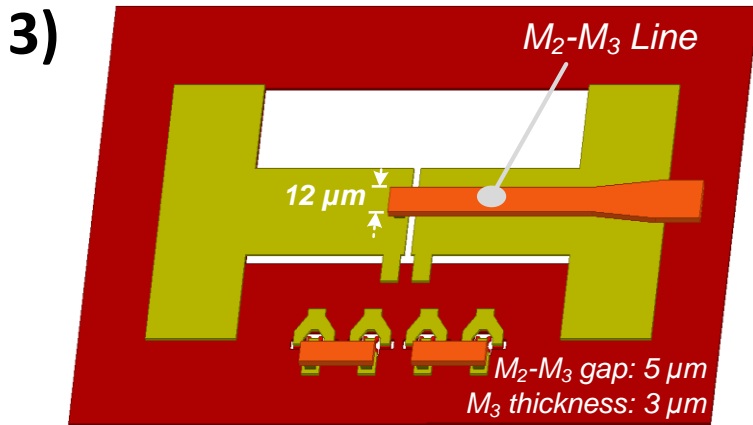
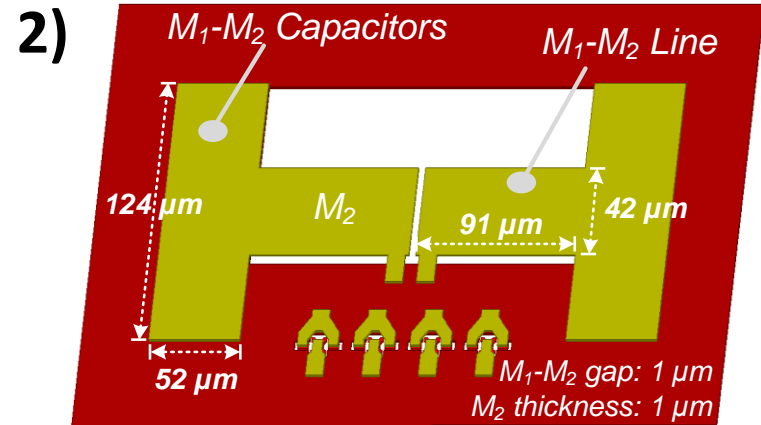
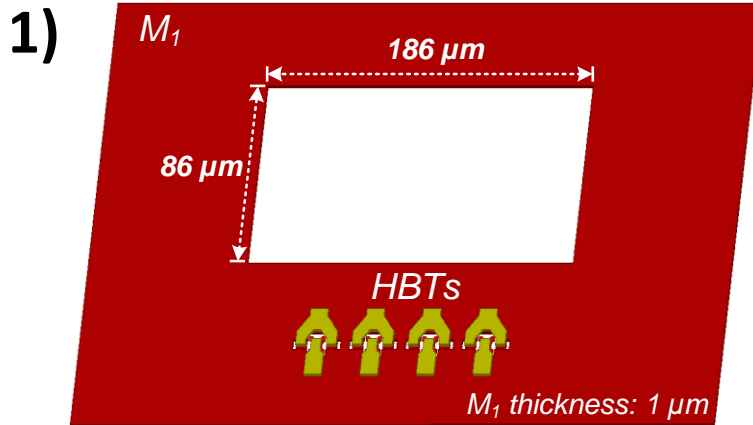


Ideal Tri-axial Line



Two separate transmission lines (m_3 - m_2 , m_2 - m_1)
→ E, H fields between m_3 and m_1 perfectly shielded

Baluns in Real ICs



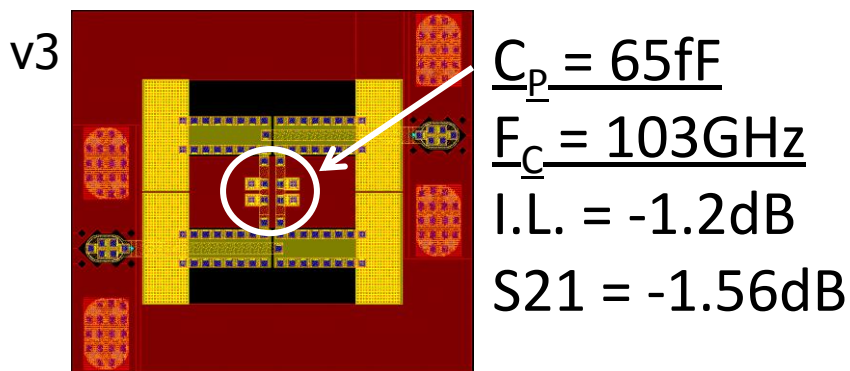
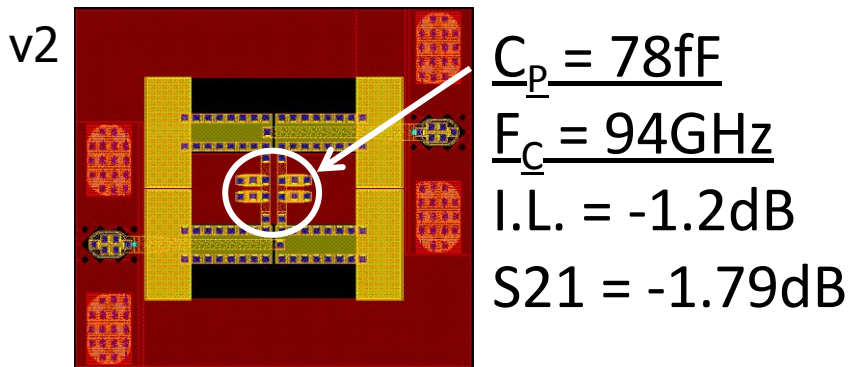
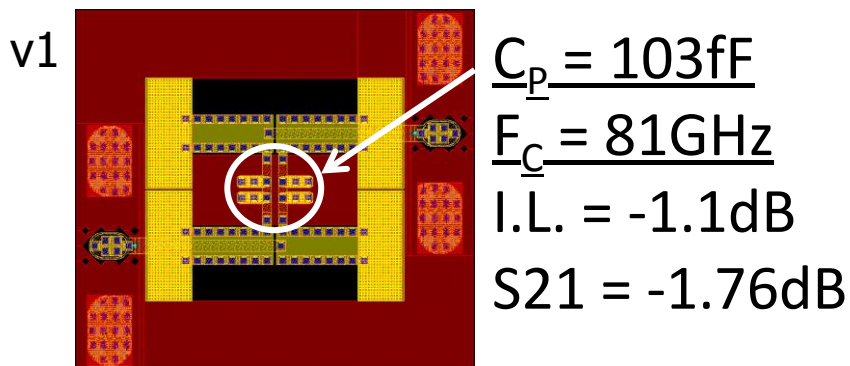
1) M_1 as a GND

2) Slot-type transmission lines (M_1 - M_2), AC short (2 pF MIM)

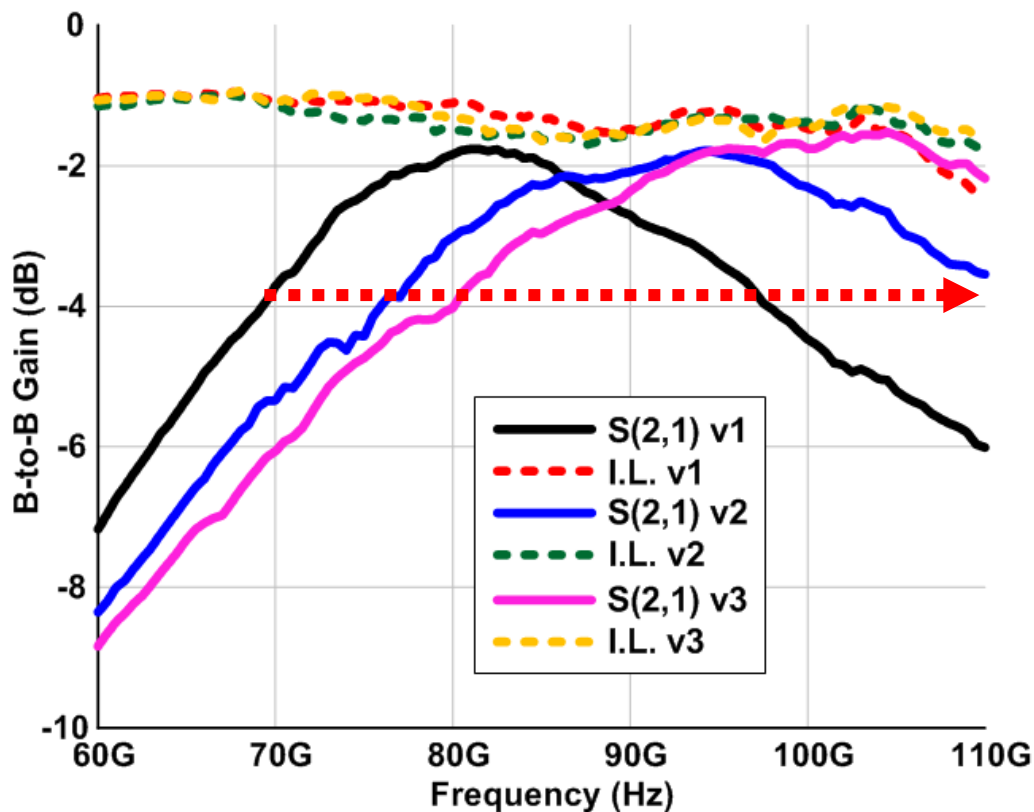
3) Microstrip line (M_2 - M_3), E-field shielding **NOT** negligible

4) **Sidewalls** between M_3 - M_1 (Faraday cages), **$\lambda/16$ length**

2:1 Balun B-to-B Test Results



Back-to-back measured S-parameters



**Does not de-embed losses of PADs, capacitors, and interconnection lines*

< 0.6dB single-pass insertion loss, 0.16 dB/2.7° imbalance

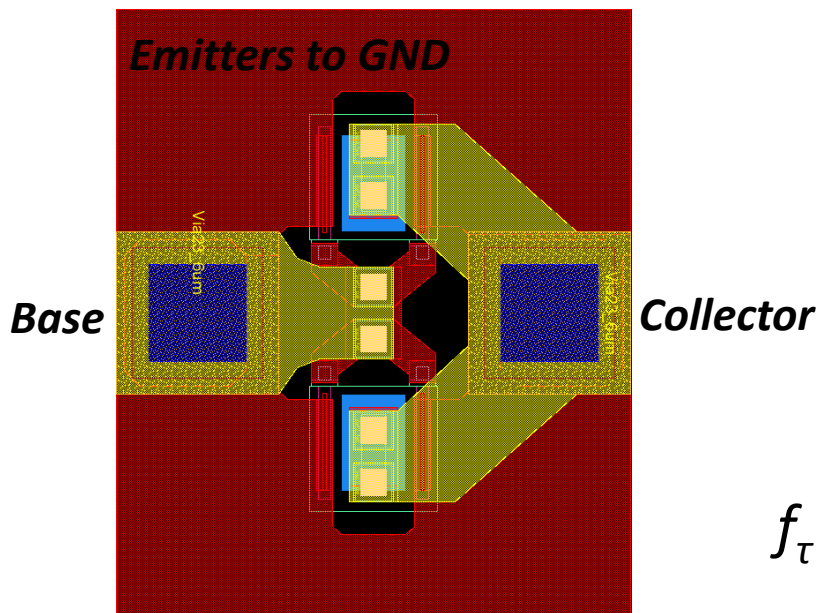
Teledyne **0.25 μm** HBTs

Cell: 4-fingers x 0.25 μm x 6 μm

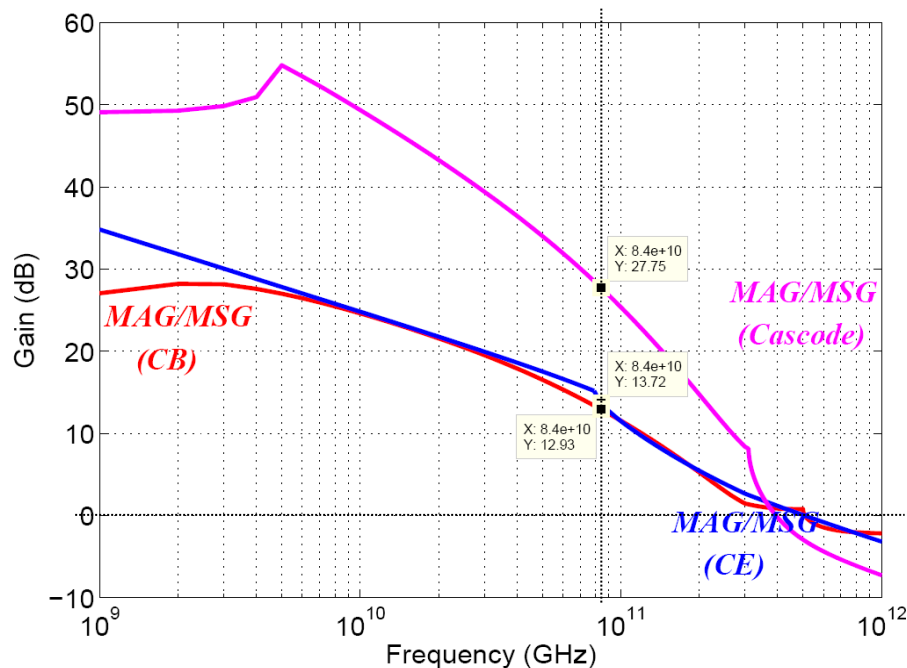
$BV_{CEO} = 4.5 \text{ V}$, $I_{C,max} = 72 \text{ mA}$

$P_{OUT} = 15.5 \text{ dBm}$

$R_{OPT} = 56 \Omega$



MAG/MSG including EM-Sim. results



$f_T = 285 \text{ GHz}$, $f_{max} = 525 \text{ GHz}$

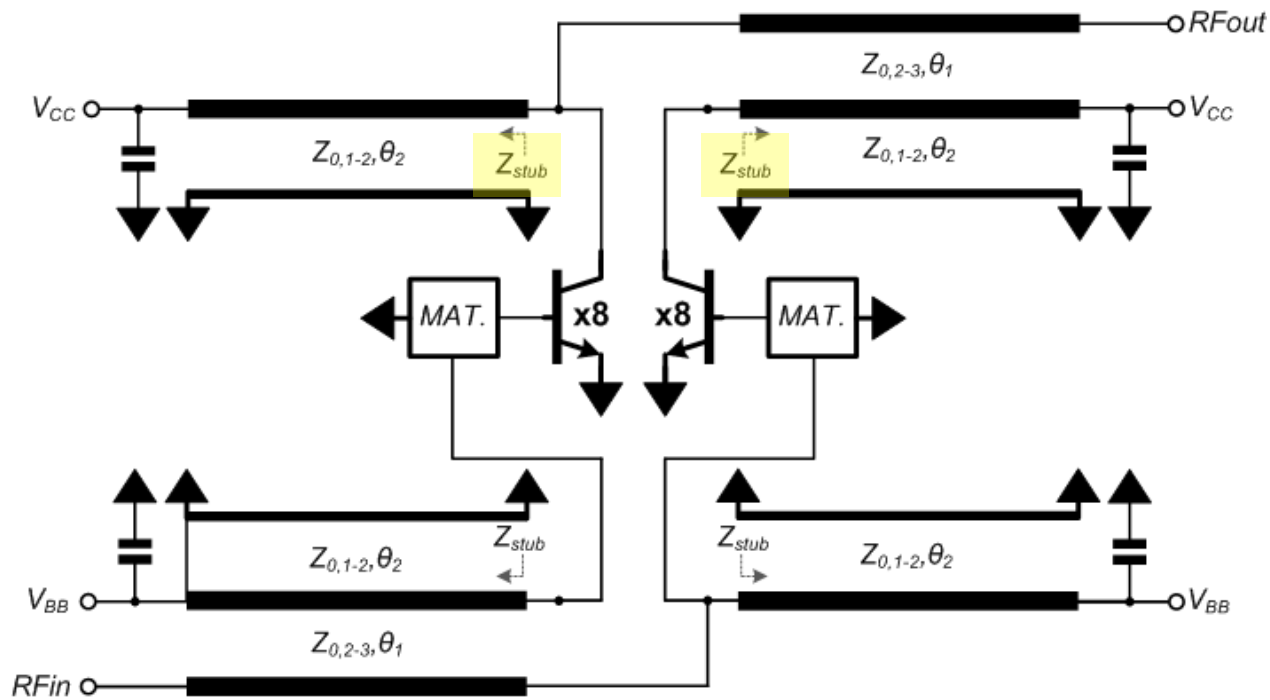
@ $J_E = 4.2 \text{ mA}/\mu\text{m}^2$ and $V_{CE} = 2.5 \text{ V}$

12~13dB MAG @ 86 GHz

[Z. Griffith et al, IPRM 2012]

Multi-finger 250nm InP HBTs for 220GHz mm-Wave Power Multi-finger 250nm InP HBTs for 220GHz mm-Wave Power

Sub- $\lambda/4$ Baluns: PA Design



Each HBT loaded by 25 Ω

HBT junction area selected
so that $I_{\max} = V_{\max} / 25 \Omega$

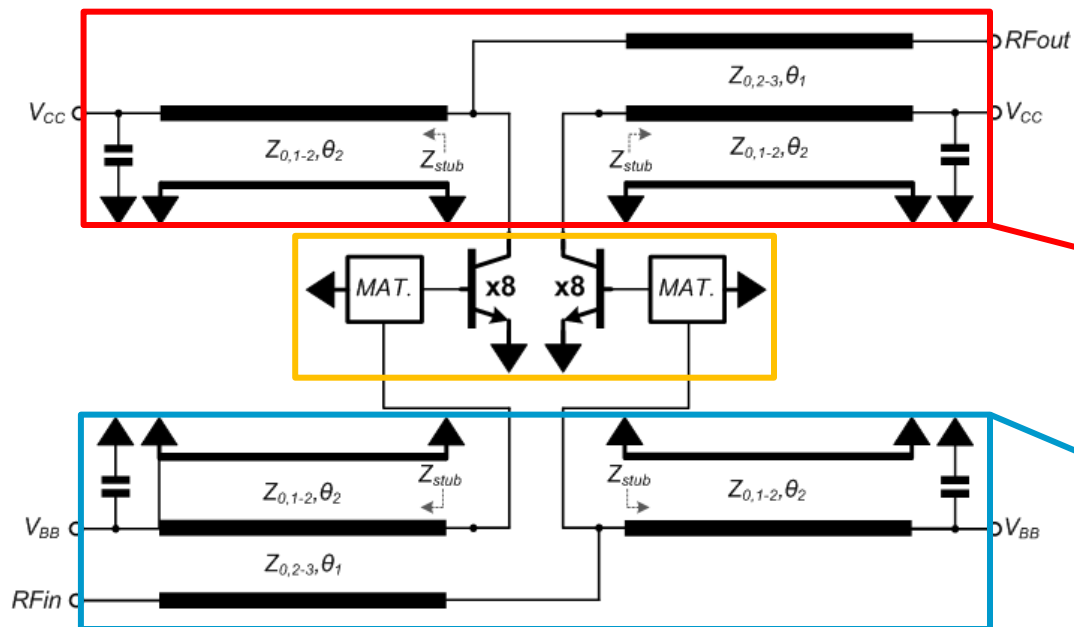
Each HBT has some C_{OUT}

Stub length picked so that
 $Z_{\text{stub}} = -1/j\omega C_{OUT} \rightarrow$ tunes HBT

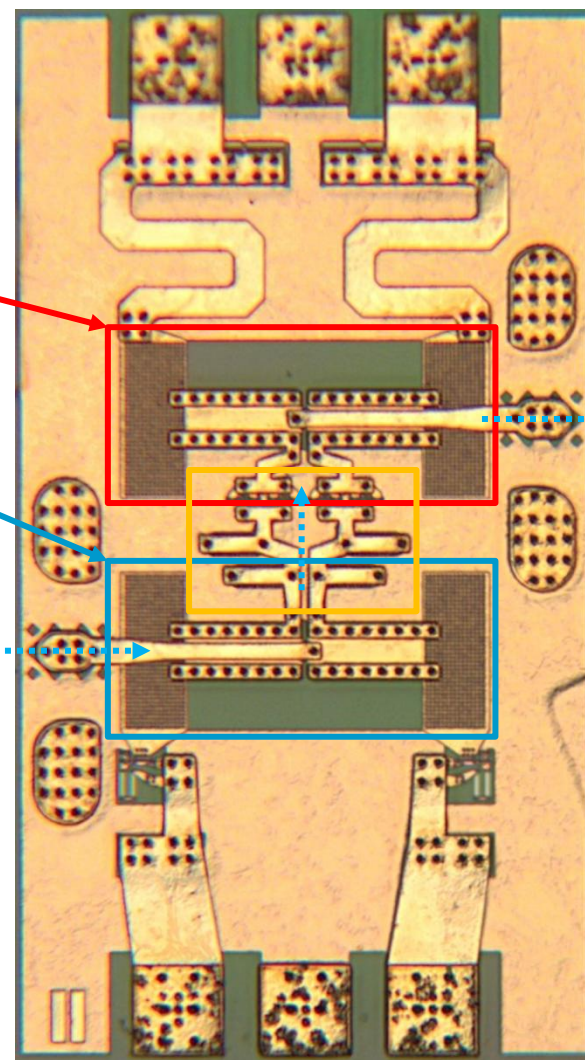
$$P_{out} = 4 \times \left(\frac{V_{\max}^2}{8 \cdot 50 \Omega} \right)$$

**4:1 more power
than without the combiner.**

4:1 PA Designs Using 2:1 Balun



Identical input / output baluns
2-section LC input matching network
Active bias: Thermal stability & class-AB



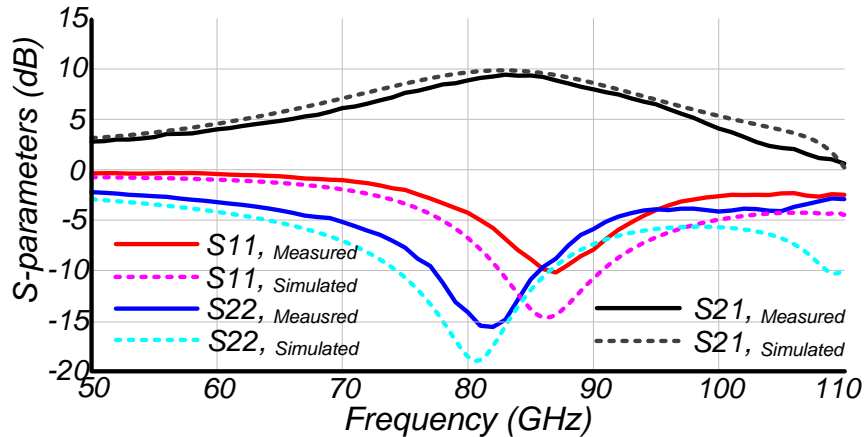
IC size: 450 x 820 μm^2

[H. Park et al, CSICS 2013]

30% PAE W-Band InP Power Amplifiers Using Sub-Quarter-Wavelength Baluns for Series-Connected Power-Combining

Single-Stage PA IC Test Results (86GHz)

Small signal measurements



x4 larger output power
than 50 Ohm R_{OPT} device

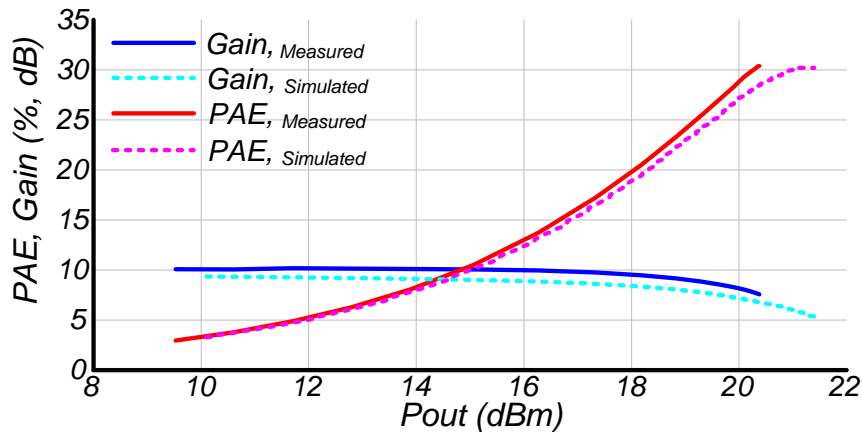
Gain: 10 dB

P_{SAT} : >100 mW @2.5V

PAE: >30 %

3-dB BW: 23 GHz

Large signal measurements

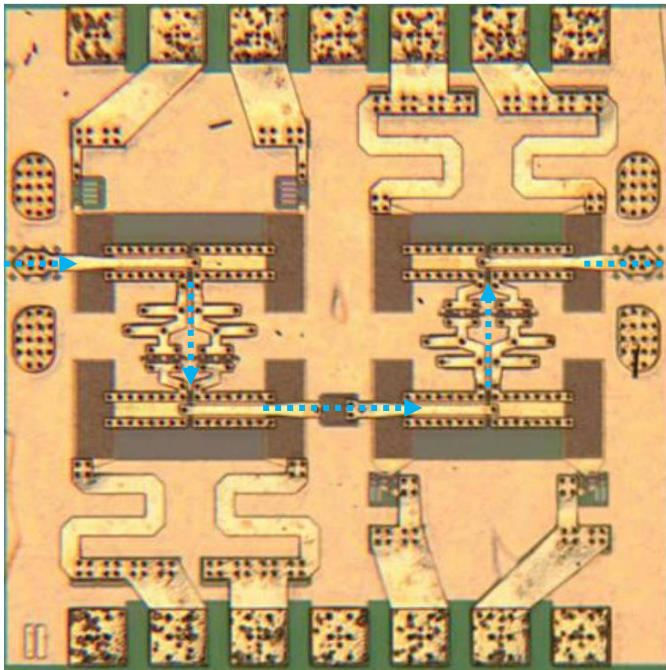


Power density (power/die area)
= 294 mW/mm² (including RF pads)
= 1210 mW/mm² (core area)

[H. Park et al, CSICS 2013]

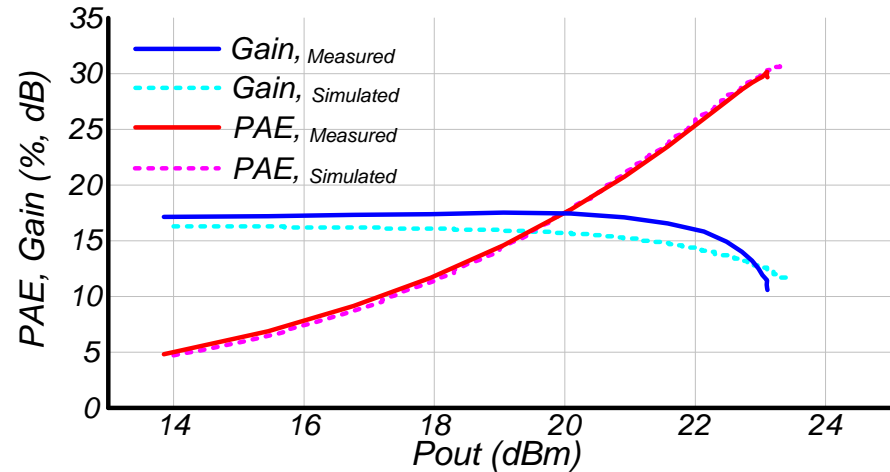
30% PAE W-Band InP Power Amplifiers Using Sub-Quarter-Wavelength Baluns for Series-Connected Power-Combining

Two-Stage PA IC Test Results (86GHz)



IC size: 825 x 820 μm^2

Large signal measurements



Gain: 17.5 dB

P_{SAT} : >200 mW @ 3.0 V

PAE: >30 %

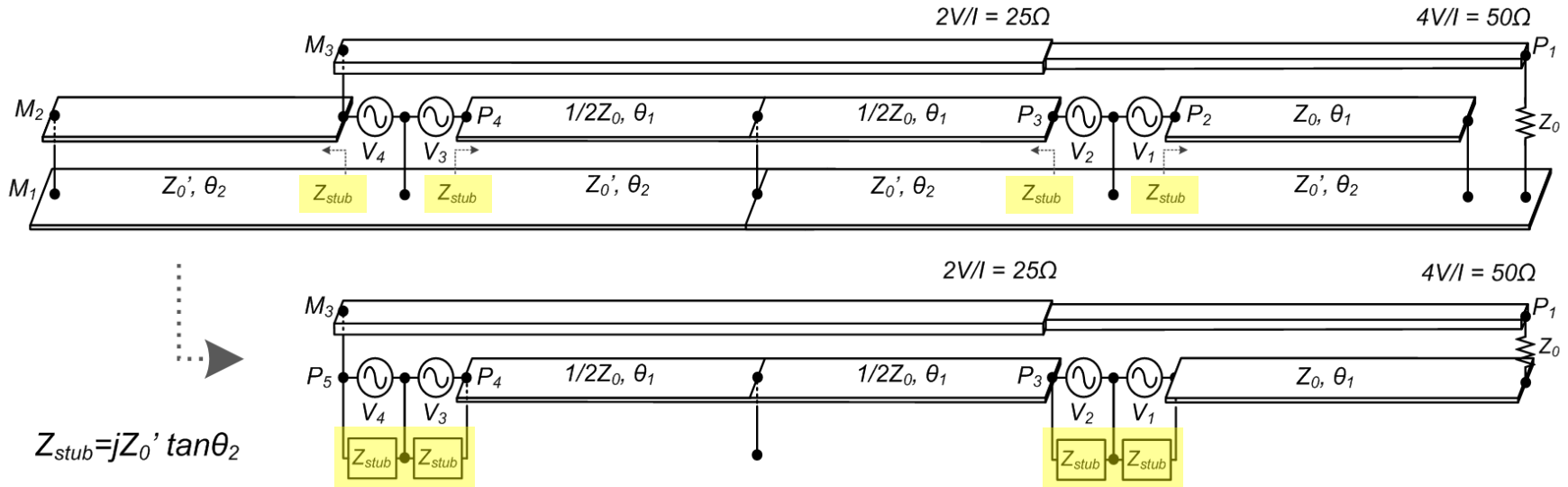
Power density (power/die area)
= 307 mW/mm² (including RF pads)
= 927 mW/mm² (core area)

[H. Park et al, CSICS 2013]

30% PAE W-Band InP Power Amplifiers Using Sub-Quarter-Wavelength Baluns for Series-Connected Power-Combining

16:1 PA Using 4:1 Baluns

4:1 series-connected power-combining



Each HBT loaded by 12.5Ω

HBT junction area selected
so that $I_{max} = V_{max} / 12.5\Omega$

Each HBT has some C_{OUT}

Stub length picked so that
 $Z_{stub} = -1/j\omega C_{out} \rightarrow$ tunes HBT

$$P_{out} = 16 \times \left(\frac{V_{max}^2}{8 \cdot 50\Omega} \right)$$

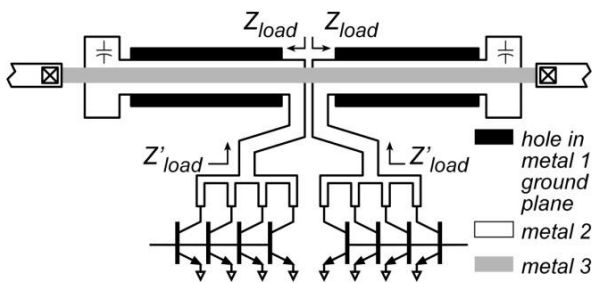
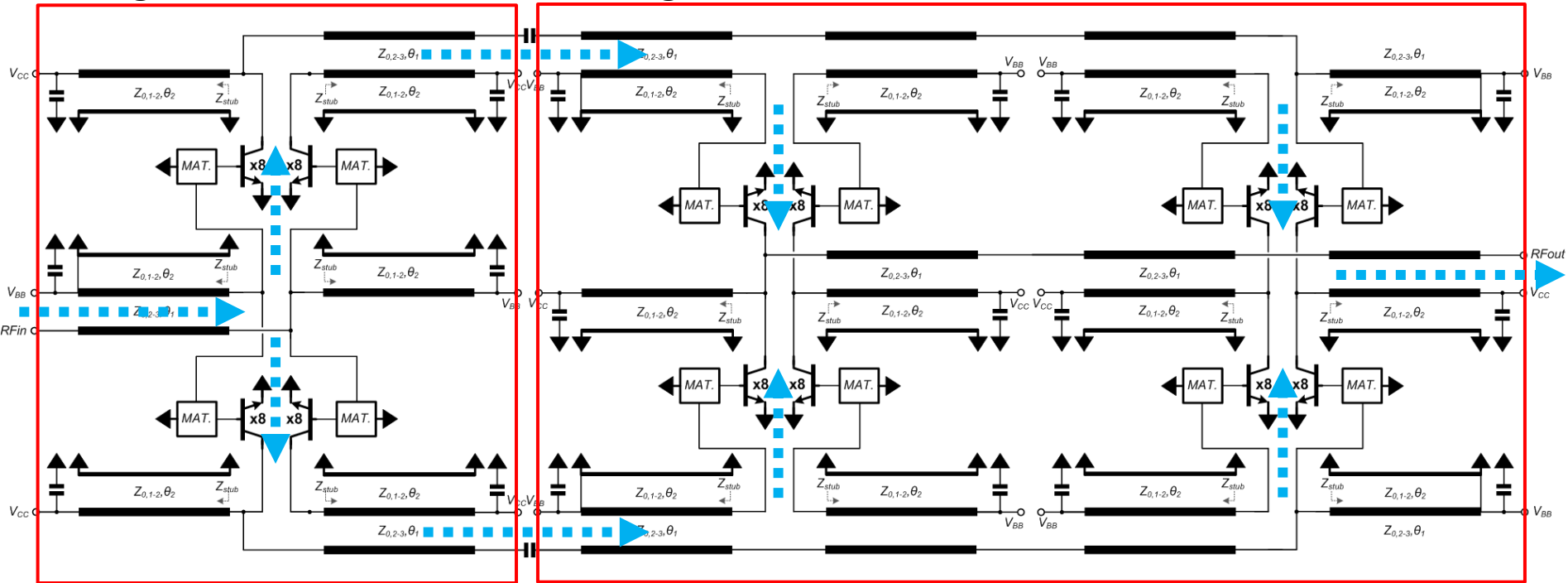
16:1 more power
than without combiner.

PA IC Schematic (2-stages)

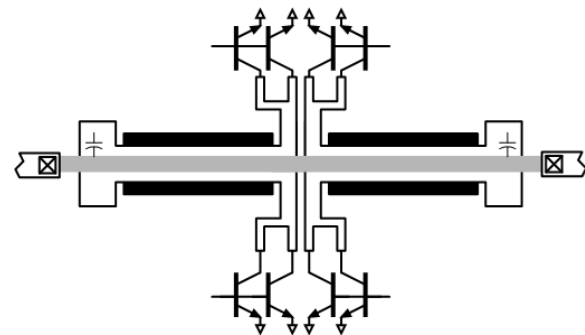
2-stage PA using 2:1 and 4:1 baluns

1st stage

2nd stage

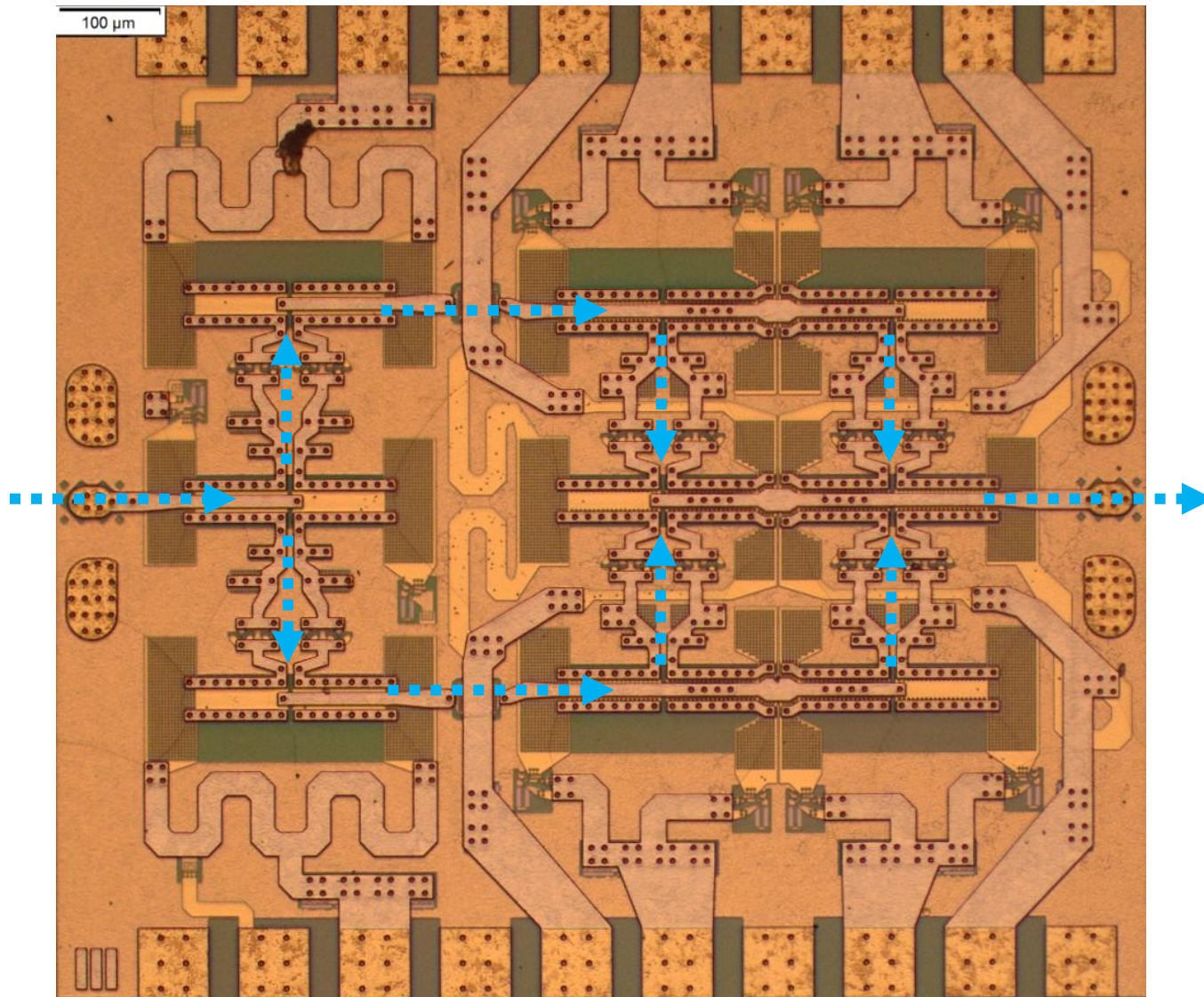


Long lead lines
 $Z_{load} \neq Z'_{load}$



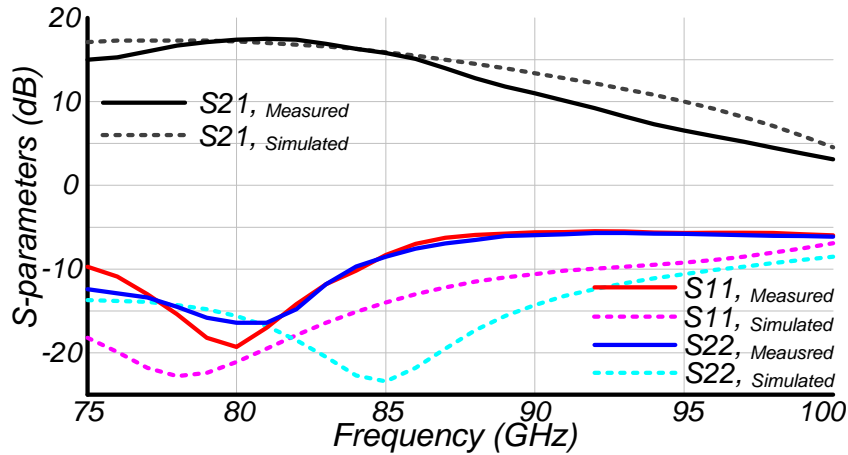
PA IC Die Image (2-stages)

IC Size: 1.08 x 0.98 mm²



PA IC Test Results (81 GHz)

Small signal measurements



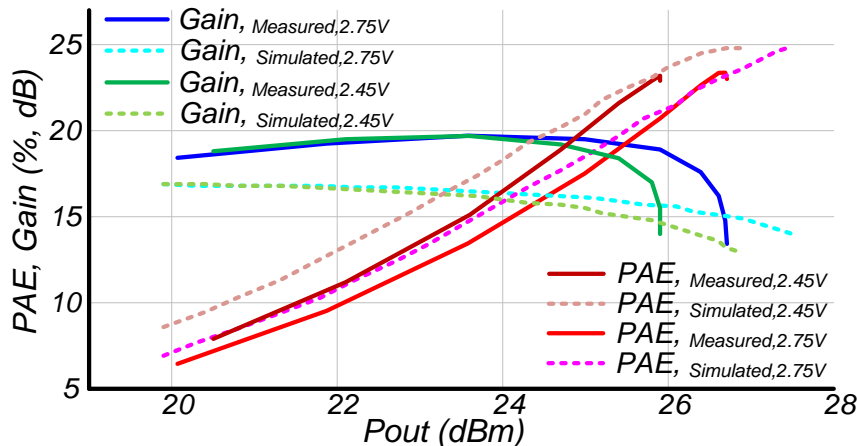
x16 larger output power than 50 Ohm R_{OPT} device

Gain: 17.8dB

Output Power: 470mW @2.75 V

PAE: 23.4%

Large signal measurements



Power density (power/die area)
= 443 mW/mm² (including pads)
= 1020 mW/mm² (only core area)

mm-Wave Power Combiners

Ref.	Tech.	Type	N-way	Freq. (GHz)	IL (dB)	Size (mm ²)
This work	0.25 μ m InP HBT	Sub- $\lambda/4$ TL	2:1	86 (60-105)	0.52 (0.68)	0.03
This work	0.25 μ m InP HBT	Sub- $\lambda/4$ TL (ring)	2:1	86 (60-110)	0.50 (0.63)	0.04
This work	0.25 μ m InP HBT	Sub- $\lambda/4$ TL	4:1	87 (75-103)	0.91 (1.32)	0.06
2012 Yi	0.13 μ m BiCMOS	TF	4:1	60 77/79	0.73* 1.20*	0.015
2013 Thian	0.18 μ m BiCMOS	TF	8:1	83.5 (70.5-85)	1.25 (0.80*)	0.02 [#]
2010 Chen	65 nm CMOS	TF	4:1	60	0.63*	0.02 [#]
2010 Law	90 nm CMOS	Wilkinson	2:1	60	0.54	0.08
2014 Zhao	40 nm CMOS	Series/ parallel TF	4:1	75 (65-90)	0.92* (1.0)	0.05 [#]
2007 Niknejad	90 nm CMOS	TL	4:1	60 (55-65)	1.09* (1.25*)	-
2007 Liu	0.18 μ m CMOS	Marchand	2:1	57	3.40	0.55
2005 Hamed	InGaP/GaAs	Marchand	2:1	(15-45)	(1.50)	0.40

*Simulation results, [#]Area estimated by chip image. IL: insertion loss, TF: transformer, and TL: transmission-line. Parentheses in the frequency and insertion loss columns indicate worst-case insertion loss over the indicated bandwidth.

mm-Wave Power Amplifiers

Ref.	Tech. f_{\max}/f_t (GHz)	Freq. (GHz)	BW (GHz)	Max. S_{21} (dB)	P_{out} (dBm)	Peak PAE (%)	V_{CC} or V_{DD} (V)	Size (mm ²)	mW /mm ²
This work	0.25 μm InP HBT 525 / 285	86	23	9.4	20.4	30.4	2.5	0.37 0.09*	294 1210*
This work	0.25 μm InP HBT 525 / 285	86	33	10.2	20.8	35.0	2.5	0.43 0.14*	285 858*
This Work	0.25 μm InP HBT 525 / 285	81	>11.5	17.5	26.7	23.4	2.75	1.06 0.46*	443 1020*
2011 Brown	0.14 μm GaN HEMT	91	7+	16.0	30.8	>20.0	17.5	2.25	530
2012 Micovic	0.14 μm GaN HEMT 230 / 97	95	10+	18.0+	31.5+	20.5+	12.0	-	-
2012 Yi	0.13 μm BiCMOS 270 / 240	62 84	>10 >8	20.6 27.0	20.1 18.0	18.0 9.0	1.8 2.5	0.72 0.68	142 93
2013 Agah	45 nm SOI CMOS	89	10+	10.3	15.8	11.0	2.8	0.37 0.05*	103 760*
2013 Thian	0.18 μm BiCMOS 250 / 170	78	8.9	18.3	14	2.0	3.2	0.85*	29*
2010 Chen	65nm CMOS	60	9	20.3	18.6	15.1	1.0	0.28*	256*
2010 Law	90nm CMOS	60	8	20.6	19.9	14.2	1.2	1.76	55
2014 Zhao	40nm CMOS	80	15.2	18.1	20.9	22.3	0.9	0.19*	647*

*IC core area (excluding DC feed lines and RF pads), +Value estimated from figure, ^c)Corporate transmission-line power-combiners, ^s)Stacked PA.

Conclusion

Sub- $\lambda/4$ baluns for series-power-combining using a low V_{BV} device

Low-loss **<0.6dB** @ 2:1 balun, **<0.92dB** loss @ 4:1 balun

→ High power, high efficiency, compact PA IC designs

W-band power amplifiers using the 2:1 & 4:1 baluns

Record **>30 % PAE** @ 100 mW, 200 mW, **23.4 % PAE @470 mW**

Record 23 GHz 3-dB bandwidth, >10GHz 3-dB BW

Record **1210 mW/mm²** power density, **1020 mW/mm²**

Future directions

220GHz PA designs using the sub- $\lambda/4$ baluns

SiGe PA designs with the optimized balun structures

Phased arrays at K/V/E/W bands

Thanks for your attention!

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